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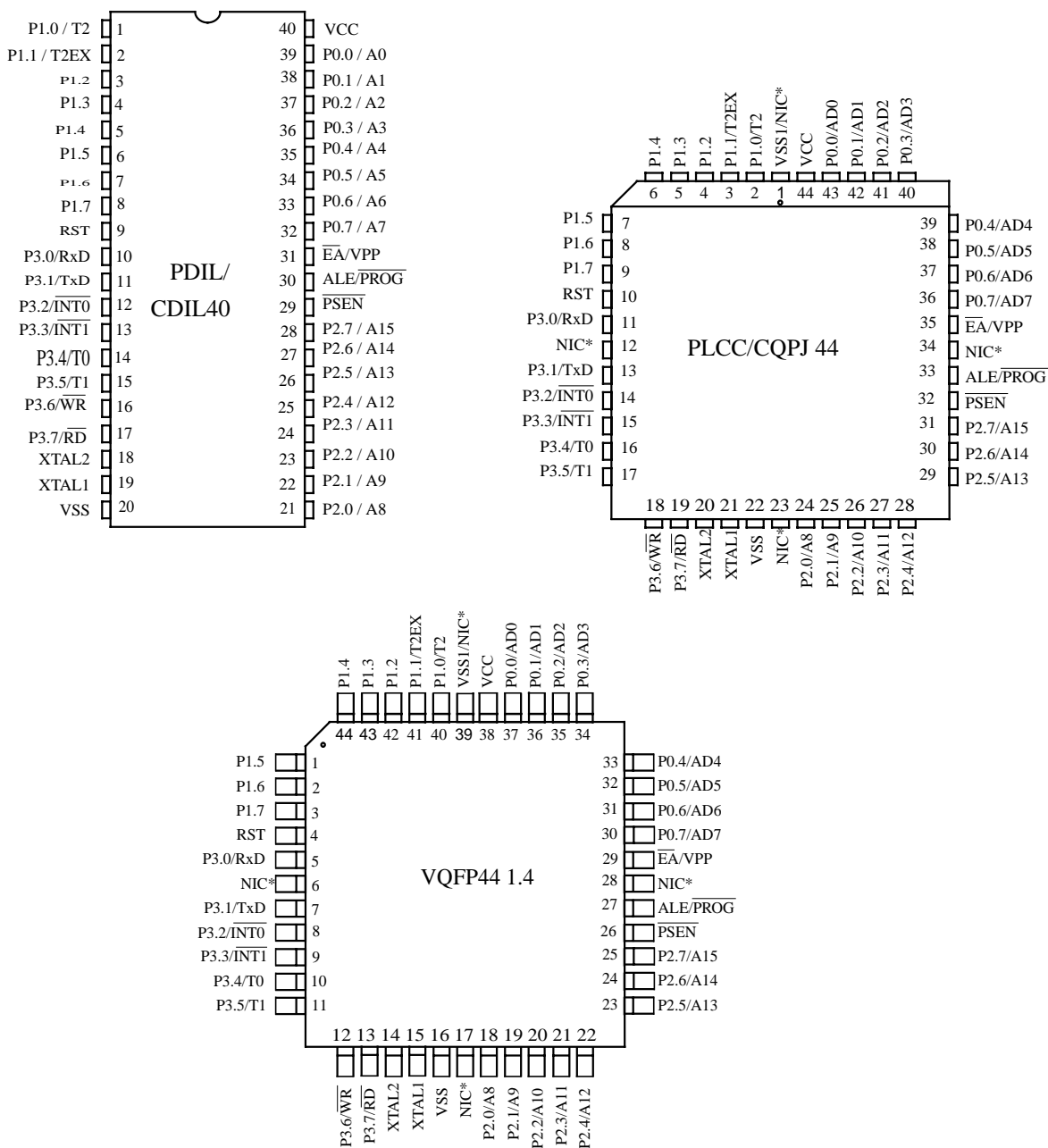
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rc2-lie">https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rc2-lie</a>

## 5. Pin Configuration



\*NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name And Function
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
$\overline{\text{PSEN}}$	29	32	26	O	<b>Program Store ENable:</b> The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/\text{V}_{\text{PP}}$	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC). $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage ( $\text{V}_{\text{PP}}$ ) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier

## 5.1. Pin Description for 64/68 pin Packages

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1 written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

**Table 2. 64/68 Pin Packages Configuration**

	<b>PLCC68</b>	<b>SQUARE VQFP64 1.4</b>
VSS	51	9/40
VCC	17	8
P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

## 6. TS80C51Rx2 Enhanced Features

In comparison to the original 80C52, the TS80C51Rx2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The extended RAM.
- The Programmable Counter Array (PCA).
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

### 6.1. X2 Feature

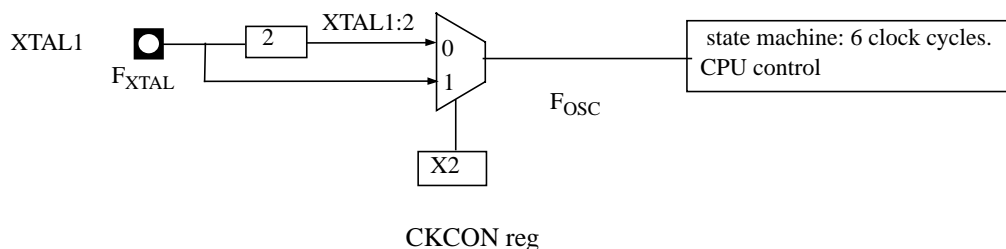
The TS80C51Rx2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

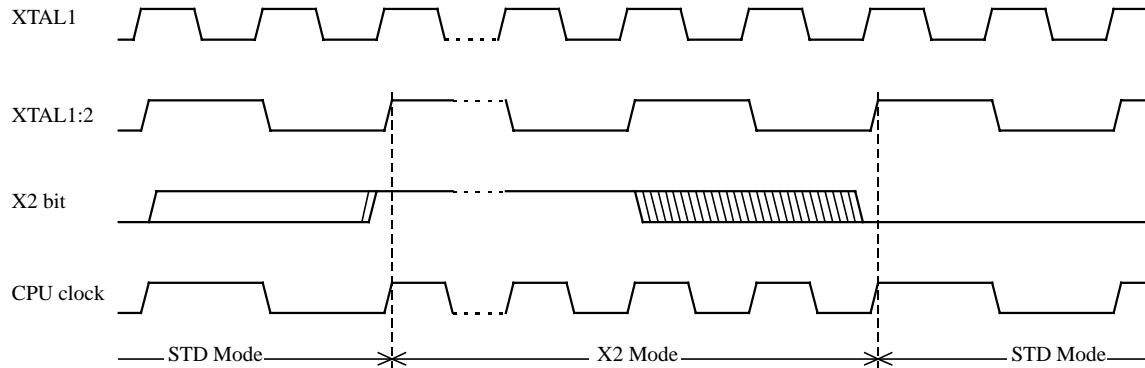
In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

#### 6.1.1. Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.



**Figure 1. Clock Generation Diagram**



**Figure 2. Mode Switching Waveforms**

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

#### **CAUTION**

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

**Table 3. CKCON Register**

**CKCON - Clock Control Register (8Fh)**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	<b>X2</b>

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
0	X2	<b>CPU and peripheral clock bit</b> Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$ ). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$ ).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel-wm.com>)

## ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000    MOV DPTR,#SOURCE      ; address of SOURCE
0003 05A2      INC  AUXR1             ; switch data pointers
0005 90A000    MOV DPTR,#DEST        ; address of DEST
0008           LOOP:
0008 05A2      INC  AUXR1             ; switch data pointers
000A E0        MOVX A,@DPTR           ; get a byte from SOURCE
000B A3        INC  DPTR              ; increment SOURCE address
000C 05A2      INC  AUXR1             ; switch data pointers
000E F0        MOVX @DPTR,A           ; write the byte to DEST
000F A3        INC  DPTR              ; increment DEST address
0010 70F6      JNZ  LOOP              ; check for 0 terminator
0012 05A2      INC  AUXR1             ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



## **6.4. Timer 2**

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6) and T2MOD register (See Table 7). Timer 2 operation is similar to Timer 0 and Timer 1.  $C/\overline{T2}$  selects  $F_{OSC}/12$  (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and  $CP/\overline{RL2}$  (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### **6.4.1. Auto-Reload Mode**

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 5. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

Table 10. CCAPMn: PCA Modules Compare/Capture Control Registers

CCAPMn Address

n = 0 - 4

CCAPM0=0DAH

CCAPM1=0DBH

CCAPM2=0DCH

CCAPM3=0DDH

CCAPM4=0DEH

	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Reset value	X	0	0	0	0	0	0	0

Symbol	Function
-	Not implemented, reserved for future use. <sup>a</sup>
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

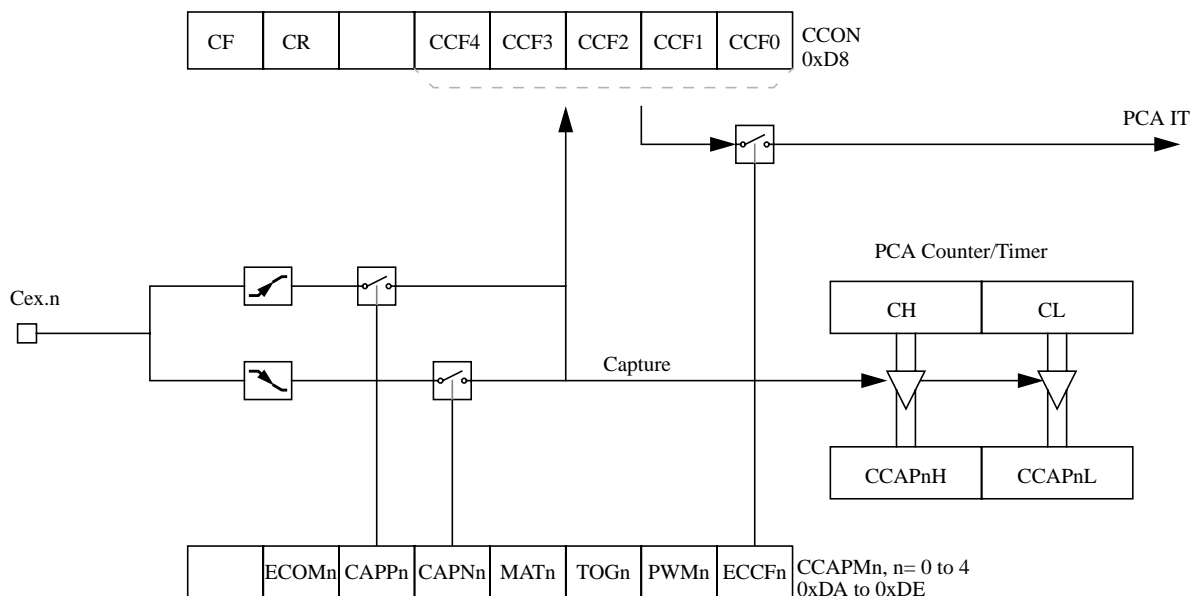
Table 11. PCA Module Modes (CCAPMn Registers)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module Function
0	0	0	0	0	0	0	No Operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
1	0	0	1	0	0	X	16-bit Software Timer / Compare mode.
1	0	0	1	1	0	X	16-bit High Speed Output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	Watchdog Timer (module 4 only)

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 12 & Table 13)

### 6.5.1. PCA Capture Mode

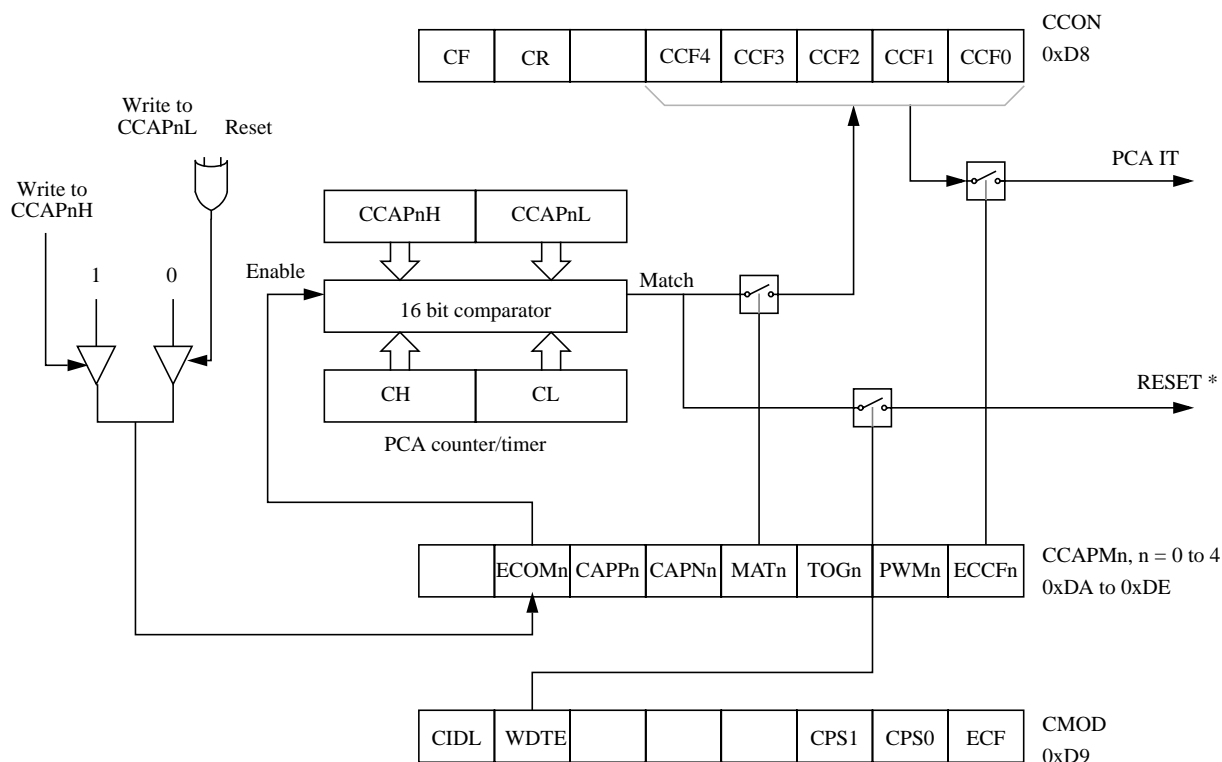
To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 9).



**Figure 9. PCA Capture Mode**

## 6.5.2. 16-bit Software Timer / Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 10).



\* Only for Module 4

**Figure 10. PCA Compare Mode and PCA Watchdog Timer**

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

Table 18. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 19. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	<b>Enable All interrupt bit</b> Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	EC	<b>PCA interrupt enable bit</b> Clear to disable . Set to enable.
5	ET2	<b>Timer 2 overflow interrupt Enable bit</b> Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	<b>Serial port Enable bit</b> Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	<b>Timer 1 overflow interrupt Enable bit</b> Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	<b>External interrupt 1 Enable bit</b> Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	<b>Timer 0 overflow interrupt Enable bit</b> Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	<b>External interrupt 0 Enable bit</b> Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b

Bit addressable

## 6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

### 6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is  $96 \times T_{OSC}$ , where  $T_{OSC} = 1/F_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a  $2^7$  counter has been added to extend the Time-out capability, ranking from 16ms to 2s @  $F_{OSC} = 12\text{MHz}$ . To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

**Table 23. WDTRST Register**

**WDTRST Address (0A6h)**

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

## **6.11. ONCE™ Mode (ON Chip Emulation)**

The ONCE mode facilitates testing and debugging of systems using TS80C51Rx2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51Rx2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and  $\overline{\text{PSEN}}$  is high.
- Hold ALE low as RST is deactivated.

While the TS80C51Rx2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 25. External Pin Status during ONCE Mode**

<b>ALE</b>	<b>PSEN</b>	<b>Port 0</b>	<b>Port 1</b>	<b>Port 2</b>	<b>Port 3</b>	<b>XTAL1/2</b>
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

## 6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by  $V_{CC}$  switch-on. A warm start reset occurs while  $V_{CC}$  is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when  $V_{CC}$  rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a  $V_{CC}$  range from 4.5V to 5.5V. For lower  $V_{CC}$  value, reading POF bit will return indeterminate value.

**Table 26. PCON Register**

**PCON - Power Control Register (87h)**

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	POF	<b>Power-Off Flag</b> Clear to recognize next reset type. Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	<b>Power-Down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable



## 10. Electrical Characteristics

### 10.1. Absolute Maximum Ratings <sup>(1)</sup>

Ambiant Temperature Under Bias:

C = commercial

0°C to 70°C

I = industrial

-40°C to 85°C

Storage Temperature

-65°C to + 150°C

Voltage on  $V_{CC}$  to  $V_{SS}$

-0.5 V to + 7 V

Voltage on  $V_{PP}$  to  $V_{SS}$

-0.5 V to + 13 V

Voltage on Any Pin to  $V_{SS}$

-0.5 V to  $V_{CC} + 0.5$  V

Power Dissipation

1 W<sup>(2)</sup>

#### NOTES

1. Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

### 10.2. Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating  $I_{cc}$  measurements under reset, which made sense for the designs where the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating  $I_{cc}$ :

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA =  $V_{CC}$ , RST =  $V_{SS}$ , XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating  $I_{cc}$ .

### 10.3. DC Parameters for Standard Voltage

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $F = 0$  to  $40\text{ MHz}$ .

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $F = 0$  to  $40\text{ MHz}$ .

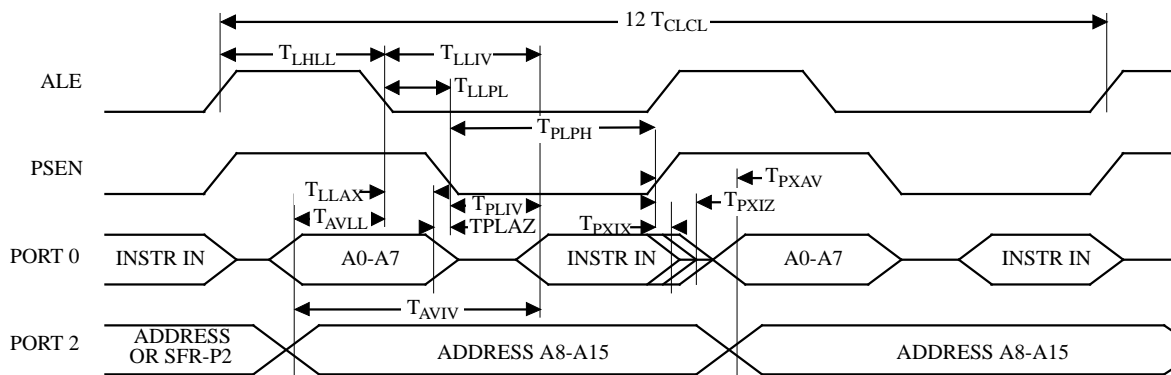
**Table 32. DC Parameters in Standard Voltage**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
$V_{IH}$	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
$V_{IH1}$	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage, ports 1, 2, 3, 4, 5 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 100\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 1.6\text{ mA}$ <sup>(4)</sup> $I_{OL} = 3.5\text{ mA}$ <sup>(4)</sup>
$V_{OL1}$	Output Low Voltage, port 0 <sup>(6)</sup>			0.3 0.45 1.0	V V V	$I_{OL} = 200\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 3.2\text{ mA}$ <sup>(4)</sup> $I_{OL} = 7.0\text{ mA}$ <sup>(4)</sup>
$V_{OL2}$	Output Low Voltage, ALE, $\overline{\text{PSEN}}$			0.3 0.45 1.0	V V V	$I_{OL} = 100\text{ }\mu\text{A}$ <sup>(4)</sup> $I_{OL} = 1.6\text{ mA}$ <sup>(4)</sup> $I_{OL} = 3.5\text{ mA}$ <sup>(4)</sup>
$V_{OH}$	Output High Voltage, ports 1, 2, 3, 4, 5	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10\text{ }\mu\text{A}$ $I_{OH} = -30\text{ }\mu\text{A}$ $I_{OH} = -60\text{ }\mu\text{A}$ $V_{CC} = 5\text{ V} \pm 10\%$
$V_{OH1}$	Output High Voltage, port 0	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -200\text{ }\mu\text{A}$ $I_{OH} = -3.2\text{ mA}$ $I_{OH} = -7.0\text{ mA}$ $V_{CC} = 5\text{ V} \pm 10\%$
$V_{OH2}$	Output High Voltage, ALE, $\overline{\text{PSEN}}$	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -100\text{ }\mu\text{A}$ $I_{OH} = -1.6\text{ mA}$ $I_{OH} = -3.5\text{ mA}$ $V_{CC} = 5\text{ V} \pm 10\%$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
$I_{IL}$	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	$\mu\text{A}$	$V_{in} = 0.45\text{ V}$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu\text{A}$	$0.45\text{ V} < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	$\mu\text{A}$	$V_{in} = 2.0\text{ V}$
$C_{IO}$	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup>	50	$\mu\text{A}$	$2.0\text{ V} < V_{CC} < 5.5\text{ V}$ <sup>(3)</sup>
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5\text{ V}$ <sup>(1)</sup>

**Table 38. AC Parameters for a Variable Clock: derating formula**

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{LHLL}$	Min	$2 T - x$	$T - x$	10	8	15	ns
$T_{AVLL}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLAX}$	Min	$T - x$	$0.5 T - x$	15	13	20	ns
$T_{LLIV}$	Max	$4 T - x$	$2 T - x$	30	22	35	ns
$T_{LLPL}$	Min	$T - x$	$0.5 T - x$	10	8	15	ns
$T_{PLPH}$	Min	$3 T - x$	$1.5 T - x$	20	15	25	ns
$T_{PLIV}$	Max	$3 T - x$	$1.5 T - x$	40	25	45	ns
$T_{PXIX}$	Min	x	x	0	0	0	ns
$T_{PXIZ}$	Max	$T - x$	$0.5 T - x$	7	5	15	ns
$T_{AVIV}$	Max	$5 T - x$	$2.5 T - x$	40	30	45	ns
$T_{PLAZ}$	Max	x	x	10	10	10	ns

### 10.5.3. External Program Memory Read Cycle

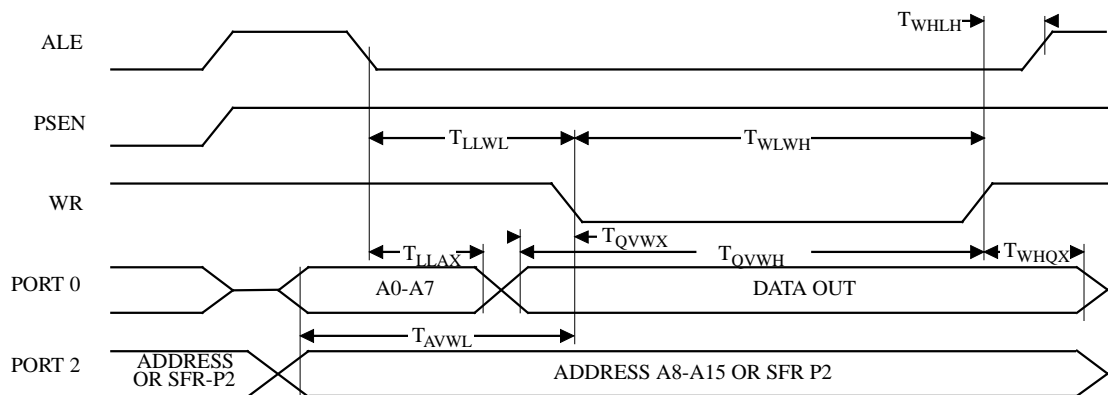


**Figure 25. External Program Memory Read Cycle**

**Table 41. AC Parameters for a Variable Clock: derating formula**

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{RLRH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{WLWH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{RLDV}$	Max	5 T - x	2.5 T - x	25	23	30	ns
$T_{RHDx}$	Min	x	x	0	0	0	ns
$T_{RHDZ}$	Max	2 T - x	T - x	20	15	25	ns
$T_{LLDV}$	Max	8 T - x	4T - x	40	35	45	ns
$T_{AVDV}$	Max	9 T - x	4.5 T - x	60	50	65	ns
$T_{LLWL}$	Min	3 T - x	1.5 T - x	25	20	30	ns
$T_{LLWL}$	Max	3 T + x	1.5 T + x	25	20	30	ns
$T_{AVWL}$	Min	4 T - x	2 T - x	25	20	30	ns
$T_{QVWX}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{QVWH}$	Min	7 T - x	3.5 T - x	15	10	20	ns
$T_{WHQX}$	Min	T - x	0.5 T - x	10	8	15	ns
$T_{RLAZ}$	Max	x	x	0	0	0	ns
$T_{WHLH}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{WHLH}$	Max	T + x	0.5 T + x	15	10	20	ns

### 10.5.5. External Data Memory Write Cycle

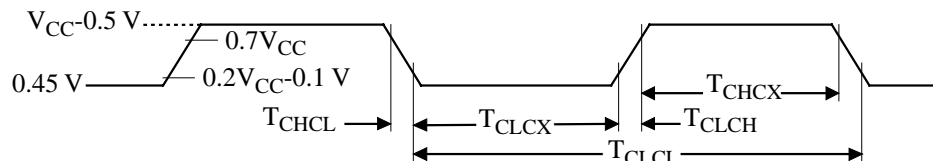

**Figure 26. External Data Memory Write Cycle**

### 10.5.11. External Clock Drive Characteristics (XTAL1)

**Table 46. AC Parameters**

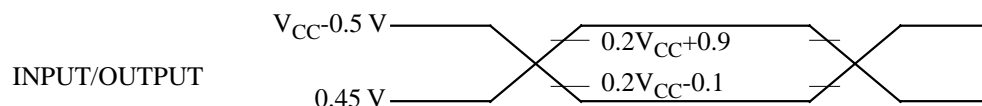
Symbol	Parameter	Min	Max	Units
$T_{CLCL}$	Oscillator Period	25		ns
$T_{CHCX}$	High Time	5		ns
$T_{CLCX}$	Low Time	5		ns
$T_{CLCH}$	Rise Time		5	ns
$T_{CHCL}$	Fall Time		5	ns
$T_{CHCX}/T_{CLCX}$	Cyclic ratio in X2 mode	40	60	%

### 10.5.12. External Clock Drive Waveforms



**Figure 30. External Clock Drive Waveforms**

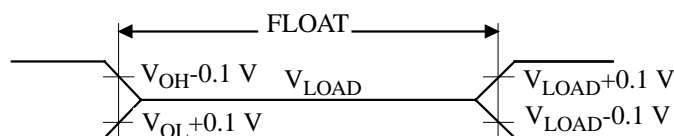
### 10.5.13. AC Testing Input/Output Waveforms



**Figure 31. AC Testing Input/Output Waveforms**

AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at  $V_{IH}$  min for a logic “1” and  $V_{IL}$  max for a logic “0”.

### 10.5.14. Float Waveforms



**Figure 32. Float Waveforms**