



#### Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rc2-mca

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# 4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

#### Table 1. All SFRs with their address and their reset value

	Bit addressable	Non Bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		F
F0h	B 0000 0000								F
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		E
E0h	ACC 0000 0000								E
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		D
D0h	PSW 0000 0000								D
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			C
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C
B8h	IP X000 000	SADEN 0000 0000							B
B0h	P3 1111 1111							IPH X000 0000	В
A8h	IE 0000 0000	SADDR 0000 0000							A
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A
98h	SCON 0000 0000	SBUF XXXX XXXX							91
90h	P1 1111 1111								9
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	81
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	8
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved







Mnemonic	]	Pin Nu	mber	Туре	Name And Function
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	0	<b>Program Store ENable:</b> The read strobe to external program memory. When executing code from the external program memory, $\overrightarrow{PSEN}$ is activated twice each machine cycle, except that two $\overrightarrow{PSEN}$ activations are skipped during each access to external data memory. $\overrightarrow{PSEN}$ is not activated during fetches from internal program memory.
EA/V <sub>pp</sub>	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V <sub>PP</sub> ) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	Ι	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier



	PLCC68	SQUARE VQFP64 1.4
P3.2	40	29
P3.3	41	30
P3.4	42	31
P3.5	43	32
P3.6	45	34
P3.7	47	36
RESET	30	21
ALE/PROG	68	56
PSEN	67	55
EA/VPP	2	58
XTAL1	49	38
XTAL2	48	37
P4.0	20	11
P4.1	24	15
P4.2	26	17
P4.3	44	33
P4.4	46	35
P4.5	50	39
P4.6	53	42
P4.7	57	46
P5.0	60	49
P5.1	62	51
P5.2	63	52
P5.3	7	62
P5.4	8	63
P5.5	10	1
P5.6	13	4
P5.7	16	7



# 6. TS80C51Rx2 Enhanced Features

In comparison to the original 80C52, the TS80C51Rx2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The extended RAM.
- The Programmable Counter Array (PCA).
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

## 6.1. X2 Feature

The TS80C51Rx2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

### 6.1.1. Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.



Figure 1. Clock Generation Diagram



### Table 3. CKCON Register

### CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description				
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.				
6	-	eserved The value read from this bit is indeterminate. Do not set this bit.				
5	-	eserved The value read from this bit is indeterminate. Do not set this bit.				
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.				
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.				
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.				
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.				
0	X2	<b>CPU and peripheral clock bit</b> Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$ ). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$ ).				

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)



### Table 7. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

			,				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	Timer 2 Output Enable bit Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	<b>Down Counter Enable bit</b> Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b Not bit addressable



## 6.5. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency  $\div$  12 ( $\div$  6 in X2 mode)
- Oscillator frequency  $\div$  4 ( $\div$  2 in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

**The PCA timer** is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)



## 6.5.3. High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 11).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.



Figure 11. PCA High Speed Output Mode

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.



Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 14. and Figure 15.).







Figure 15. UART Timings in Modes 2 and 3

### 6.6.2. Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).



### 6.6.5. Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

### SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b Not bit addressable

#### SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b Not bit addressable



### Table 18. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

### Table 19. IE Register

#### IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ЕТО	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	EC	PCA interrupt enable bit Clear to disable . Set to enable.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit         Clear to disable timer 1 overflow interrupt.         Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b Bit addressable



### Table 20. IP Register

#### **IP - Interrupt Priority Register (B8h)**

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	PPC	PCA interrupt priority bit Refer to PPCH for priority level.
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.
4	PS	Serial port Priority bit Refer to PSH for priority level.
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.

Reset Value = X000 0000b Bit addressable



## 6.8. Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

## 6.9. Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 17., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated.  $V_{CC}$  can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts  $\overline{INT0}$  and  $\overline{INT1}$  are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 17. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C51Rx2 into power-down mode.



### Figure 17. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content. NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.



## 6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

## 6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x  $T_{OSC}$ , where  $T_{OSC} = 1/F_{OSC}$ . To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a  $2^7$  counter has been added to extend the Time-out capability, ranking from 16ms to 2s @  $F_{OSC} = 12$ MHz. To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

### Table 23. WDTRST Register

#### WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	Х	Х	Х	Х	Х	Х	Х

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.



# 7. TS83C51RB2/RC2/RD2 ROM

## 7.1. ROM Structure

The TS83C51RB2/RC2/RD2 ROM memory is divided in three different arrays:

•	the code array:	es.
•	the encryption array:	s.
•	the signature array:	es.

# 7.2. ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

## 7.2.1. 7.2.1. Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

## 7.2.2. Program Lock Bits

The lock bits when programmed according to Table 28. will provide different level of protection for the on-chip code and data.

	Program	Lock Bits		
Security level	LB1	LB2	LB3	Protection description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Р	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset.
3	U	Р	U	Same as level 1+ Verify disable. This security level is only available for 51RDX2 devices.

Table	28.	Program	Lock	bits
-------	-----	---------	------	------

U: unprogrammed

P: programmed

## 7.2.3. Signature bytes

The TS83C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

### 7.2.4. Verify Algorithm

Refer to 8.3.4.



# **10. Electrical Characteristics**

## 10.1. Absolute Maximum Ratings <sup>(1)</sup>

Ambiant Temperature Under Bias:	
C = commercial	0°C to 70°C
I = industrial	-40°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V <sub>CC</sub> to V <sub>SS</sub>	-0.5 V to + 7 V
Voltage on V <sub>PP</sub> to V <sub>SS</sub>	-0.5 V to + 13 V
Voltage on Any Pin to V <sub>SS</sub>	-0.5 V to $V_{CC}$ + 0.5 V
Power Dissipation	$1 W^{(2)}$

NOTES

1. Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

### 10.2. Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.



## **10.5.2. External Program Memory Characteristics**

Table 36. Symbol Description	Table 3	36.	Symbol	Description
------------------------------	---------	-----	--------	-------------

Symbol	Parameter
Т	Oscillator clock period
T <sub>LHLL</sub>	ALE pulse width
T <sub>AVLL</sub>	Address Valid to ALE
T <sub>LLAX</sub>	Address Hold After ALE
T <sub>LLIV</sub>	ALE to Valid Instruction In
T <sub>LLPL</sub>	ALE to PSEN
T <sub>PLPH</sub>	PSEN Pulse Width
T <sub>PLIV</sub>	PSEN to Valid Instruction In
T <sub>PXIX</sub>	Input Instruction Hold After PSEN
T <sub>PXIZ</sub>	Input Instruction FloatAfter PSEN
T <sub>PXAV</sub>	PSEN to Address Valid
T <sub>AVIV</sub>	Address to Valid Instruction In
T <sub>PLAZ</sub>	PSEN Low to Address Float

## Table 37. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Т	25		33		25		50		33		ns
T <sub>LHLL</sub>	40		25		42		35		52		ns
T <sub>AVLL</sub>	10		4		12		5		13		ns
T <sub>LLAX</sub>	10		4		12		5		13		ns
T <sub>LLIV</sub>		70		45		78		65		98	ns
T <sub>LLPL</sub>	15		9		17		10		18		ns
T <sub>PLPH</sub>	55		35		60		50		75		ns
T <sub>PLIV</sub>		35		25		50		30		55	ns
T <sub>PXIX</sub>	0		0		0		0		0		ns
T <sub>PXIZ</sub>		18		12		20		10		18	ns
T <sub>AVIV</sub>		85		53		95		80		122	ns
T <sub>PLAZ</sub>		10		10		10		10		10	ns



Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T <sub>RLRH</sub>	130		85		135		125		175		ns
T <sub>WLWH</sub>	130		85		135		125		175		ns
T <sub>RLDV</sub>		100		60		102		95		137	ns
T <sub>RHDX</sub>	0		0		0		0		0		ns
T <sub>RHDZ</sub>		30		18		35		25		42	ns
T <sub>LLDV</sub>		160		98		165		155		222	ns
T <sub>AVDV</sub>		165		100		175		160		235	ns
T <sub>LLWL</sub>	50	100	30	70	55	95	45	105	70	130	ns
T <sub>AVWL</sub>	75		47		80		70		103		ns
T <sub>QVWX</sub>	10		7		15		5		13		ns
T <sub>QVWH</sub>	160		107		165		155		213		ns
T <sub>WHQX</sub>	15		9		17		10		18		ns
T <sub>RLAZ</sub>		0		0		0		0		0	ns
T <sub>WHLH</sub>	10	40	7	27	15	35	5	45	13	53	ns

Table 40. AC Parameters for a Fix Clock



## **10.5.9. EPROM Programming and Verification Characteristics**

TA = 21°C to 27°C;  $V_{SS} = 0V$ ;  $V_{CC} = 5V \pm 10\%$  while programming.  $V_{CC}$  = operating range while verifying

Symbol	Parameter	Min	Max	Units	
V <sub>PP</sub>	Programming Supply Voltage	12.5	13	V	
I <sub>PP</sub>	Programming Supply Current		75	mA	
1/T <sub>CLCL</sub>	Oscillator Frquency	4	6	MHz	
T <sub>AVGL</sub>	Address Setup to PROG Low	48 T <sub>CLCL</sub>			
T <sub>GHAX</sub>	Adress Hold after PROG	48 T <sub>CLCL</sub>			
T <sub>DVGL</sub>	Data Setup to PROG Low	48 T <sub>CLCL</sub>			
T <sub>GHDX</sub>	Data Hold after PROG	48 T <sub>CLCL</sub>			
T <sub>EHSH</sub>	(Enable) High to V <sub>PP</sub>	48 T <sub>CLCL</sub>			
T <sub>SHGL</sub>	V <sub>PP</sub> Setup to PROG Low	10		μs	
T <sub>GHSL</sub>	V <sub>PP</sub> Hold after PROG	10		μs	
T <sub>GLGH</sub>	PROG Width	90	110	μs	
T <sub>AVQV</sub>	Address to Valid Data		48 T <sub>CLCL</sub>		
T <sub>ELQV</sub>	ENABLE Low to Data Valid		48 T <sub>CLCL</sub>		
T <sub>EHQZ</sub>	Data Float after ENABLE	0	48 T <sub>CLCL</sub>		

### Table 45. EPROM Programming Parameters

### 10.5.10. EPROM Programming and Verification Waveforms



\* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

### Figure 29. EPROM Programming and Verification Waveforms