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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rd2-lcmd

Email: info@E-XFL.COM

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4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

Table 1. All SFRs with their address and their reset value

	Bit addressable			Noi	n Bit address	able			
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		F
F0h	B 0000 0000								F
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		E
E0h	ACC 0000 0000								E
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		D
D0h	PSW 0000 0000								D
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			C
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C
B8h	IP X000 000	SADEN 0000 0000							B
B0h	P3 1111 1111							IPH X000 0000	В
A8h	IE 0000 0000	SADDR 0000 0000							A
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A
98h	SCON 0000 0000	SBUF XXXX XXXX							91
90h	P1 1111 1111								9
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	81
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	8
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved



Reset	9	10	4	Ι	Reset: A high on this pin for two machine cycles while the oscillator is running,
					resets the device. An internal diffused resistor to $V_{\mbox{\scriptsize SS}}$ permits a power-on reset
					using only an external capacitor to V_{CC} . If the hardware watchdog reaches its
					time-out, the reset pin becomes an output during the time the internal reset is
					activated.



Mnemonic	Pin Number		mber	Туре	Name And Function
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	0	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, \overrightarrow{PSEN} is activated twice each machine cycle, except that two \overrightarrow{PSEN} activations are skipped during each access to external data memory. \overrightarrow{PSEN} is not activated during fetches from internal program memory.
EA/V _{pp}	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	Ι	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier



Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0						
-	-	-	-	-	-	-	X2						

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)





Figure 4. Internal and External Data Memory Address

AUXR ress 08EH		-	-	-	-	-	-	EXTRA M	AO		
Reset	value	X	Х	Х	Х	Х	Х	0	0		
Symbol					Functior	1					
-	Not imp	aplemented, reserved for future use. ^a									
AO	Disable/I	le/Enable ALE									
	AO	Operating Mode									
	0	ALI X2	E is emitte mode is u	ed at a cor sed)	istant rate	of 1/6 the	oscillator	frequency (or	r 1/3 if		
	1	AL	E is active	only duri	ng a MOV	X or MO	VC instruc	tion			
EXTRAM	Internal/I	External R	AM (00H-	FFH) acce	ess using N	AOVX @	Ri/ @ DP	TR			
	EXTR	AM Op	Operating Mode								
	0	Inte	Internal XRAM access using MOVX @ Ri/ @ DPTR								
	1	Ext	ernal data	memory a	ccess						

 Table 5. Auxiliary Register AUXR

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.



6.4. Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6) and T2MOD register (See Table 7). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and $CP/\overline{RL2}$ (T2CON), as described in the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description.

Refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

6.4.1. Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel Wireless & Microcontrollers 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 5. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.





Figure 5. Auto-Reload Mode Up/Down Counter (DCEN = 1)

6.4.2. Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 6) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.



Table 12	2. CCAPnH:	PCA Modu	es Capture/C	Compare	Registers	High
----------	------------	----------	--------------	---------	-----------	------

CCAPnH Address n = 0 - 4	CCAP0H=0FAH CCAP1H=0FBH CCAP2H=0FCH CCAP3H=0FDH CCAP3H=0FEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

Table 13. CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address n = 0 - 4	CCAP0L=0EAH CCAP1L=0EBH CCAP2L=0ECH CCAP3L=0EDH CCAP4L=0EEH								
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

Table 14. CH: PCA Counter High

CH Address 0F9H									
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

Table 15. CL: PCA Counter Low

CL Address 0E9H									
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0



Table 16. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0					
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI					
Bit Number	Bit Mnemonic		Description									
7	FE	Framing Error bit Clear to reset the Set by hardware SMOD0 must be	'raming Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit									
	SM0	Serial port Mode bi Refer to SM1 fo SMOD0 must be	erial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit									
		Serial port Mode bi	t 1 [1]Mode	Descriptio	on Baud Rate	2						
6	SMI	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$										
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.										
4	REN	Reception Enable bit Clear to disable serial reception. Set to enable serial reception.										
3	TB8	Transmitter Bit 8 / Clear to transmi Set to transmit a	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.									
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.										
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.										
0	RI	Receive Interrupt fl Clear to acknow Set by hardware	ag ledge interrupt. at the end of the 8	th bit time in mode	0, see Figure 14.	and Figure 15. in	Receive Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 14. and Figure 15. in the other modes.					

Reset Value = 0000 0000b Bit addressable



6.7. Interrupt System

The TS80C51Rx2 has a total of 7 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

WARNING: Note that in the first version of RC devices, the PCA interrupt is in the lowest priority. Thus the order in INTO, TF0, INT1, TF1, RI or TI, TF2 or EXF2, PCA.



Figure 16. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 19.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 20.) and in the Interrupt Priority High register (See Table 21.). shows the bit values and priority levels associated with each combination.

The PCA interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.



Table 20. IP Register

IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Dit Number	Bit	Description					
Dit Nullibei	Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	PPC	PCA interrupt priority bit Refer to PPCH for priority level.					
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.					
4	PS	Serial port Priority bit Refer to PSH for priority level.					
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.					
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.					
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.					
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.					

Reset Value = X000 0000b Bit addressable



6.10. Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

6.10.1. Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is 96 x T_{OSC} , where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ $F_{OSC} = 12$ MHz. To manage this feature, refer to WDTPRG register description, Table 24. (SFR0A7h).

Table 23. WDTRST Register

WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	Х	Х	Х	Х	Х	Х	Х

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.





* See Table 31. for proper value on these inputs

Figure 18. Set-Up Modes Configuration

8.3.3. Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51RB2/RC2/RD2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise \overline{EA}/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/PROG once.
- Step 6: Lower \overline{EA}/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 19.).

8.3.4. Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51RB2/RC2/RD2.

P 2.7 is used to enable data output.

To verify the TS87C51RB2/RC2/RD2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 19.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.





Figure 19. Programming and Verification Signal's Waveform

8.4. EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

8.4.1. Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 μ W/cm² rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.



Symbol	Туре	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	x	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

 Table 38. AC Parameters for a Variable Clock: derating formula

10.5.3. External Program Memory Read Cycle



Figure 25. External Program Memory Read Cycle



10.5.4. External Data Memory Characteristics

Table 57. Symbol Description						
Symbol	Parameter					
T _{RLRH}	RD Pulse Width					
T _{WLWH}	WR Pulse Width					
T _{RLDV}	RD to Valid Data In					
T _{RHDX}	Data Hold After RD					
T _{RHDZ}	Data Float After RD					
T _{LLDV}	ALE to Valid Data In					
T _{AVDV}	Address to Valid Data In					
T _{LLWL}	ALE to WR or RD					
T _{AVWL}	Address to WR or RD					
T _{QVWX}	Data Valid to WR Transition					
T _{QVWH}	Data set-up to WR High					
T _{WHQX}	Data Hold After WR					
T _{RLAZ}	RD Low to Address Float					
T _{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE high					

Table 39. Symbol Description



Speed	-] 40 M	M MHz	X2 1 30 M 60 MH	V node MHz z equiv.	- standar 40 M	V °d mode MHz		L node MHz z equiv.	- standar 30 M	L rd mode MHz	Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{RLRH}	130		85		135		125		175		ns
T _{WLWH}	130		85		135		125		175		ns
T _{RLDV}		100		60		102		95		137	ns
T _{RHDX}	0		0		0		0		0		ns
T _{RHDZ}		30		18		35		25		42	ns
T _{LLDV}		160		98		165		155		222	ns
T _{AVDV}		165		100		175		160		235	ns
T _{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T _{AVWL}	75		47		80		70		103		ns
T _{QVWX}	10		7		15		5		13		ns
T _{QVWH}	160		107		165		155		213		ns
T _{WHQX}	15		9		17		10		18		ns
T _{RLAZ}		0		0		0		0		0	ns
T _{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Table 40. AC Parameters for a Fix Clock



10.5.9. EPROM Programming and Verification Characteristics

TA = 21°C to 27°C; $V_{SS} = 0V$; $V_{CC} = 5V \pm 10\%$ while programming. V_{CC} = operating range while verifying

Symbol	Parameter	Min	Max	Units
V _{PP}	Programming Supply Voltage	12.5	13	V
I _{PP}	Programming Supply Current		75	mA
1/T _{CLCL}	Oscillator Frquency	4	6	MHz
T _{AVGL}	Address Setup to PROG Low	48 T _{CLCL}		
T _{GHAX}	Adress Hold after PROG	48 T _{CLCL}		
T _{DVGL}	Data Setup to PROG Low	48 T _{CLCL}		
T _{GHDX}	Data Hold after PROG	48 T _{CLCL}		
T _{EHSH}	(Enable) High to V _{PP}	48 T _{CLCL}		
T _{SHGL}	V _{PP} Setup to PROG Low	10		μs
T _{GHSL}	V _{PP} Hold after PROG	10		μs
T _{GLGH}	PROG Width	90	110	μs
T _{AVQV}	Address to Valid Data		48 T _{CLCL}	
T _{ELQV}	ENABLE Low to Data Valid		48 T _{CLCL}	
T _{EHQZ}	Data Float after ENABLE	0	48 T _{CLCL}	

Table 45. EPROM Programming Parameters

10.5.10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Figure 29. EPROM Programming and Verification Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \ge \pm 20$ mA.

10.5.15. Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A=25^{\circ}C$ fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.



11. Ordering Information



(*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for proto typing, not for volume production. Ceramic packages are available for OTP only.

Table	47.	Maximum	Clock	Frequency
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Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	60	40	