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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rd2-mib

Email: info@E-XFL.COM

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PDIL40 PLCC44 VQFP44 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RA2	0	0	256	512	32
TS80C51RD2	0	0	768	1024	32
TS83C51RB2	16k	0	256	512	32
TS83C51RC2	32k	0	256	512	32
TS83C51RD2	64k	0	768	1024	32
TS87C51RB2	0	16k	256	512	32
TS87C51RC2	0	32k	256	512	32
TS87C51RD2	0	64k	768	1024	32

PLCC68 VQFP64 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O	
TS80C51RD2	0	0	768	1024	48	
TS83C51RD2	64k	0	768	1024	48	
TS87C51RD2	0	64k	768	1024	48	

3. Block Diagram





Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0					
-	-	-	-	-	-	-	X2					

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)





Figure 4. Internal and External Data Memory Address

AUXR ess 08EH		-	-	-	-	-	-	EXTRA M	AO		
Reset	value	X	Х	Х	Х	Х	Х	0	0		
Symbol	Function										
-	Not imp	lemented,	eserved for	or future u	se. ^a						
AO	Disable/I	Disable/Enable ALE									
	AO	Op	erating M	ode							
	0	ALI X2	E is emitte mode is u	ed at a cor sed)	istant rate	of 1/6 the	oscillator	frequency (or	r 1/3 if		
	1	1 ALE is active only during a MOVX or MOVC instruction									
EXTRAM	Internal/I	External R	AM (00H-	FFH) acce	ess using N	AOVX @	Ri/ @ DP	TR			
EXTRAM Operating Mode											
	0	Inte	Internal XRAM access using MOVX @ Ri/ @ DPTR								
	1	Ext	External data memory access								

 Table 5. Auxiliary Register AUXR

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.





Figure 5. Auto-Reload Mode Up/Down Counter (DCEN = 1)

6.4.2. Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 6) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.





Figure 7. PCA Timer/Counter

Table	8.	CMOD:	PCA	Counter	Mode	Register
abic	υ.	CITOD.	IUII	Counter	mout	Register

CMOD Address 0D9H		CI	DL	WDTE	-	-	-	CPS1	CPS0	ECF	
Reset value			()	0	Х	Х	Х	0	0	0
Symbol Function											
CIDL		Counter idle Mo	Counter Idle control: $CIDL = 0$ programs the PCA Counter to continue functioning during idle Mode. $CIDL = 1$ programs it to be gated off during idle.								
WDTE	C	Watchd WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.								
-		Not imp	Not implemented, reserved for future use. ^a								
CPS1		PCA Co	ount Puls	se Se	lect bit 1.						
CPS0		PCA Co	ount Puls	se Se	lect bit 0.						
		CPS1	CPS0	Sele	cted PCA	input. ^b					
		0	0	Inte	rnal clock	$f_{osc}/12$ (C	Dr f _{osc} /6 in	X2 Mode	e).		
		0	1	Inte	rnal clock	$f_{osc}/4$ (Or	f _{osc} /2 in	X2 Mode)			
		1	0	0 Timer 0 Overflow							
		1	1	Exte	ernal clock	at ECI/P1	.2 pin (ma	ax rate = f	osc/ 8)		
ECF		PCA Ei interrup	nable Co t. ECF =	unter = 0 di	Overflow sables that	interrupt: t function	ECF = 1 of CF.	enables Cl	F bit in C	CON to ge	enerate an

User software should not write 1s to reserved bits. These bits may be used in future 8051 family a. products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate. b. $f_{osc} = oscillator frequency$

The CMOD SFR includes three additional bits associated with the PCA (See Figure 7 and Table 8).

- The CIDL bit which allows the PCA to stop during idle mode. •
- The WDTE bit which enables or disables the watchdog function on module 4. •



The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

CCON Address 0D8H		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0		
	Rese	et value	0	0	X	0	0	0	0	0	
Syı	nbol	Function	l								
CF		PCA Count an interrup can only be	CA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags in interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.								
CR		PCA Count by software	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.								
-		Not implen	nented, res	erved for	future use	a					
CCF4		PCA Modu cleared by	ile 4 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be	
CCF3		PCA Modu cleared by	ile 3 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be	
CCF2		PCA Modu cleared by	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must cleared by software.						Must be		
CCF1		PCA Modu cleared by	ile 1 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captı	ire occurs.	Must be	
CCF0		PCA Modu cleared by	ile 0 inter software.	rupt flag.	Set by ha	rdware wh	en a matc	h or captu	ire occurs.	Must be	

 Table 9. CCON: PCA Counter Control Register

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The watchdog timer function is implemented in module 4 (See Figure 10).

The PCA interrupt system is shown in Figure 8



6.5.1. PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 9).



Figure 9. PCA Capture Mode



6.5.3. High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 11).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.



Figure 11. PCA High Speed Output Mode

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.



6.5.4. Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.



Figure 12. PCA PWM Mode

6.5.5. PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 10 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.



6.6.3. Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be 1111 1111b. For example:

SADDR	0101 0110b
SADEN	1111 1100b
Given	0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR <u>SADEN</u> Given	1111 0001b <u>1111 1010b</u> 1111 0X0Xb
Slave B:	SADDR <u>SADEN</u> Given	1111 0011b <u>1111 1001b</u> 1111 0XX1b
Slave C:	SADDR <u>SADEN</u> Given	1111 0010b <u>1111 1101b</u> 1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

6.6.4. Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

0101	0110b
1111	1100b
1111	111Xb
	0101 1111 1111

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR <u>SADEN</u> Broadcast	1111 0001b <u>1111 1010b</u> 1111 1X11b,
Slave B:	SADDR <u>SADEN</u> Broadcast	1111 0011b <u>1111 1001b</u> 1111 1X11B,
Slave C:	SADDR= <u>SADEN</u> Broadcast	1111 0010b <u>1111 1101b</u> 1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.



6.6.5. Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b Not bit addressable

SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b Not bit addressable



Table 17. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0	
SMOD1	SMOD) -	POF	GF1	GF0	PD	IDL	
Bit Number	Bit Mnemonic		Description					
7	SMOD1	Serial port Mode bi Set to select dou	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	Serial port Mode bi Clear to select S Set to to select F	erial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	Reserved The value read fr	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-Off Flag Clear to recogniz Set by hardware	Power-Off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	General purpose Fla Cleared by user for g	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	General purpose Fla Cleared by user for g	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	Power-Down mode Cleared by hardy Set to enter powe	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.						

Reset Value = 00X1 0000b Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.



6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

Table 26. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0	
SMOD1	SMOD	- POF GF1 GF0 PD					IDL	
Bit Number	Bit Mnemonic			Descrip	tion			
7	SMOD1	Serial port Mode bit Set to select dou	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	Serial port Mode bit Clear to select SI Set to to select F	erial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	Reserved The value read fr	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-Off Flag Clear to recogniz Set by hardware	Power-Off Flag Clear to recognize next reset type. Set by hardware when V _{CC} rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.						
2	GF0	General purpose Fla Cleared by user f Set by user for g	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	Power-Down mode I Cleared by hardw Set to enter powe	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardwar Set to enter idle r	e when interrupt on ode.	or reset occurs.				

Reset Value = 00X1 0000b Not bit addressable



7. TS83C51RB2/RC2/RD2 ROM

7.1. ROM Structure

The TS83C51RB2/RC2/RD2 ROM memory is divided in three different arrays:

•	the code array:	es.
•	the encryption array:	s.
•	the signature array:	es.

7.2. ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

7.2.1. 7.2.1. Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

7.2.2. Program Lock Bits

The lock bits when programmed according to Table 28. will provide different level of protection for the on-chip code and data.

	Program	Lock Bits		
Security level	LB1	LB2	LB3	Protection description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Р	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset.
3	U	Р	U	Same as level 1+ Verify disable. This security level is only available for 51RDX2 devices.

Table	28.	Program	Lock	bits
-------	-----	---------	------	------

U: unprogrammed

P: programmed

7.2.3. Signature bytes

The TS83C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

7.2.4. Verify Algorithm

Refer to 8.3.4.



9. Signature Bytes

The TS83/87C51RB2/RC2/RD2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 31. shows the content of the signature byte for the TS87C51RB2/RC2/RD2.

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel Wireless & Microcontrollers
31h	57h	Family Code: C51 X2
60h	7Ch	Product name: TS83C51RD2
60h	FCh	Product name: TS87C51RD2
60h	37h	Product name: TS83C51RC2
60h	B7h	Product name: TS87C51RC2
60h	3Bh	Product name: TS83C51RB2
60h	BBh	Product name: TS87C51RB2
61h	FFh	Product revision number

Table 31. Signature Bytes Content



10.3. DC Parameters for Standard Voltage

TA = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz. TA = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

Table 32. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage, ports 1, 2, 3, 4, 5 ⁽⁶⁾			0.3 0.45 1.0	V V V	$I_{OL} = 100 \ \mu A^{(4)}$ $I_{OL} = 1.6 \ m A^{(4)}$ $I_{OL} = 3.5 \ m A^{(4)}$
V _{OL1}	Output Low Voltage, port 0 ⁽⁶⁾			0.3 0.45 1.0	V V V	$I_{OL} = 200 \ \mu A^{(4)}$ $I_{OL} = 3.2 \ m A^{(4)}$ $I_{OL} = 7.0 \ m A^{(4)}$
V _{OL2}	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 100 \; \mu A^{(4)} \\ I_{OL} &= 1.6 \; m A^{(4)} \\ I_{OL} &= 3.5 \; m A^{(4)} \end{split}$
V _{OH}	Output High Voltage, ports 1, 2, 3, 4, 5	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$\begin{split} I_{OH} &= -10 \; \mu A \\ I_{OH} &= -30 \; \mu A \\ I_{OH} &= -60 \; \mu A \\ V_{CC} &= 5 \; V \pm 10\% \end{split}$
V _{OH1}	Output High Voltage, port 0	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
V _{OH2}	Output High Voltage, ALE, PSEN	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
R _{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	kΩ	
I _{IL}	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μΑ	Vin = 0.45 V
I _{LI}	Input Leakage Current			±10	μΑ	0.45 V < Vin < V _{CC}
I _{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μA	Vin = 2.0 V
C _{IO}	Capacitance of I/O Buffer			10	pF	$Fc = 1 MHz$ $TA = 25^{\circ}C$
I _{PD}	Power Down Current		20 ⁽⁵⁾	50	μΑ	$2.0 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}^{(3)}$
I _{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 V^{(1)}$



10.5.2. External Program Memory Characteristics

Table 36. Symbol Description	Table 3	36.	Symbol	Description
------------------------------	---------	-----	--------	-------------

Symbol	Parameter
Т	Oscillator clock period
T _{LHLL}	ALE pulse width
T _{AVLL}	Address Valid to ALE
T _{LLAX}	Address Hold After ALE
T _{LLIV}	ALE to Valid Instruction In
T _{LLPL}	ALE to PSEN
T _{PLPH}	PSEN Pulse Width
T _{PLIV}	PSEN to Valid Instruction In
T _{PXIX}	Input Instruction Hold After PSEN
T _{PXIZ}	Input Instruction FloatAfter PSEN
T _{PXAV}	PSEN to Address Valid
T _{AVIV}	Address to Valid Instruction In
T _{PLAZ}	PSEN Low to Address Float

Table 37. AC Parameters for Fix Clock

Speed	-1 40 N	М ЛНz	X2 1 30 N 60 MH	V node MHz z equiv.	standar 40 N	V rd mode MHz	X2 r 20 N 40 MH	L node MHz z equiv.	standar 30 N	L [.] d mode ⁄IHz	Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Т	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns



10.5.6. External Data Memory Read Cycle



Figure 27. External Data Memory Read Cycle

10.5.7. Serial Port Timing - Shift Register Mode

Table 42. Symbol Description

Symbol	Parameter
T _{XLXL}	Serial port clock cycle time
T _{QVHX}	Output data set-up to clock rising edge
T _{XHQX}	Output data hold after clock rising edge
T _{XHDX}	Input data hold after clock rising edge
T _{XHDV}	Clock rising edge to input data valid

Table 43. AC Parameters for a Fix Clock

Speed	-1 40 N	M MHz	- X2 n 30 N 60 MH	V node ⁄IHz z equiv.	standar 40 N	V •d mode ⁄IHz	X2 m 20 M 40 MH	L node ⁄IHz z equiv.	standar 30 N	L ·d mode ⁄IHz	Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{XLXL}	300		200		300		300		400		ns
T _{QVHX}	200		117		200		200		283		ns
T _{XHQX}	30		13		30		30		47		ns
T _{XHDX}	0		0		0		0		0		ns
T _{XHDV}		117		34		117		117		200	ns



10.5.11. External Clock Drive Characteristics (XTAL1)

Table	46.	AC	Parameters
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Symbol	Parameter	Min	Max	Units
T _{CLCL}	Oscillator Period	25		ns
T _{CHCX}	High Time	5		ns
T _{CLCX}	Low Time	5		ns
T _{CLCH}	Rise Time		5	ns
T _{CHCL}	Fall Time		5	ns
T _{CHCX} /T _{CLCX}	Cyclic ratio in X2 mode	40	60	%

10.5.12. External Clock Drive Waveforms



Figure 30. External Clock Drive Waveforms

10.5.13. AC Testing Input/Output Waveforms



Figure 31. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at V_{IH} min for a logic "1" and V_{IL} max for a logic "0".

10.5.14. Float Waveforms



Figure 32. Float Waveforms



11. Ordering Information



(*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for proto typing, not for volume production. Ceramic packages are available for OTP only.

Table	47.	Maximum	Clock	Frequency
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Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	60	40	