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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

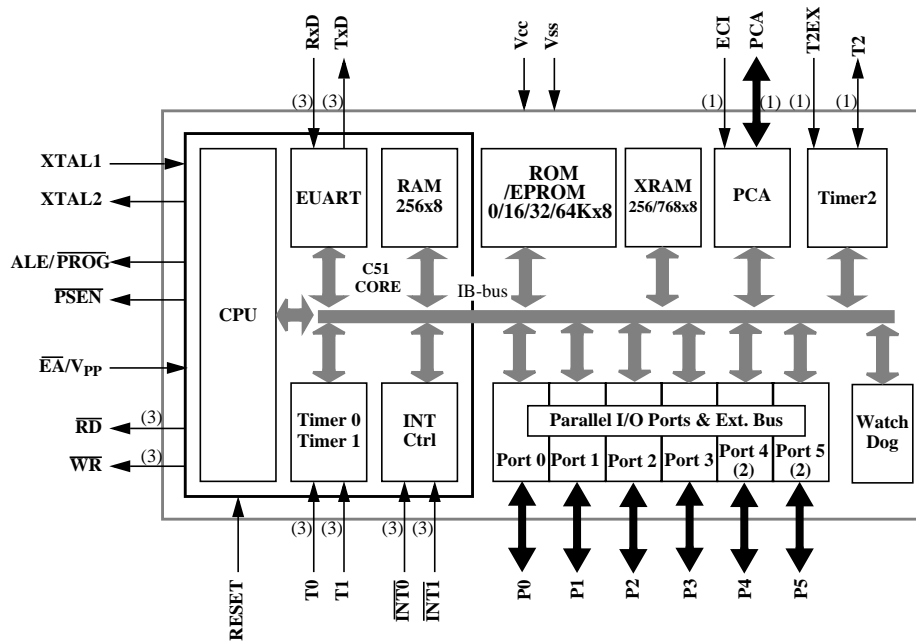
Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rd2-vcb

PDIL40 PLCC44 VQFP44 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RA2	0	0	256	512	32
TS80C51RD2	0	0	768	1024	32
TS83C51RB2	16k	0	256	512	32
TS83C51RC2	32k	0	256	512	32
TS83C51RD2	64k	0	768	1024	32
TS87C51RB2	0	16k	256	512	32
TS87C51RC2	0	32k	256	512	32
TS87C51RD2	0	64k	768	1024	32

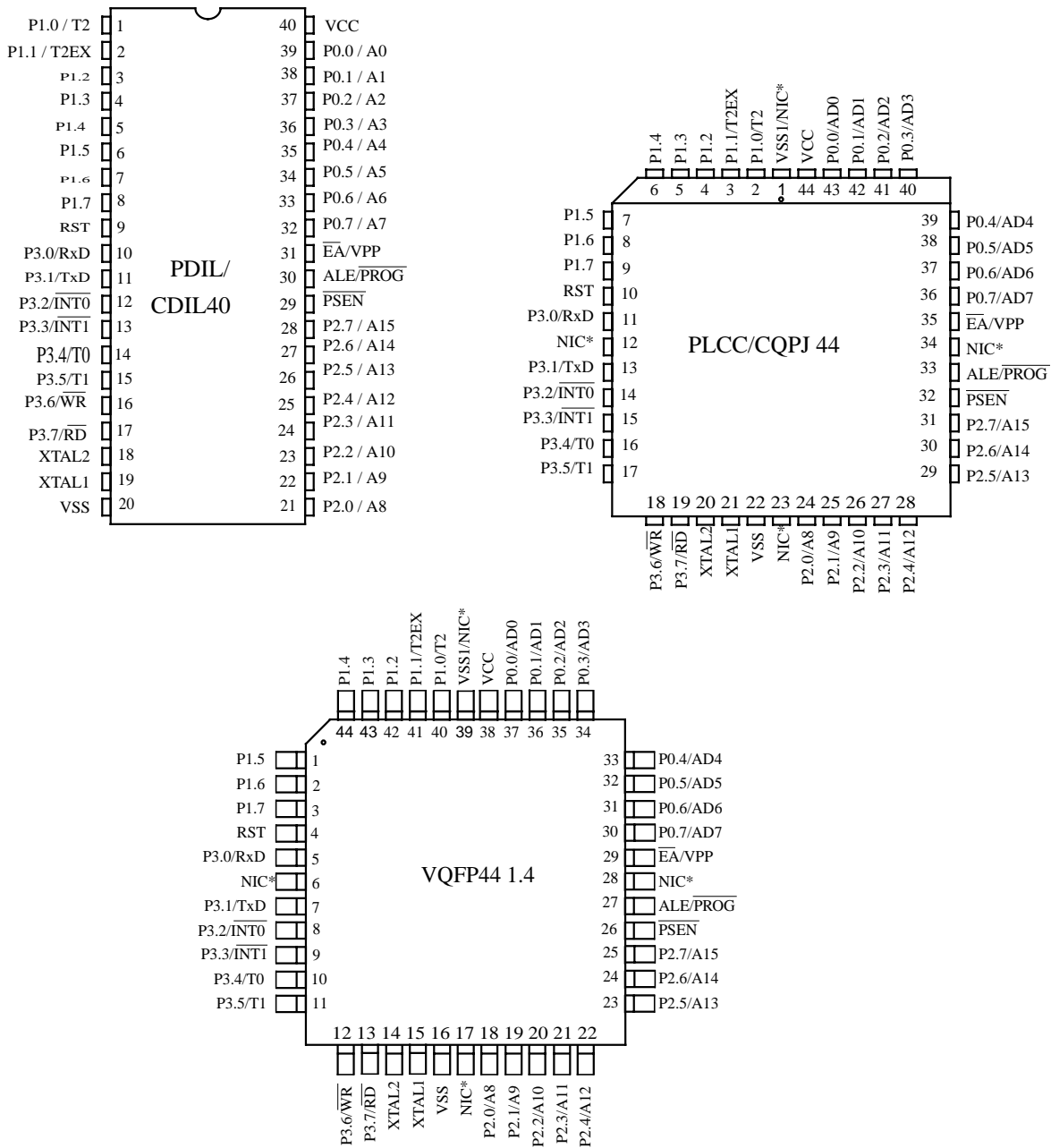
PLCC68 VQFP64 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RD2	0	0	768	1024	48
TS83C51RD2	64k	0	768	1024	48
TS87C51RD2	0	64k	768	1024	48

3. Block Diagram



- (1): Alternate function of Port 1
- (2): Only available on high pin count packages
- (3): Alternate function of Port 3

5. Pin Configuration



*NIC: No Internal Connection



TS80C51RA2/RD2
TS83C51RB2/RC2/RD2
TS87C51RB2/RC2/RD2

Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} . If the hardware watchdog reaches its time-out, the reset pin becomes an output during the time the internal reset is activated.
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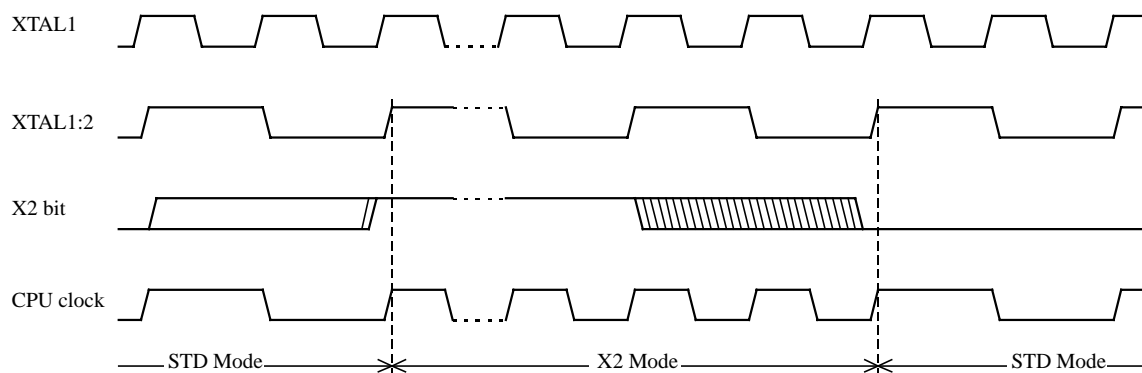


Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel-wm.com>)

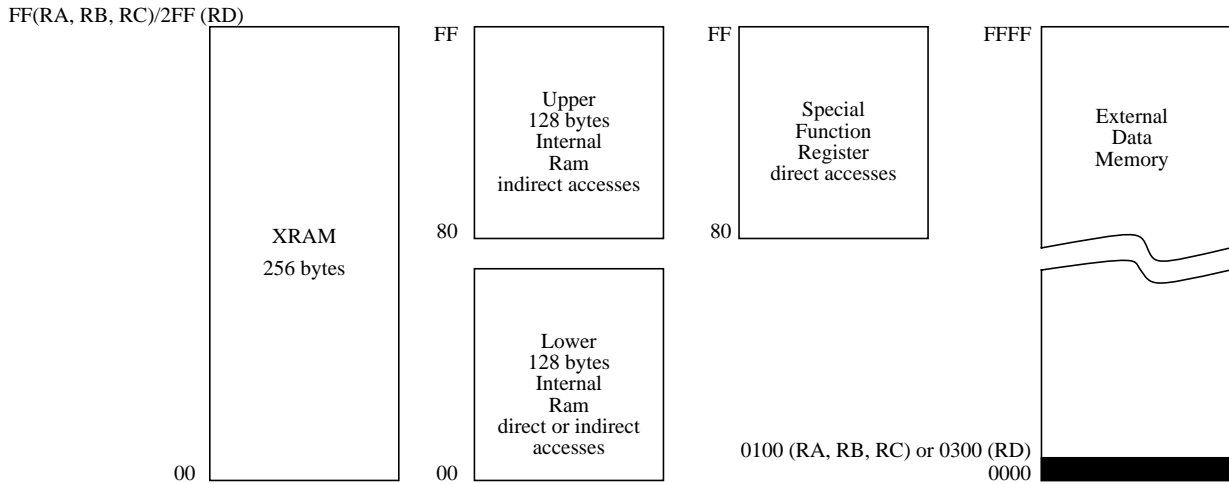


Figure 4. Internal and External Data Memory Address

Table 5. Auxiliary Register AUXR

AUXR Address 08EH	-	-	-	-	-	-	EXTRA M	AO
Reset value	X	X	X	X	X	X	0	0

Symbol	Function	
-	Not implemented, reserved for future use. ^a	
AO	Disable/Enable ALE	
	AO	Operating Mode
	0	ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used)
1	ALE is active only during a MOVX or MOVC instruction	
EXTRAM	Internal/External RAM (00H-FFH) access using MOVX @ Ri/ @ DPTR	
	EXTRAM	Operating Mode
	0	Internal XRAM access using MOVX @ Ri/ @ DPTR
1	External data memory access	

a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

6.5. Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/ capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency $\div 12$ ($\div 6$ in X2 mode)
- Oscillator frequency $\div 4$ ($\div 2$ in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 7). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 8) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)

Table 12. CCAPnH: PCA Modules Capture/Compare Registers High

CCAPnH Address n = 0 - 4	CCAP0H=0FAH CCAP1H=0FBH CCAP2H=0FCH CCAP3H=0FDH CCAP4H=0FEH		7	6	5	4	3	2	1	0
Reset value		0	0	0	0	0	0	0	0	0

Table 13. CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address n = 0 - 4	CCAP0L=0EAH CCAP1L=0EBH CCAP2L=0ECH CCAP3L=0EDH CCAP4L=0EEH		7	6	5	4	3	2	1	0
Reset value		0	0	0	0	0	0	0	0	0

Table 14. CH: PCA Counter High

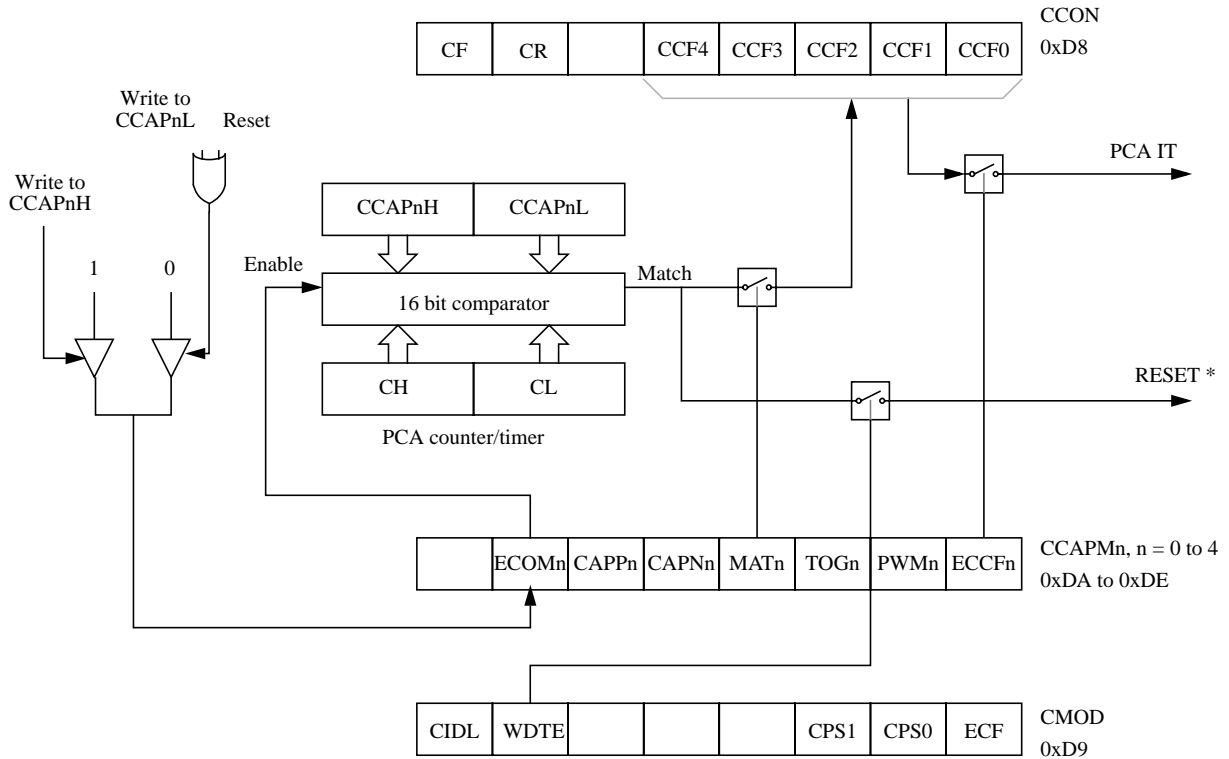
CH Address 0F9H		7	6	5	4	3	2	1	0
Reset value		0	0	0	0	0	0	0	0

Table 15. CL: PCA Counter Low

CL Address 0E9H		7	6	5	4	3	2	1	0
Reset value		0	0	0	0	0	0	0	0

6.5.2. 16-bit Software Timer / Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 10).



* Only for Module 4

Figure 10. PCA Compare Mode and PCA Watchdog Timer

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

6.6.5. Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

6.7. Interrupt System

The TS80C51Rx2 has a total of 7 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt and the PCA global interrupt. These interrupts are shown in Figure 16.

WARNING: Note that in the first version of RC devices, the PCA interrupt is in the lowest priority. Thus the order in $\overline{INT0}$, TF0, $\overline{INT1}$, TF1, RI or TI, TF2 or EXF2, PCA.

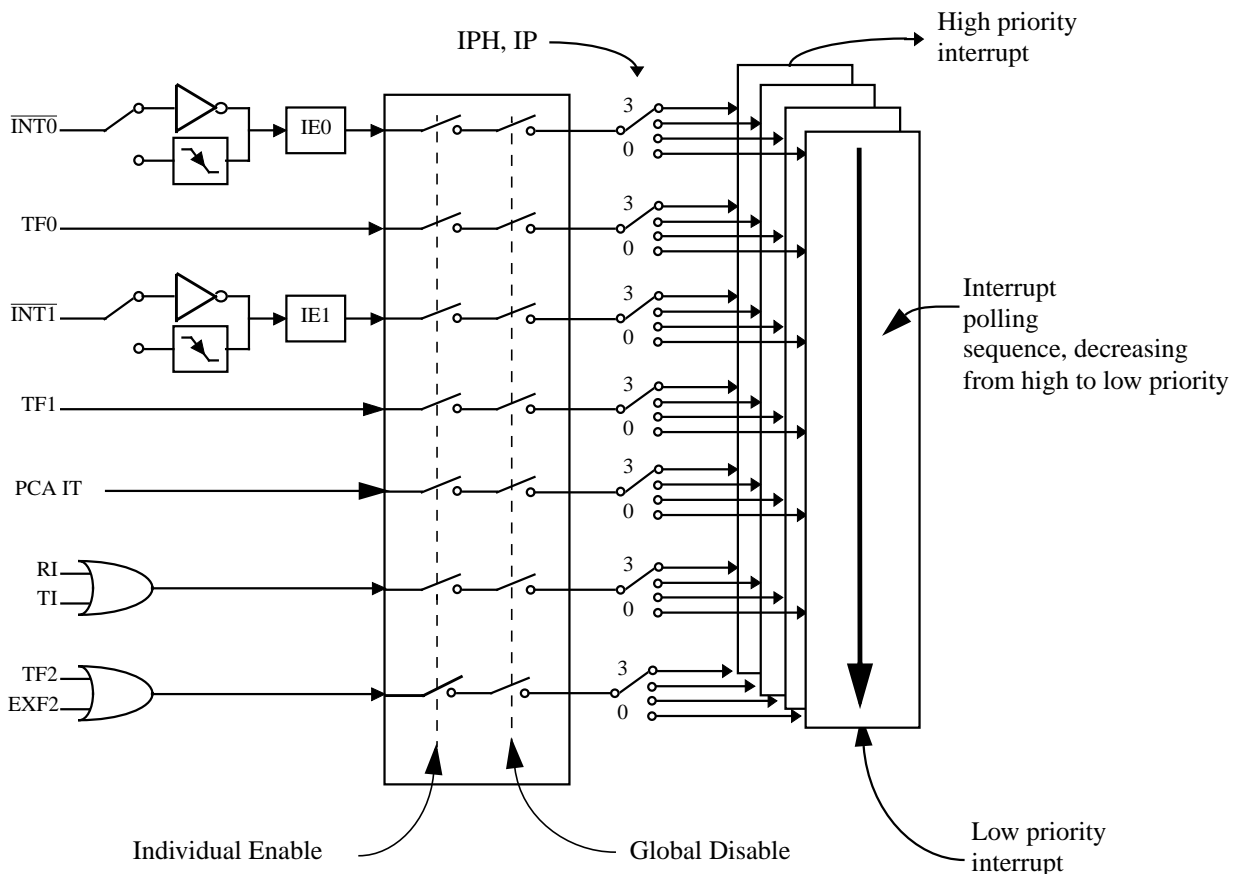


Figure 16. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 19.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 20.) and in the Interrupt Priority High register (See Table 21.). shows the bit values and priority levels associated with each combination.

The PCA interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.

Table 18. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 19. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	EC	PCA interrupt enable bit Clear to disable . Set to enable.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b

Bit addressable

Table 20. IP Register

IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	PPC	PCA interrupt priority bit Refer to PPCH for priority level.
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.
4	PS	Serial port Priority bit Refer to PSH for priority level.
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.

Reset Value = X000 0000b

Bit addressable

6.13. Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 27. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	EXTRAM bit See Table 5.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XX00b

Not bit addressable

8. TS87C51RB2/RC2/RD2 EPROM

8.1. EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

- the code array: 16/32/64 Kbytes.
- the encryption array: 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: 4 bytes.

8.2. EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

8.2.1. Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

8.2.2. Program Lock Bits

The three lock bits, when programmed according to Table 29.8.2.3. , will provide different level of protection for the on-chip code and data.

Table 29. Program Lock bits

Program Lock Bits				Protection description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed,
 P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

8.2.3. Signature bytes

The TS87C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

10. Electrical Characteristics

10.1. Absolute Maximum Ratings ⁽¹⁾

Ambiant Temperature Under Bias:

C = commercial	0°C to 70°C
I = industrial	-40°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V _{CC} to V _{SS}	-0.5 V to + 7 V
Voltage on V _{PP} to V _{SS}	-0.5 V to + 13 V
Voltage on Any Pin to V _{SS}	-0.5 V to V _{CC} + 0.5 V
Power Dissipation	1 W ⁽²⁾

NOTES

1. Stresses at or above those listed under “ Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

10.2. Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating I_{cc} measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That’s why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating I_{cc}:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = V_{cc}, RST = V_{ss}, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating I_{cc}.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			3 + 0.6 Freq (MHz) @ 12MHz 10.2 @ 16MHz 12.6	mA	$V_{CC} = 5.5 \text{ V}^{(8)}$
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.25+0.3 Freq (MHz) @ 12MHz 3.9 @ 16MHz 5.1	mA	$V_{CC} = 5.5 \text{ V}^{(2)}$

10.4. DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{SS} = 0 \text{ V}$; $V_{CC} = 2.7 \text{ V}$ to $5.5 \text{ V} \pm 10\%$; $F = 0$ to 30 MHz .

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{SS} = 0 \text{ V}$; $V_{CC} = 2.7 \text{ V}$ to $5.5 \text{ V} \pm 10\%$; $F = 0$ to 30 MHz .

Table 33. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IHI}	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3, 4, 5 ⁽⁶⁾			0.45	V	$I_{OL} = 0.8 \text{ mA}^{(4)}$
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ ⁽⁶⁾			0.45	V	$I_{OL} = 1.6 \text{ mA}^{(4)}$
V_{OH}	Output High Voltage, ports 1, 2, 3, 4, 5	$0.9 V_{CC}$			V	$I_{OH} = -10 \mu\text{A}$
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40 \mu\text{A}$
I_{IL}	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μA	$V_{in} = 0.45 \text{ V}$
I_{LI}	Input Leakage Current			± 10	μA	$0.45 \text{ V} < V_{in} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μA	$V_{in} = 2.0 \text{ V}$
R_{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	k Ω	
CIO	Capacitance of I/O Buffer			10	pF	$F_c = 1 \text{ MHz}$ $T_A = 25^\circ\text{C}$
I_{PD}	Power Down Current		20 ⁽⁵⁾ 10 ⁽⁵⁾	50 30	μA	$V_{CC} = 2.0 \text{ V}$ to $5.5 \text{ V}^{(3)}$ $V_{CC} = 2.0 \text{ V}$ to $3.3 \text{ V}^{(3)}$
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.2 Freq (MHz) @ 12MHz 3.4 @ 16MHz 4.2	mA	$V_{CC} = 3.3 \text{ V}^{(1)}$
I_{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.3 Freq (MHz) @ 12MHz 4.6 @ 16MHz 5.8	mA	$V_{CC} = 3.3 \text{ V}^{(8)}$

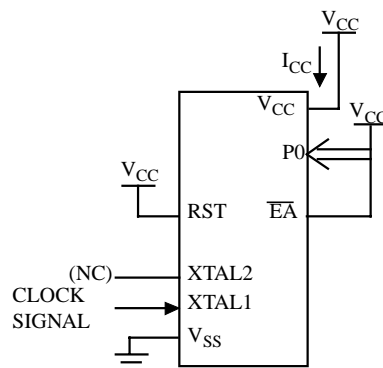
TS80C51RA2/RD2
TS83C51RB2/RC2/RD2
TS87C51RB2/RC2/RD2



Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @ 12MHz 2 @ 16MHz 2.6	mA	$V_{CC} = 3.3 \text{ V}^{(2)}$

NOTES

- I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$ (see Figure 24.), $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; $\overline{EA} = RST = \text{Port } 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator is used.
- Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; Port 0 = V_{CC} ; $\overline{EA} = RST = V_{SS}$ (see Figure 22.).
- Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$, PORT 0 = V_{CC} ; XTAL2 N.C.; RST = V_{SS} (see Figure 23.).
- Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.
- Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
 Maximum I_{OL} per port pin: 10 mA
 Maximum I_{OL} per 8-bit port:
 Port 0: 26 mA
 Ports 1, 2, 3 and 4 and 5 when available: 15 mA
 Maximum total I_{OL} for all output pins: 71 mA
 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$ (see Figure 24.), $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; $\overline{EA} = \text{Port } 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I_{CC} Test Condition, under reset

10.5.2. External Program Memory Characteristics

Table 36. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T _{LHLL}	ALE pulse width
T _{AVLL}	Address Valid to ALE
T _{LLAX}	Address Hold After ALE
T _{LLIV}	ALE to Valid Instruction In
T _{LLPL}	ALE to PSEN
T _{PLPH}	PSEN Pulse Width
T _{PLIV}	PSEN to Valid Instruction In
T _{PXIX}	Input Instruction Hold After PSEN
T _{PXIZ}	Input Instruction Float After PSEN
T _{PXAV}	PSEN to Address Valid
T _{AVIV}	Address to Valid Instruction In
T _{PLAZ}	PSEN Low to Address Float

Table 37. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Symbol											
T	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

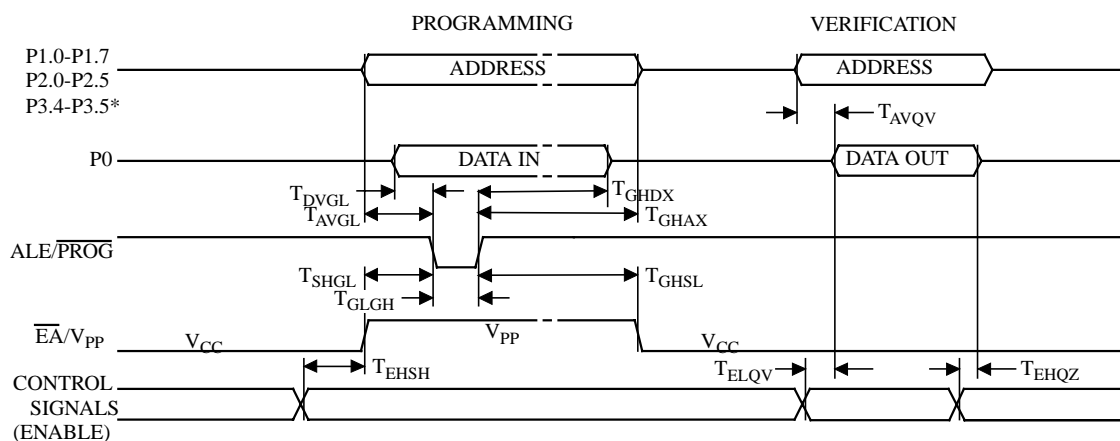
10.5.9. EPROM Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$ to 27°C ; $V_{SS} = 0\text{V}$; $V_{CC} = 5\text{V} \pm 10\%$ while programming. V_{CC} = operating range while verifying

Table 45. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frquency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHAX}	Adress Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHDX}	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{EHS}	(Enable) High to V_{PP}	$48 T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
T_{GHSL}	V_{PP} Hold after $\overline{\text{PROG}}$	10		μs
T_{GLGH}	$\overline{\text{PROG}}$ Width	90	110	μs
T_{AVQV}	Address to Valid Data		$48 T_{CLCL}$	
T_{ELQV}	ENABLE Low to Data Valid		$48 T_{CLCL}$	
T_{EHQZ}	Data Float after ENABLE	0	$48 T_{CLCL}$	

10.5.10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Figure 29. EPROM Programming and Verification Waveforms