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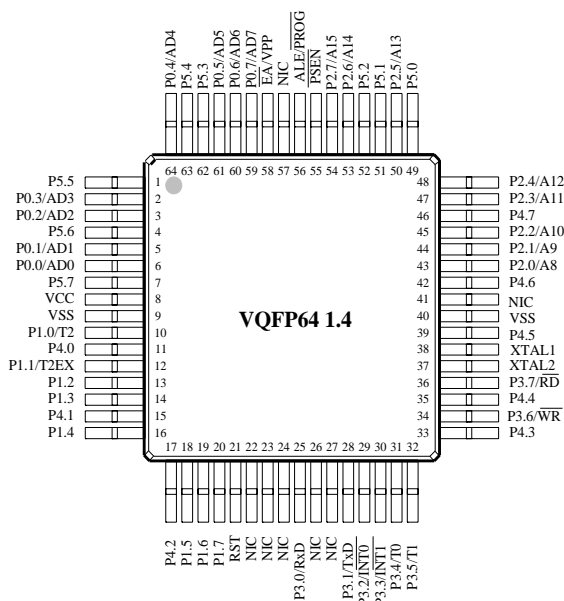
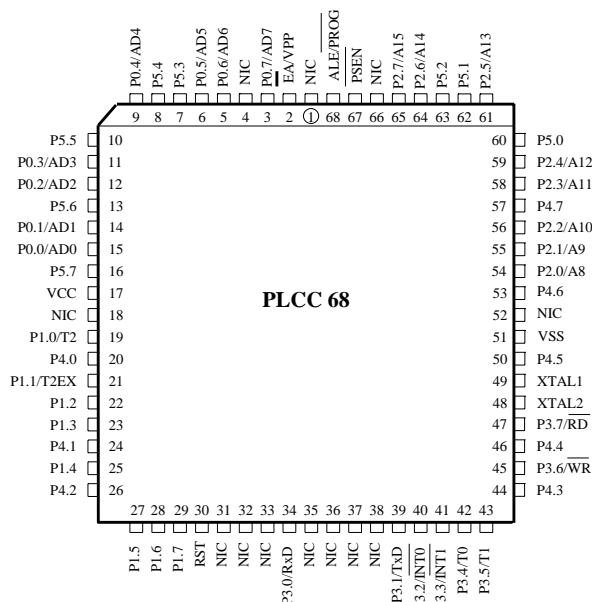
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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/30MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c51rd2-vie



NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name And Function
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
$\overline{\text{PSEN}}$	29	32	26	O	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/\text{V}_{\text{PP}}$	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC). $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier

6. TS80C51Rx2 Enhanced Features

In comparison to the original 80C52, the TS80C51Rx2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The extended RAM.
- The Programmable Counter Array (PCA).
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

6.1. X2 Feature

The TS80C51Rx2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

6.1.1. Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.

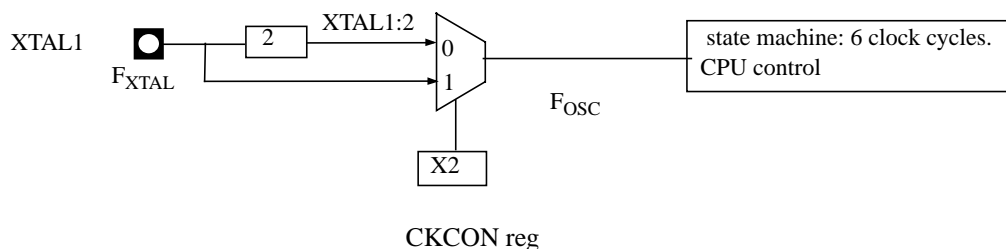


Figure 1. Clock Generation Diagram

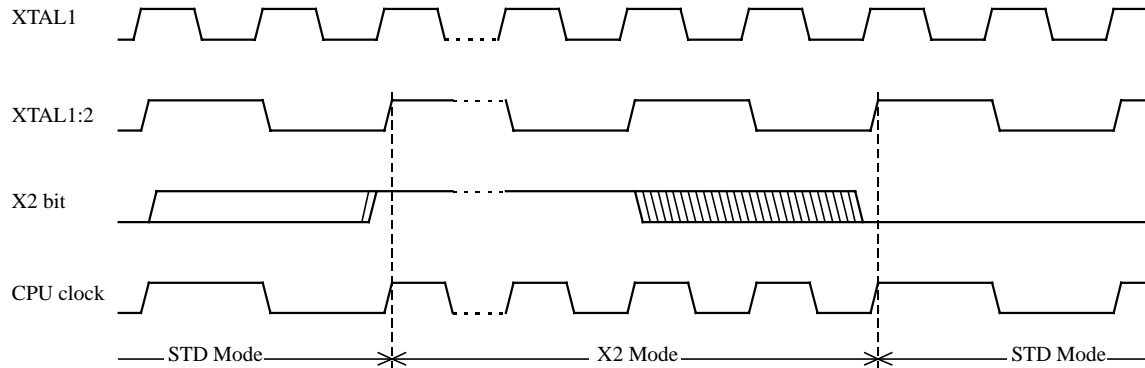


Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

6.2. Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 4.) that allows the program code to switch between them (Refer to Figure 3).

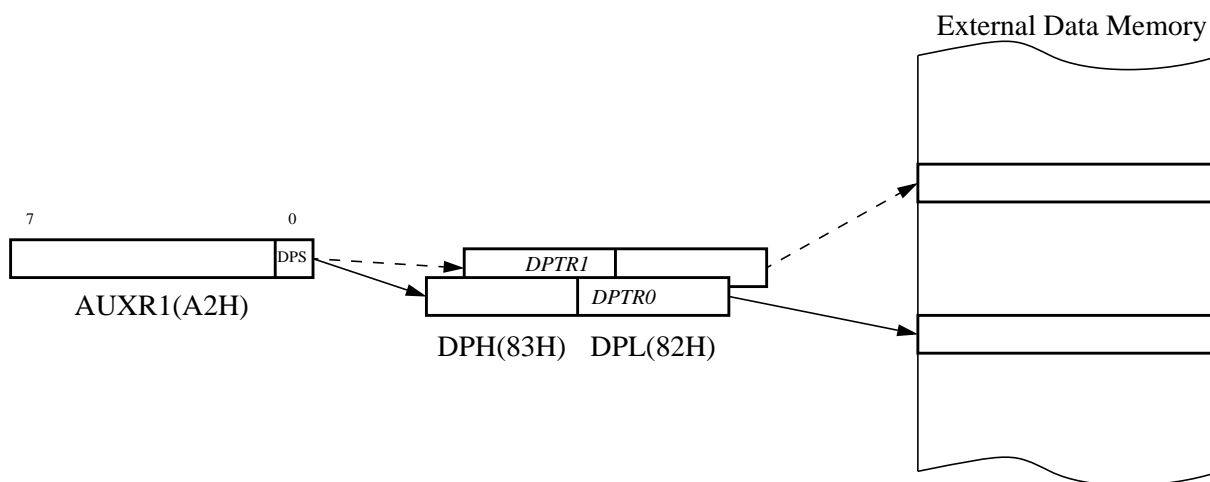


Figure 3. Use of Dual Pointer

Table 4. AUXR1: Auxiliary Register 1

AUXR1 Address 0A2H		-	-	-	-	GF3	-	-	DPS
	Reset value	X	X	X	X	0	X	X	0

Symbol	Function
-	Not implemented, reserved for future use. ^a
DPS	Data Pointer Selection.
	DPS Operating Mode
	0 DPTR0 Selected
	1 DPTR1 Selected
GF3	This bit is a general purpose user flag ^b .

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
- b. GF3 will not be available on first version of the RC devices.

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2          AUXR1 EQU 0A2H
;
0000 909000   MOV DPTR,#SOURCE      ; address of SOURCE
0003 05A2     INC  AUXR1             ; switch data pointers
0005 90A000   MOV DPTR,#DEST        ; address of DEST
0008          LOOP:
0008 05A2     INC  AUXR1             ; switch data pointers
000A E0       MOVX A,@DPTR           ; get a byte from SOURCE
000B A3       INC  DPTR              ; increment SOURCE address
000C 05A2     INC  AUXR1             ; switch data pointers
000E F0       MOVX @DPTR,A           ; write the byte to DEST
000F A3       INC  DPTR              ; increment DEST address
0010 70F6     JNZ  LOOP              ; check for 0 terminator
0012 05A2     INC  AUXR1             ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

6.3. Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of random access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 5.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data** ,accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect ports P0, P2, P3.6 (\overline{WR}) and P3.7 (\overline{RD}).** **For example, with EXTRAM = 0, MOVX @R0, # data** where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure . For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight address bits (DPL) with data. MOVX @ Ri and MOVX @DPTR will generate either read or write signals on P3.6 (\overline{WR}) and P3.7 (\overline{RD}).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the XRAM.

The **CCON SFR** contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 9).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Table 9. CCON: PCA Counter Control Register

CCON Address 0D8H		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
Reset value		0	0	X	0	0	0	0	0
Symbol	Function								
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.								
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.								
-	Not implemented, reserved for future use. ^a								
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								

- a. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The **watchdog timer** function is implemented in module 4 (See Figure 10).

The **PCA interrupt** system is shown in Figure 8

6.5.1. PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 9).

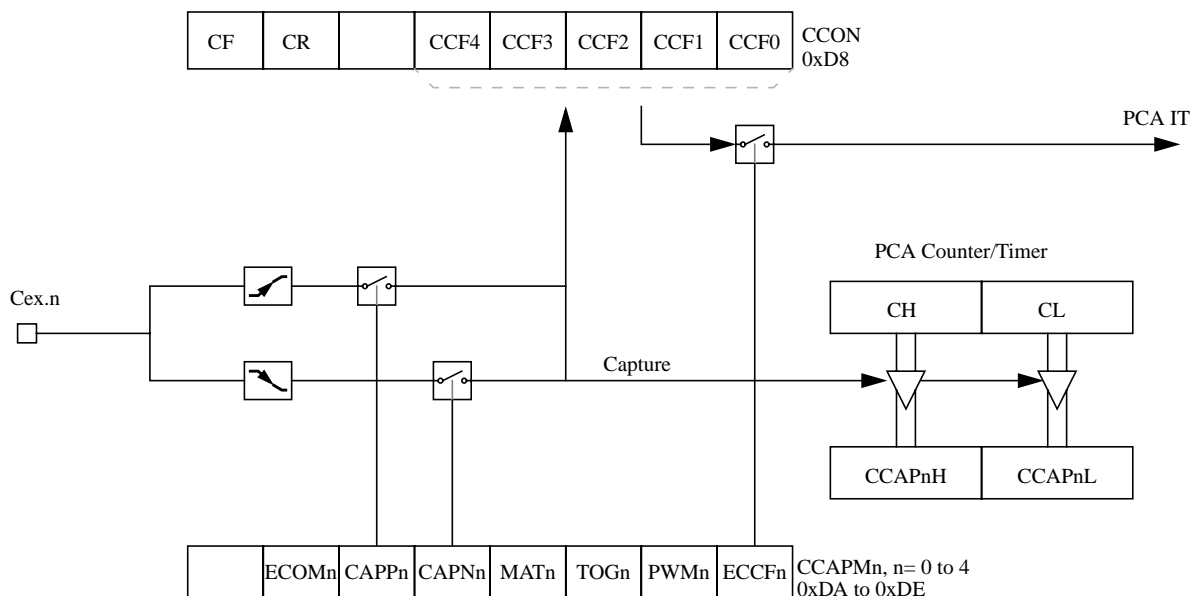


Figure 9. PCA Capture Mode

6.6.3. Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed. To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

SADDR	0101 0110b
<u>SADEN</u>	<u>1111 1100b</u>
Given	0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Given	1111 0X0Xb

Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Given	1111 0XX1b

Slave C:	SADDR	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Given	1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

6.6.4. Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

	SADDR	0101 0110b
	SADEN	1111 1100b
Broadcast = SADDR OR SADEN		1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Broadcast	1111 1X11b,

Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Broadcast	1111 1X11B,

Slave C:	SADDR=	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Broadcast	1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

6.6.5. Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

Table 16. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit Number	Bit Mnemonic	Description																									
7	FE	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit																									
	SM0	Serial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit																									
6	SM1	Serial port Mode bit 1 <table><tr><th>SM0</th><th>SM1</th><th>Mode</th><th>Description</th><th>Baud Rate</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Shift Register</td><td>F_{XTAL}/12 (/6 in X2 mode)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8-bit UART</td><td>Variable</td></tr><tr><td>1</td><td>0</td><td>2</td><td>9-bit UART</td><td>F_{XTAL}/64 or F_{XTAL}/32 (/32, /16 in X2 mode)</td></tr><tr><td>1</td><td>1</td><td>3</td><td>9-bit UART</td><td>Variable</td></tr></table>	SM0	SM1	Mode	Description	Baud Rate	0	0	0	Shift Register	F _{XTAL} /12 (/6 in X2 mode)	0	1	1	8-bit UART	Variable	1	0	2	9-bit UART	F _{XTAL} /64 or F _{XTAL} /32 (/32, /16 in X2 mode)	1	1	3	9-bit UART	Variable
SM0	SM1	Mode	Description	Baud Rate																							
0	0	0	Shift Register	F _{XTAL} /12 (/6 in X2 mode)																							
0	1	1	8-bit UART	Variable																							
1	0	2	9-bit UART	F _{XTAL} /64 or F _{XTAL} /32 (/32, /16 in X2 mode)																							
1	1	3	9-bit UART	Variable																							
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																									
4	REN	Reception Enable bit Clear to disable serial reception. Set to enable serial reception.																									
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																									
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																									
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																									
0	RI	Receive Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 14. and Figure 15. in the other modes.																									

Reset Value = 0000 0000b

Bit addressable

6.12. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 26.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a V_{CC} range from 4.5V to 5.5V. For lower V_{CC} value, reading POF bit will return indeterminate value.

Table 26. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

7. TS83C51RB2/RC2/RD2 ROM

7.1. ROM Structure

The TS83C51RB2/RC2/RD2 ROM memory is divided in three different arrays:

- the code array: 16/32/64 Kbytes.
- the encryption array: 64 bytes.
- the signature array: 4 bytes.

7.2. ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

7.2.1. 7.2.1. Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

7.2.2. Program Lock Bits

The lock bits when programmed according to Table 28. will provide different level of protection for the on-chip code and data.

Table 28. Program Lock bits

Program Lock Bits				Protection description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset.
3	U	P	U	Same as level 1+ Verify disable. This security level is only available for 51RDX2 devices.

U: unprogrammed

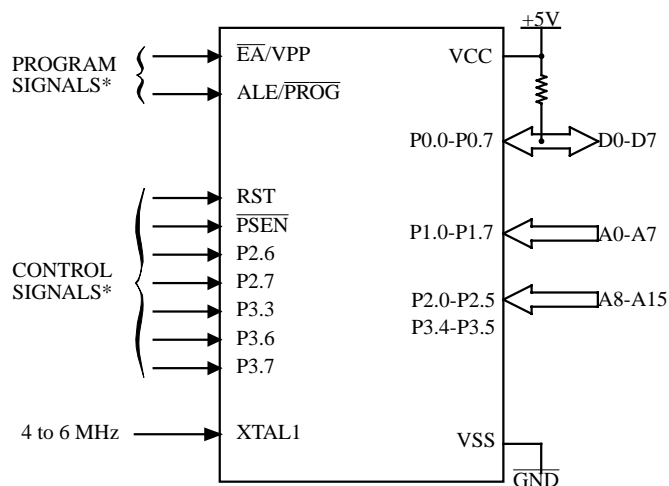
P: programmed

7.2.3. Signature bytes

The TS83C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.

7.2.4. Verify Algorithm

Refer to 8.3.4.



* See Table 31. for proper value on these inputs

Figure 18. Set-Up Modes Configuration

8.3.3. Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51RB2/RC2/RD2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise \overline{EA}/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/\overline{PROG} once.
- Step 6: Lower \overline{EA}/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 19.).

8.3.4. Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51RB2/RC2/RD2.

P 2.7 is used to enable data output.

To verify the TS87C51RB2/RC2/RD2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 19.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

TS80C51RA2/RD2

TS83C51RB2/RC2/RD2

TS87C51RB2/RC2/RD2



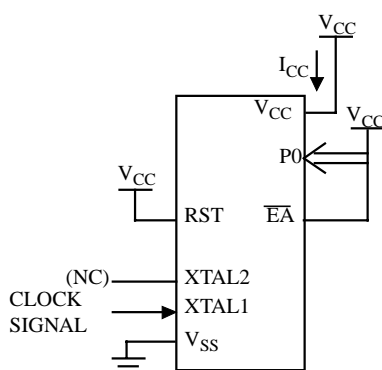
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @ 12MHz 2 @ 16MHz 2.6	mA	$V_{CC} = 3.3 \text{ V}^{(2)}$

NOTES

- I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$ (see Figure 24.), $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; $\overline{EA} = RST = \text{Port } 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator is used.
- Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; Port 0 = V_{CC} ; $\overline{EA} = RST = V_{SS}$ (see Figure 22.).
- Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$; PORT 0 = V_{CC} ; XTAL2 N.C.; RST = V_{SS} (see Figure 23.).
- Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.
- Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2, 3 and 4 and 5 when available: 15 mA
Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$ (see Figure 24.), $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; $\overline{EA} = \text{Port } 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 20. I_{CC} Test Condition, under reset

Table 40. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{RLRH}	130		85		135		125		175		ns
T _{WLWH}	130		85		135		125		175		ns
T _{RLDV}		100		60		102		95		137	ns
T _{RHDX}	0		0		0		0		0		ns
T _{RHDZ}		30		18		35		25		42	ns
T _{LLDV}		160		98		165		155		222	ns
T _{AVDV}		165		100		175		160		235	ns
T _{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T _{AVWL}	75		47		80		70		103		ns
T _{QVWX}	10		7		15		5		13		ns
T _{QVWH}	160		107		165		155		213		ns
T _{WHQX}	15		9		17		10		18		ns
T _{RLAZ}		0		0		0		0		0	ns
T _{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Table 44. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{XLXL}	Min	12 T	6 T				ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T_{XHDx}	Min	x	x	0	0	0	ns
T_{XHDV}	Max	10 T - x	5 T - x	133	133	133	ns

10.5.8. Shift Register Timing Waveforms

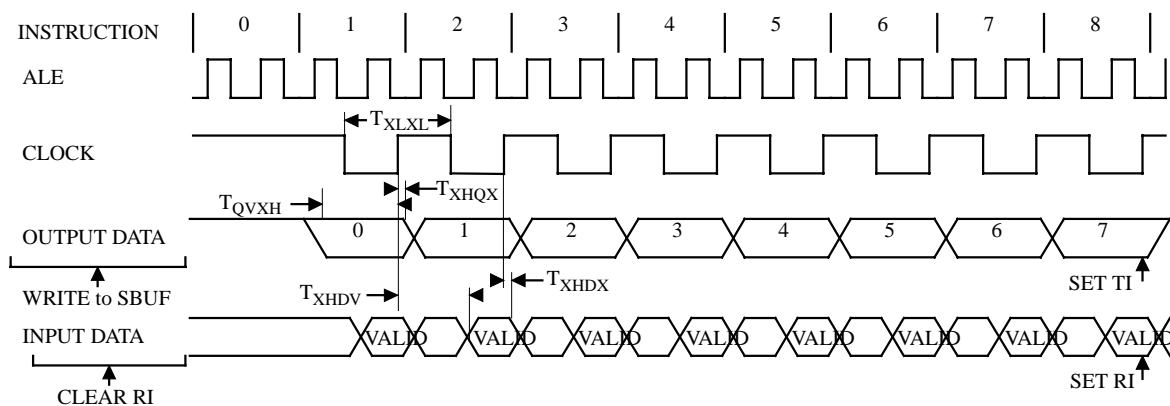


Figure 28. Shift Register Timing Waveforms

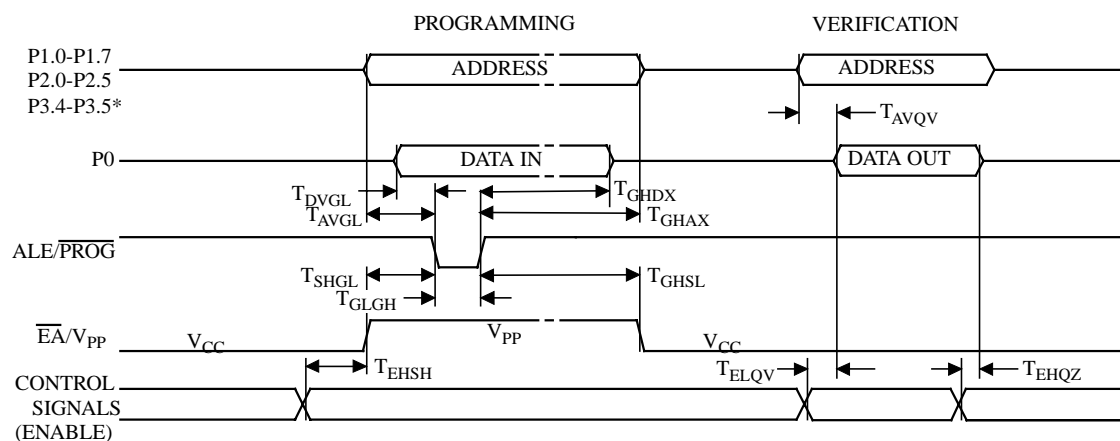
10.5.9. EPROM Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$ to 27°C ; $V_{SS} = 0\text{V}$; $V_{CC} = 5\text{V} \pm 10\%$ while programming. V_{CC} = operating range while verifying

Table 45. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHAX}	Adress Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHDX}	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{EHS}	(Enable) High to V_{PP}	$48 T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
T_{GHSL}	V_{PP} Hold after $\overline{\text{PROG}}$	10		μs
T_{GLGH}	$\overline{\text{PROG}}$ Width	90	110	μs
T_{AVQV}	Address to Valid Data		$48 T_{CLCL}$	
T_{ELQV}	ENABLE Low to Data Valid		$48 T_{CLCL}$	
T_{EHQZ}	Data Float after ENABLE	0	$48 T_{CLCL}$	

10.5.10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Figure 29. EPROM Programming and Verification Waveforms

11. Ordering Information

TS	87C51RD2	-M	C	B	R
	-M: VCC: 5V +/- 10% 40 MHz, X1 mode 20 MHz, X2 mode -V: VCC: 5V +/- 10% 40 MHz, X1 mode 30 MHz, X2 mode -L: VCC: 2.7 to 5.5 V 30 MHz, X1 mode 20 MHz, X2 mode -E: Samples		Packages: A: PDIL 40 B: PLCC 44 E: VQFP 44 (1.4mm) J: Window CDIL 40* K: Window CQPJ 44* L: PLCC68 (RD devices only)* M: VQFP64, square package, 1.4mm (RD devices only)* N: JLCC68 (RD devices only)*		Conditioning R: Tape & Reel D: Dry Pack B: Tape & Reel and Dry Pack
Part Number 80C51RA2 (ROMless, 256 bytes XRAM) 80C51RD2 (ROMless, 768bytes XRAM) 83C51RB2zzz (16k ROM, zzz is the customer code) 83C51RC2zzz (32k ROM, zzz is the customer code) 83C51RD2zzz (64k ROM, zzz is the customer code) 87C51RB2 (16k OTP EPROM) 87C51RC2 (32k OTP EPROM) 87C51RD2 (64k OTP EPROM)					
Temperature Range C: Commercial 0 to 70°C I: Industrial -40 to 85°C					

(*) Check with Atmel Wireless & Microcontrollers Sales Office for availability. Ceramic packages (J, K, N) are available for proto typing, not for volume production. Ceramic packages are available for OTP only.

Table 47. Maximum Clock Frequency

Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	60	40	