Renesas Electronics America Inc - R7FS5D57C3A01CFB#AA0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	109
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs5d57c3a01cfb-aa0

1. Overview

The MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 120 MHz with the following features:

- Up to 1-MB code flash memory
- 384-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC), USBFS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- 12-Bit A/D Converter (ADC12)
- 12-Bit D/A Converter (DAC12)
- Analog peripherals.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 120 MHz • ARM Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions. • SysTick timer: - Driven by LOCO clock.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 1 MB of code flash memory. See section 53, Flash Memory in User's Manual.
Data flash memory	32 KB of data flash memory. See section 53, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory.
SRAM	On-chip high-speed SRAM providing either parity-bit or Error Correction Code (ECC). The first 32 KB of SRAM0 is subject to ECC. Parity check is performed for other areas. See section 51, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 52, Standby SRAM in User's Manual.

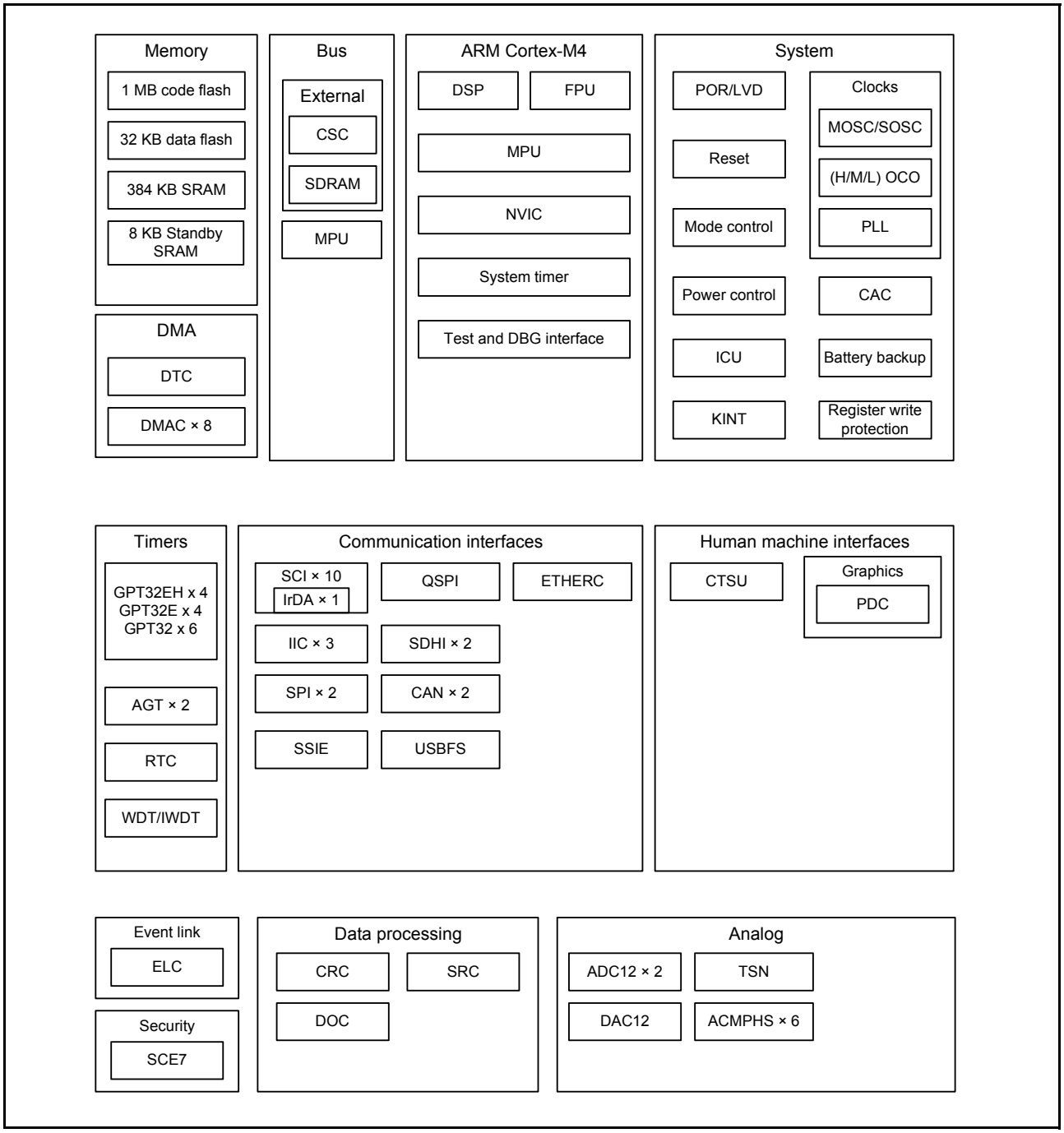


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows how to read the product part number information, including memory capacity, and package type. Table 1.14 shows a list of products.

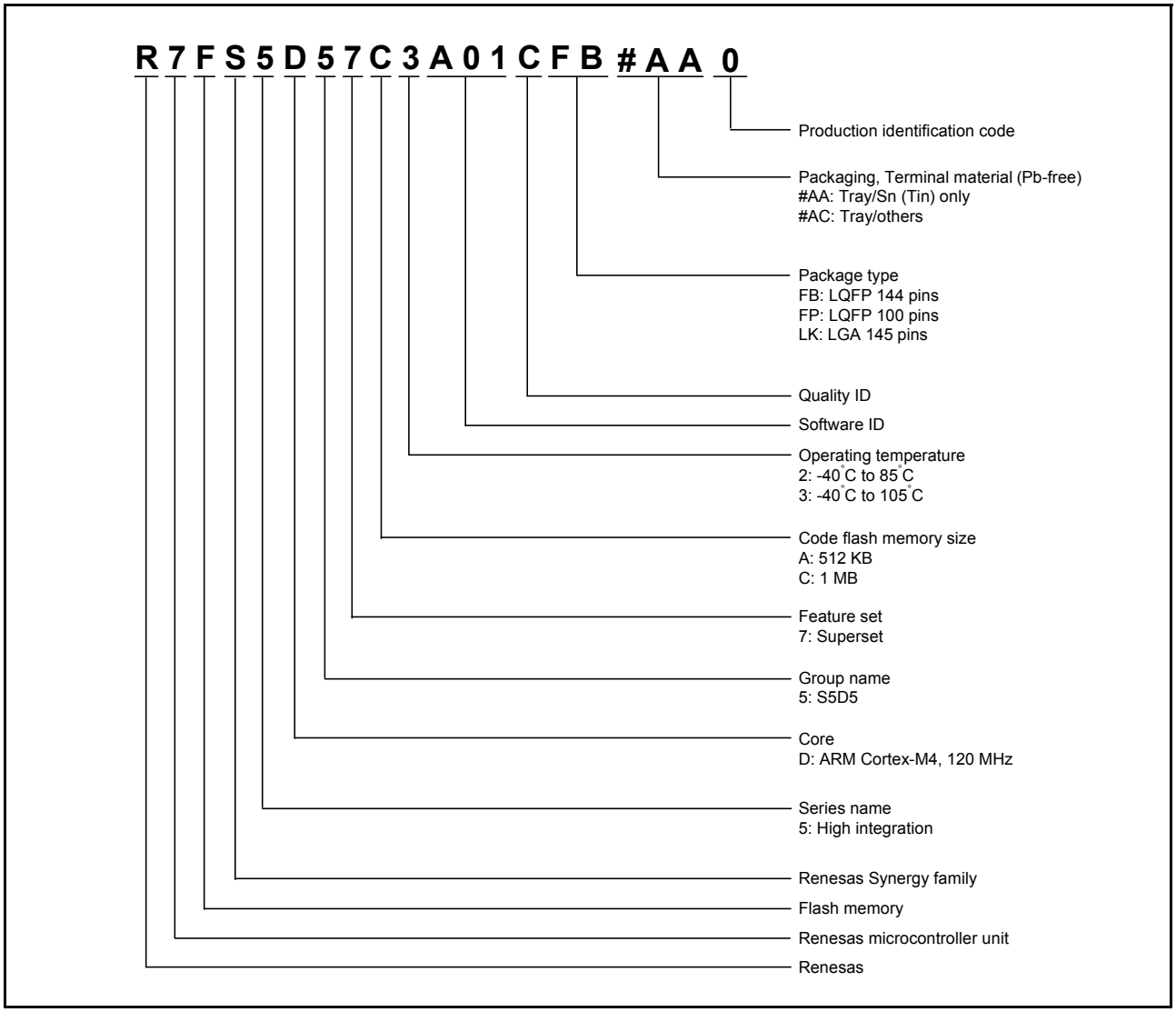


Figure 1.2 Part numbering scheme

Table 1.14 Product list

Product part number	Orderable part number	Package	Code flash	Data flash	SRAM	Operating temperature
R7FS5D57C2A01CLK	R7FS5D57C2A01CLK#AC0	PTLG0145KA-A	1 MB	32 KB	384 KB	-40 to +85°C
R7FS5D57C3A01CFB	R7FS5D57C3A01CFB#AA0	PLQP0144KA-B				-40 to +105°C
R7FS5D57C3A01CFP	R7FS5D57C3A01CFP#AA0	PLQP0100KB-B				-40 to +105°C
R7FS5D57A2A01CLK	R7FS5D57A2A01CLK#AC0	PTLG0145KA-A	512 KB			-40 to +85°C
R7FS5D57A3A01CFB	R7FS5D57A3A01CFB#AA0	PLQP0144KA-B				-40 to +105°C
R7FS5D57A3A01CFP	R7FS5D57A3A01CFP#AA0	PLQP0100KB-B				-40 to +105°C

1.4 Function Comparison

Table 1.15 Functional comparison

Function		Part numbers		
		R7FS5D57C2A01CLK/ R7FS5D57A2A01CLK	R7FS5D57C3A01CFB/ R7FS5D57A3A01CFB	R7FS5D57C3A01CFP/ R7FS5D57A3A01CFP
Pin count		145	144	100
Package		LGA	LQFP	LQFP
Code flash memory		1 MB/512 KB		
Data flash memory		32 KB		
SRAM		384 KB		
	Parity	352 KB		
	ECC	32 KB		
Standby SRAM		8 KB		
System	CPU clock	120 MHz		
	Backup registers	512 B		
	ICU	Yes		
	KINT	8		
Event link	ELC	Yes		
DMA	DTC	Yes		
	DMAC	8		
BUS	External bus	16-bit bus		8-bit bus
	SDRAM	Yes		No
Timers	GPT32EH	4	4	4
	GPT32E	4	4	4
	GPT32	6	6	5
	AGT	2	2	2
	RTC	Yes		
	WDT/IWDT	Yes		
Communication	SCI	10		
	IIC	3		2
	SPI	2		
	SSIE	1		
	QSPI	1		
	SDHI	2		
	CAN	2		
	USBFS	Yes		
	ETHERC	1		
Analog	ADC12	22		19
	DAC12	2		
	ACMPHS	6		
	TSN	Yes		
HMI	CTSU	18		12
Graphics	PDC	Yes		
Data processing	CRC	Yes		
	DOC	Yes		
	SRC	Yes		
Security		SCE7		

Table 1.16 Pin functions (2 of 5)

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM clock enable signal
	SDCS	Output	SDRAM chip select signal, active-low
	RAS	Output	SDRAM low address strobe signal, active-low
	CAS	Output	SDRAM column address strobe signal, active-low
	WE	Output	SDRAM write enable signal, active-low
	DQM0	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00
	DQM1	Output	SDRAM I/O data mask enable signal for DQ15 to DQ08
	A00 to A15	Output	Address bus
	DQ00 to DQ15	I/O	Data bus
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
SCI	SCK0 to SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0 to RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0 to TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0 to CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0 to SCL9	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDA0 to SDA9	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCK0 to SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0 to MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0 to MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS0 to SS9	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCL0 to SCL2	I/O	Input/output pins for the clock
	SDA0 to SDA2	I/O	Input/output pins for data
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins
	SSITXD0	Output	Serial data output pins
	SSIRXD0	Input	Serial data input pins
	SSIDATA0	I/O	Serial data input/output pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)

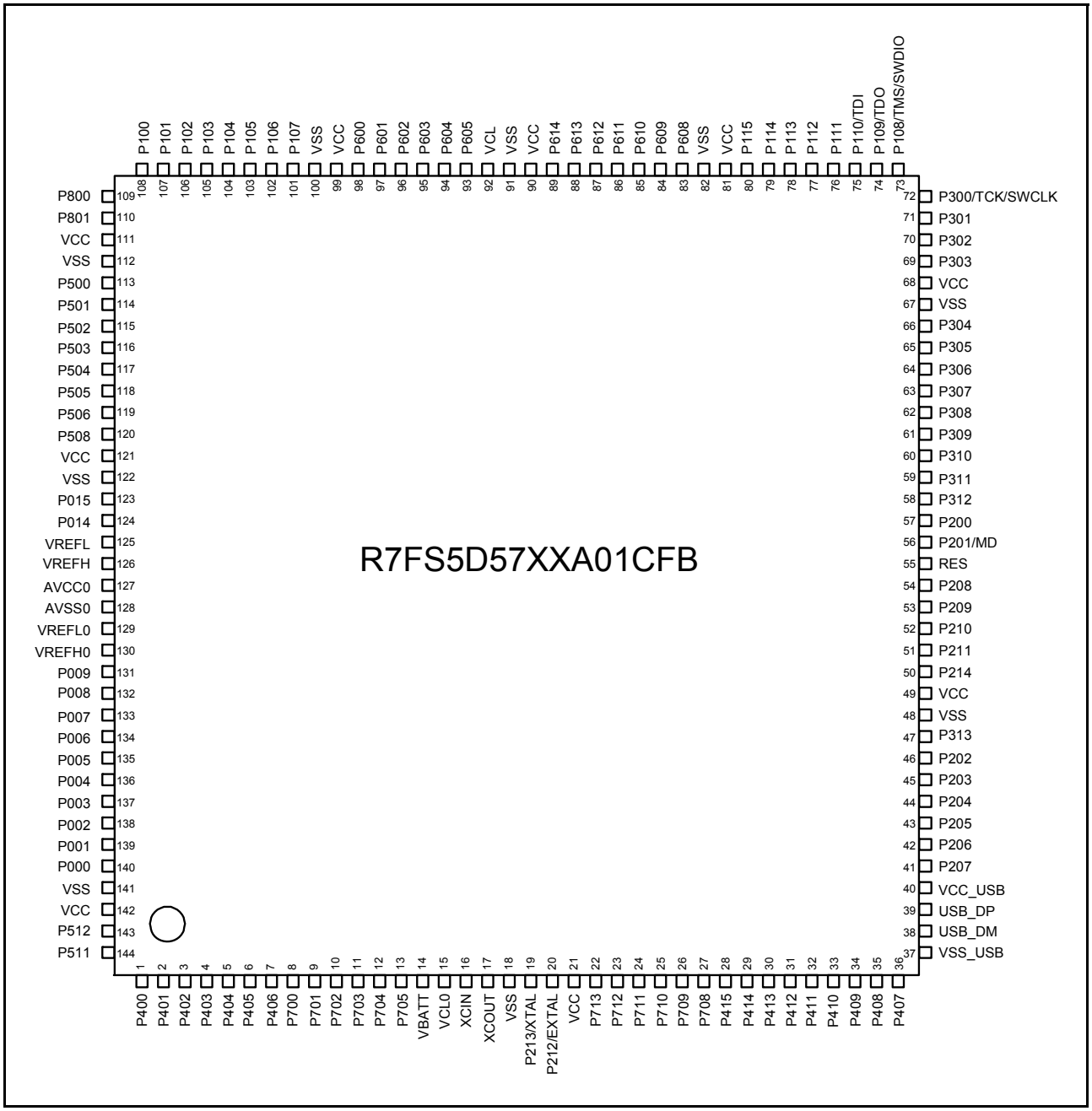


Figure 1.4 Pin assignment for 144-pin LQFP (top view)

1.7 Pin Lists

Pin number						Extbus		Timers				Communication interfaces									Analog		HMI	
LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	SDHI	ADC12	DAC12, ACMPHS	CTSU	PDC
N13	1	1	-	IRQ0	P400	-	-	AGTIO1	-	GTIOC 6A	-	-	SCK4	SCK7	SCL0 _A	-	AUDIO _CLK	ET0_WOL	ET0_WOL	-	ADTRG 1	-	-	-
L11	2	2	-	IRQ5-DS	P401	-	-	-	GTETRGA	GTIOC 6B	-	CTX0	CTS4_R TS4/SS4	TXD7/M OSI7/SD A7	SDA0 _A	-	-	ET0_MDC	ET0_MDC	-	-	-	-	-
M13	3	3	CACREF	IRQ4-DS	P402	-	-	AGTIO0/ AGTIO1	-	-	RTCI C0	CRX0	-	RXD7/MI SO7/SC L7	-	-	AUDIO _CLK	ET0_MDI O	ET0_MDI O	-	-	-	-	VSYNC
K11	4	4	-	-	P403	-	-	AGTIO0/ AGTIO1	-	GTIOC 3A	RTCI C1	-	-	CTS7_R TS7/SS7	-	-	SSIBC K0_A	ET0_LINK STA	ET0_LINK STA	SD1DA T7_B	-	-	-	PIXD7
L12	5	5	-	-	P404	-	-	-	-	GTIOC 3B	RTCI C2	-	-	-	-	-	SSILR CK0/S SIFS0 _A	ET0_EXO UT	ET0_EXO UT	SD1DA T6_B	-	-	-	PIXD6
L13	6	6	-	-	P405	-	-	-	-	GTIOC 1A	-	-	-	-	-	-	SSITX D0_A	ET0_TX_ EN	RMII0_TX D_EN_B	SD1DA T5_B	-	-	-	PIXD5
J10	7	7	-	-	P406	-	-	-	-	GTIOC 1B	-	-	-	-	-	SSLB3 _C	SSIRX D0_A	ET0_RX_ ER	RMII0_TX D1_B	SD1DA T4_B	-	-	-	PIXD4
H10	8	-	-	-	P700	-	-	-	-	GTIOC 5A	-	-	-	-	-	MISOB _C	-	ET0_ETX D1	RMII0_TX D0_B	SD1DA T3_B	-	-	-	PIXD3
K12	9	-	-	-	P701	-	-	-	-	GTIOC 5B	-	-	-	-	-	MOSIB _C	-	ET0_ETX D0	REF50CK 0_B	SD1DA T2_B	-	-	-	PIXD2
K13	10	-	-	-	P702	-	-	-	-	GTIOC 6A	-	-	-	-	-	RSPC KB_C	-	ET0_ERX D1	RMII0_RX D0_B	SD1DA T1_B	-	-	-	PIXD1
J11	11	-	-	-	P703	-	-	-	-	GTIOC 6B	-	-	-	-	-	SSLB0 _C	-	ET0_ERX D0	RMII0_RX D1_B	SD1DA T0_B	-	VCOUT	-	PIXD0
H11	12	-	-	-	P704	-	-	AGTO0	-	-	-	CTX0	-	-	-	SSLB1 _C	-	ET0_RX_ CLK	RMII0_RX _ER_B	SD1CL K_B	-	-	-	HSYNC
G11	13	-	-	-	P705	-	-	AGTIO0	-	-	-	CRX0	-	-	-	SSLB2 _C	-	ET0_CRS	RMII0_CR S_DV_B	SD1CM D_B	-	-	-	PIXCLK
J12	14	8	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J13	15	9	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H13	16	10	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H12	17	11	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F12	18	12	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G12	19	13	XTAL	IRQ2	P213	-	-	-	GTETRGC	GTIOC 0A	-	-	-	TXD1/M OSI1/SD A1	-	-	-	-	-	-	ADTRG 1	-	-	-
G13	20	14	EXTAL	IRQ3	P212	-	-	AGTEE1	GTETRGD	GTIOC 0B	-	-	-	RXD1/MI SO1/SC L1	-	-	-	-	-	-	-	-	-	-
F13	21	15	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G10	22	-	-	-	P713	-	-	AGTOA0	-	GTIOC 2A	-	-	-	-	-	-	-	-	-	-	-	-	TS17	-
F11	23	-	-	-	P712	-	-	AGTOB0	-	GTIOC 2B	-	-	-	-	-	-	-	-	-	-	-	-	TS16	-
E13	24	-	-	-	P711	-	-	AGTEE0	-	-	-	-	-	CTS1_R TS1/SS1	-	-	-	ET0_TX_ CLK	-	-	-	-	TS15	-
E12	25	-	-	-	P710	-	-	-	-	-	-	-	-	SCK1	-	-	-	ET0_TX_ ER	-	-	-	-	TS14	-
F10	26	-	-	IRQ10	P709	-	-	-	-	-	-	-	-	TXD1/M OSI1/SD A1	-	-	-	ET0_ETX D2	-	-	-	-	TS13	-
D13	27	16	CACREF	IRQ11	P708	-	-	-	-	-	-	-	-	RXD1/MI SO1/SC L1	-	SSLA3 _B	AUDIO _CLK	ET0_ETX D3	-	-	-	-	TS12	PCKO
E11	28	17	-	IRQ8	P415	-	-	-	-	GTIOC 0A	-	USB_ VBUS EN	-	-	-	SSLA2 _B	-	ET0_TX_ EN	RMII0_TX D_EN_A	SD0CD	-	-	TS11	PIXD5
D12	29	18	-	IRQ9	P414	-	-	-	-	GTIOC 0B	-	-	-	-	-	SSLA1 _B	-	ET0_RX_ ER	RMII0_TX D1_A	SD0WP	-	-	TS10	PIXD4
E10	30	19	-	-	P413	-	-	-	GTOUUP	-	-	-	CTS0_R TS0/SS0	-	-	SSLA0 _B	-	ET0_ETX D1	RMII0_TX D0_A	SD0CL K_A	-	-	TS09	PIXD3
C13	31	20	-	-	P412	-	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPC KA_B	-	ET0_ETX D0	REF50CK 0_A	SD0CM D_A	-	-	TS08	PIX02
D11	32	21	-	IRQ4	P411	-	-	AGTOA1	GTOVUP	GTIOC 9A	-	-	TXD0/M OSI0/SD A0	CTS3_R TS3/SS3	-	MOSIA _B	-	ET0_ERX D1	RMII0_RX D0_A	SD0DA T0_A	-	-	TS07	PIX01
C12	33	22	-	IRQ5	P410	-	-	AGTOB1	GTOVLO	GTIOC 9B	-	-	RXD0/MI SO0/SC L0	SCK3	-	MISOA _B	-	ET0_ERX D0	RMII0_RX D1_A	SD0DA T1_A	-	-	TS06	PIXD0
B13	34	23	-	IRQ6	P409	-	-	-	GTOWUP	GTIOC 10A	-	USB_ EXICE N	-	TXD3/M OSI3/SD A3	-	-	-	ET0_RX_ CLK	RMII0_RX _ER_A	-	-	-	TS05	HSYNC
D10	35	24	-	IRQ7	P408	-	-	-	GTOWLO	GTIOC 10B	-	USB_I D	-	RXD3/MI SO3/SC L3	SCL0 _B	-	-	ET0_CRS	RMII0_CR S_DV_A	-	-	-	TS04	PIXCLK
A13	36	25	-	-	P407	-	-	AGTIO0	-	-	RTC OUT	USB_ VBUS	CTS4_R TS4/SS4	-	SDA0 _B	SSLB3 _A	-	ET0_EXO UT	ET0_EXO UT	-	ADTRG 0	-	TS03	-
B11	37	26	VSS_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A12	38	27	-	-	-	-	-	-	-	-	-	USB_ DM	-	-	-	-	-	-	-	-	-	-	-	-
B12	39	28	-	-	-	-	-	-	-	-	-	USB_ DP	-	-	-	-	-	-	-	-	-	-	-	-
A11	40	29	VCC_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Pin number						Extbus		Timers				Communication interfaces										Analog		HMI	
LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	SDHI	ADC12	DAC12, ACMPHS	CTSU	PDC
E1	86	-	CLKOUT /CACRE F	-	P611	-	SDCS	-	-	-	-	-	-	CTS7_R TS7/SS7	-	-	-	-	-	-	-	-	-	-
F2	87	-	-	-	P612	D08[A08/ D08]	DQ08	-	-	-	-	-	-	SCK7	-	-	-	-	-	-	-	-	-	-
F1	88	-	-	-	P613	D09[A09/ D09]	DQ09	-	-	-	-	-	-	TXD7	-	-	-	-	-	-	-	-	-	-
G3	89	-	-	-	P614	D10[A10/ D10]	DQ10	-	-	-	-	-	-	RXD7	-	-	-	-	-	-	-	-	-	-
G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	93	-	-	-	P605	D11[A11/ D11]	DQ11	-	-	GTIOC 8A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G4	94	-	-	-	P604	D12[A12/ D12]	DQ12	-	-	GTIOC 8B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	95	-	-	-	P603	D13[A13/ D13]	DQ13	-	-	GTIOC 7A	-	-	-	CTS9_R TS9/SS9	-	-	-	-	-	-	-	-	-	-	-
J1	96	65	-	-	P602	EBC LK	SDCL K	-	-	GTIOC 7B	-	-	-	TXD9	-	-	-	-	-	-	-	-	-	-	-
J2	97	66	-	-	P601	WR/ WR0	DQM0	-	-	GTIOC 6A	-	-	-	RXD9	-	-	-	-	-	-	-	-	-	-	-
H4	98	67	CLKOUT /CACRE F	-	P600	RD	-	-	-	GTIOC 6B	-	-	-	SCK9	-	-	-	-	-	-	-	-	-	-	-
K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	101	68	-	KR07	P107	D07[A07/ D07]	DQ07	AGTOA0	-	GTIOC 8A	-	-	CTS8_R TS8/SS8	-	-	-	-	-	-	-	-	-	-	-	-
K3	102	69	-	KR06	P106	D06[A06/ D06]	DQ06	AGTOB0	-	GTIOC 8B	-	-	SCK8	-	-	SSLA3 _A	-	-	-	-	-	-	-	-	-
J4	103	70	-	IRQ0/ KR05	P105	D05[A05/ D05]	DQ05	-	GTETRGA	GTIOC 1A	-	-	TXD8/M OSI8/SD A8	-	-	SSLA2 _A	-	-	-	-	-	-	-	-	-
L3	104	71	-	IRQ1/ KR04	P104	D04[A04/ D04]	DQ04	-	GTETRGB	GTIOC 1B	-	-	RXD8/MI SO8/SC L8	-	-	SSLA1 _A	-	-	-	-	-	-	-	-	-
L1	105	72	-	KR03	P103	D03[A03/ D03]	DQ03	-	GTOWUP	GTIOC 2A_A	-	CTX0	CTS0_R TS0/SS0	-	-	SSLA0 _A	-	-	-	-	-	-	-	-	-
M1	106	73	-	KR02	P102	D02[A02/ D02]	DQ02	AGTO0	GTOWLO	GTIOC 2B_A	-	CRX0	SCK0	-	-	RSPC KA_A	-	-	-	-	ADTRG 0	-	-	-	-
M2	107	74	-	IRQ1/ KR01	P101	D01[A01/ D01]	DQ01	AGTEE0	GTETRGB	GTIOC 5A	-	-	TXD0/M OSI0/SD A0	CTS1_R TS1/SS1	SDA1 _B	MOSIA _A	-	-	-	-	-	-	-	-	-
N1	108	75	-	IRQ2/ KR00	P100	D00[A00/ D00]	DQ00	AGTIO0	GTETRGA	GTIOC 5B	-	-	RXD0/MI SO0/SC L0	SCK1	SCL1 _B	MISOA _A	-	-	-	-	-	-	-	-	-
L2	109	-	-	-	P800	D14[A14/ D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N2	110	-	-	-	P801	D15[A15/ D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC 11A	-	USB_ VBUS EN	-	-	-	QSPC LK	-	-	-	SD1CL K_A	AN016	IVREF0	-	-
M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC 11B	-	USB_ OVRC URA	-	TXD5/M OSI5/SD A5	-	QSSL	-	-	-	SD1CM D_A	AN116	IVREF1	-	-
L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC 12A	-	USB_ OVRC URB	-	RXD5/MI SO5/SC L5	-	QIO0	-	-	-	SD1DA T0_A	AN017	IVCMP0	-	-
K5	116	79	-	-	P503	-	-	-	GTETRGC	GTIOC 12B	-	USB_ EXICE N	CTS6_R TS6/SS6	SCK5	-	QIO1	-	-	-	SD1DA T1_A	AN117	-	-	-
L5	117	80	-	-	P504	ALE	-	-	GTETRGD	GTIOC 13A	-	USB_I D	SCK6	CTS5_R TS5/SS5	-	QIO2	-	-	-	SD1DA T2_A	AN018	-	-	-
K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC 13B	-	-	RXD6/MI SO6/SC L6	-	-	QIO3	-	-	-	SD1DA T3_A	AN118	-	-	-
L6	119	-	-	IRQ15	P506	-	-	-	-	-	-	-	TXD6/M OSI6/SD A6	-	-	-	-	-	-	SD1CD	AN019	-	-	-
N4	120	81	-	-	P508	-	-	-	-	-	-	-	SCK6	SCK5	-	-	-	-	-	SD1DA T3_A	AN020	-	-	-
N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M6	123	84	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/ AN106	DA1/ IVCMP1	-	-
N6	124	85	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/ AN105	DA0/ IVREF3	-	-
M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 2.4 I/O V_{IH}, V_{IL} (2 of 2)

Item					Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)*2			V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.3	
					ΔV_T	VCC × 0.05	-	-	
		5 V-tolerant ports*3, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3	
					V_{IL}	-	-	V_{BATT} × 0.2	
					ΔV_T	V_{BATT} × 0.05	-	-	
				When VCC power supply is selected	V_{IH}	VCC × 0.8	-	Higher voltage either VCC + 0.3 V or V_{BATT} + 0.3 V	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
			When not using the Battery Backup Function		V_{IH}	VCC × 0.8	-	VCC + 0.3	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		Other input pins*4			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
	Ports	5 V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.2	
		Other input pins*6			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	

Note 1. SCL0_B (P204), SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B (P408), SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 8 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 22 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 21 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

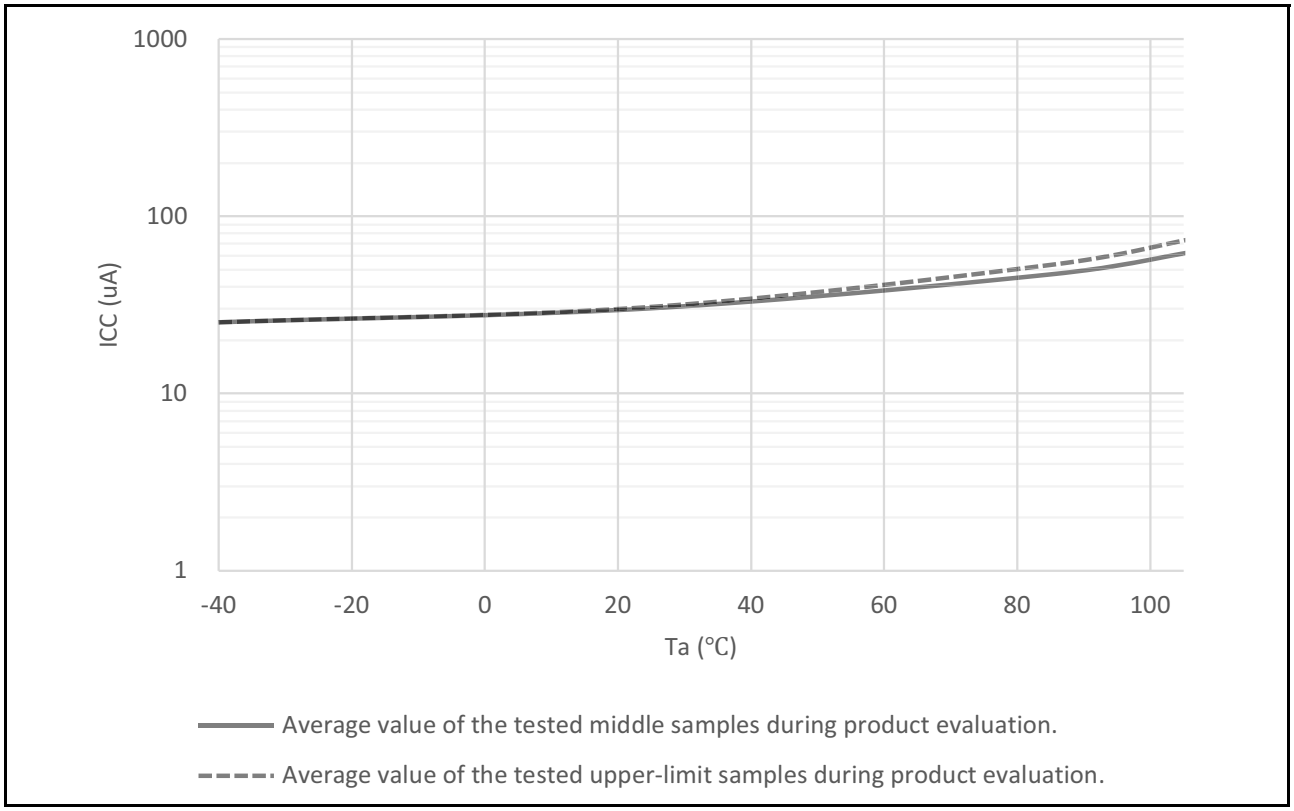


Figure 2.3 **Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)**

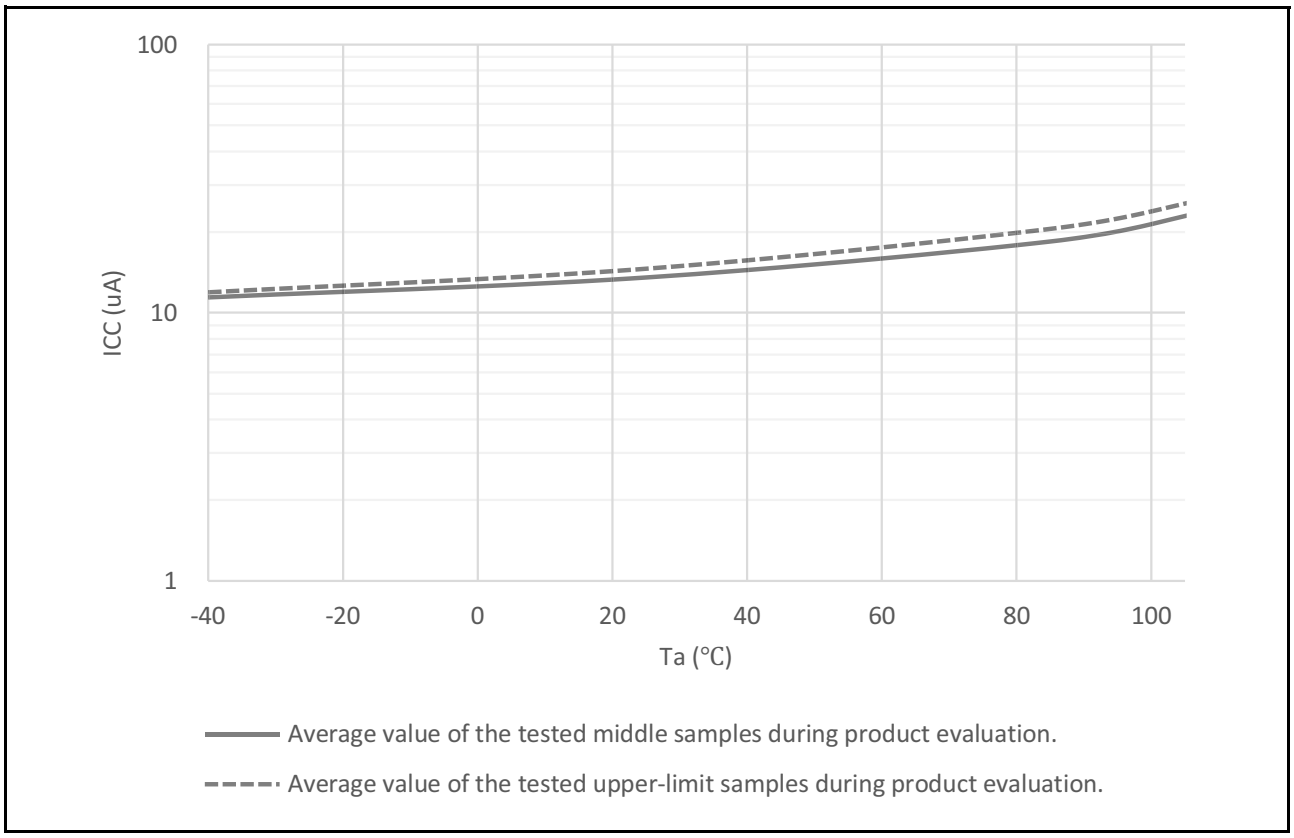


Figure 2.4 **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)**

Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL*2	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	-	-	64.7	μs	-
FLL stabilization wait time		t_{FLLWT}	-	-	1.8	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		t_{PLLWT}	-	-	174.9	μs	Figure 2.11

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	-*Note:	s	-

Note: When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

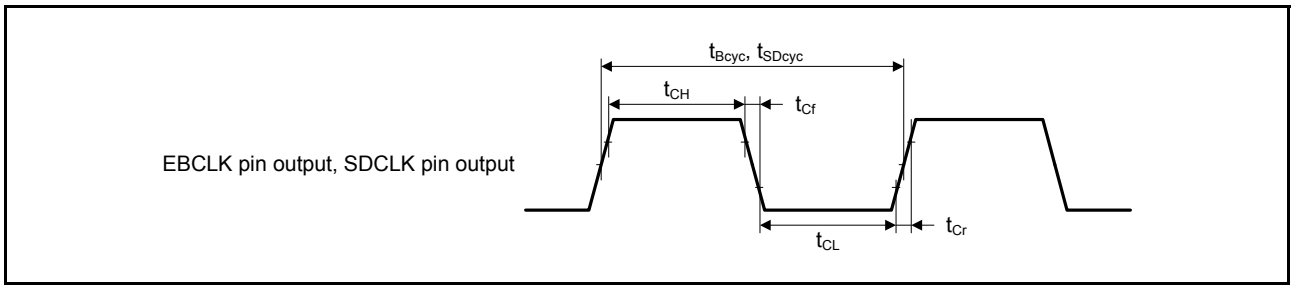
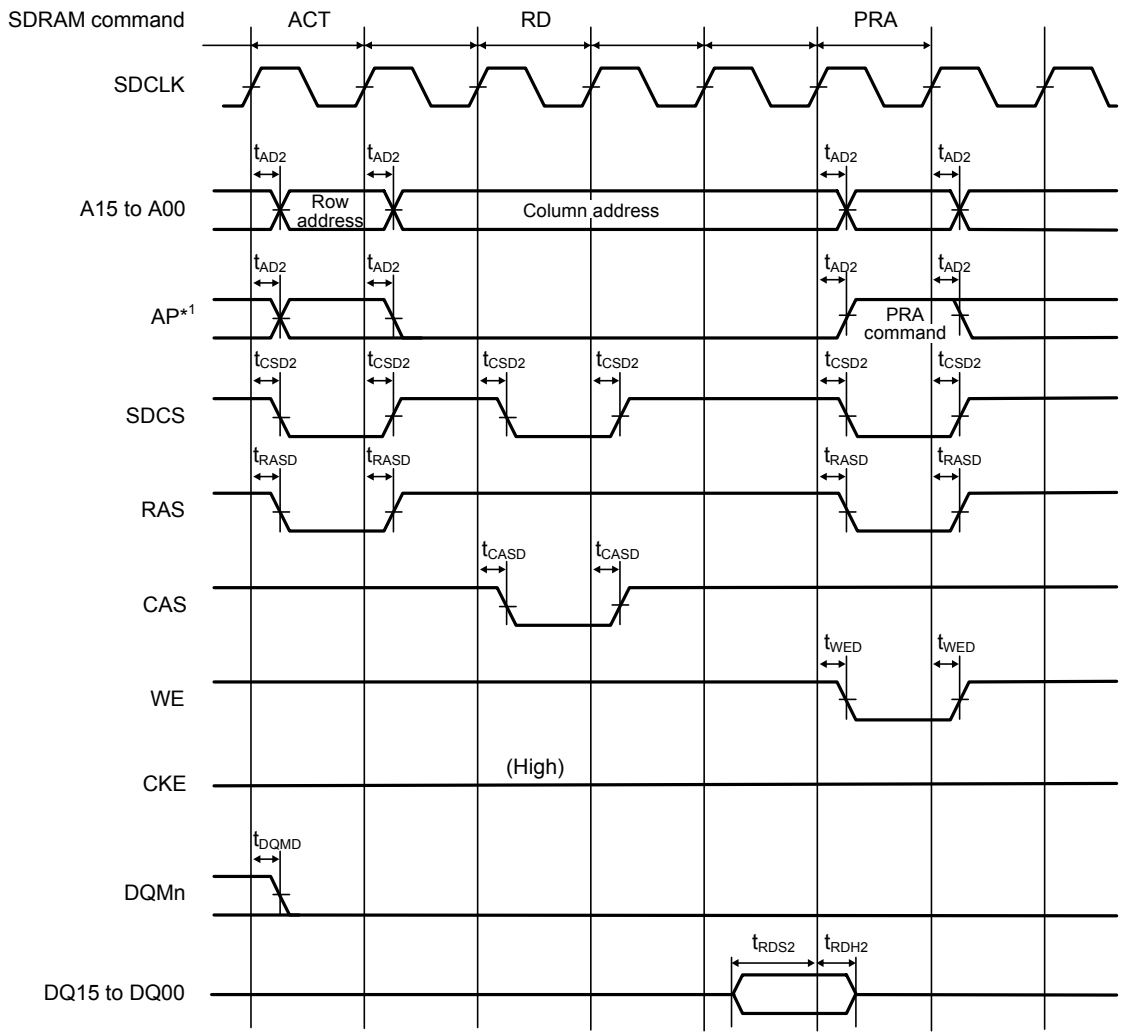
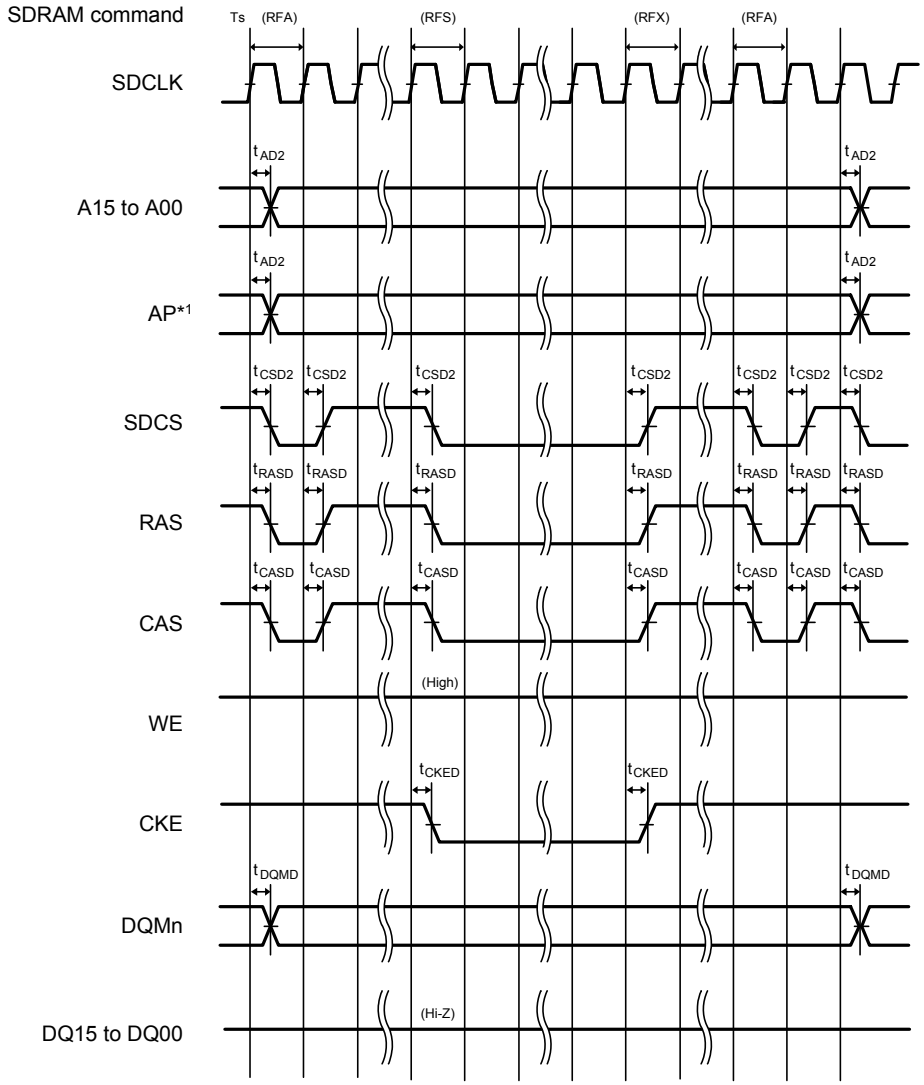


Figure 2.7 EBCLK and SDCLK output timing



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.27 SDRAM single read timing



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.30 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.31
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 2.32

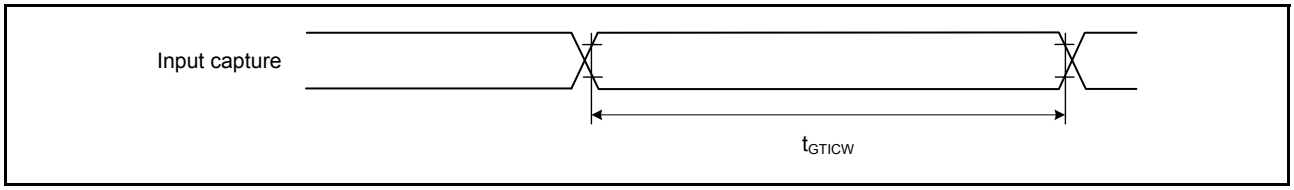


Figure 2.33 GPT32 input capture timing

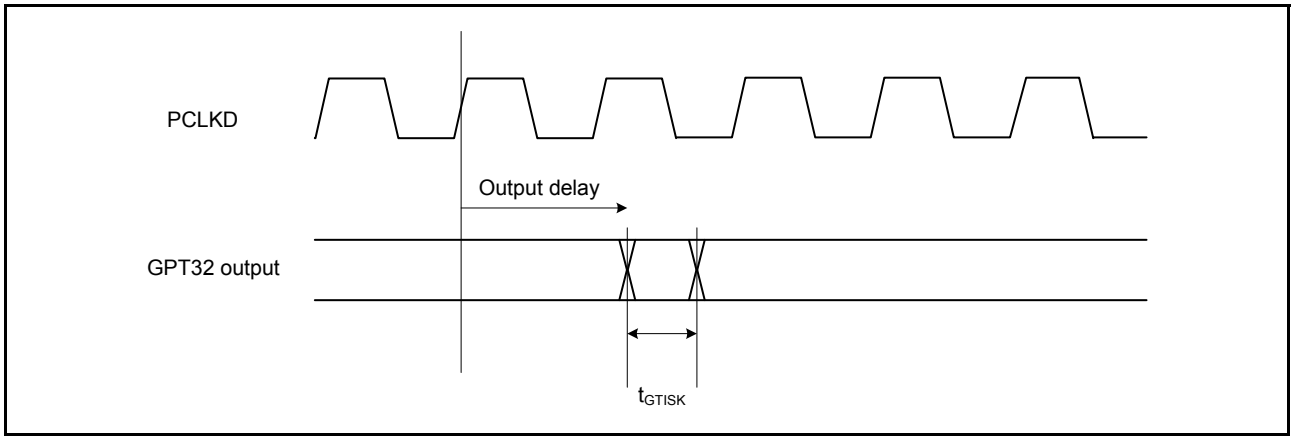


Figure 2.34 GPT32 output delay skew

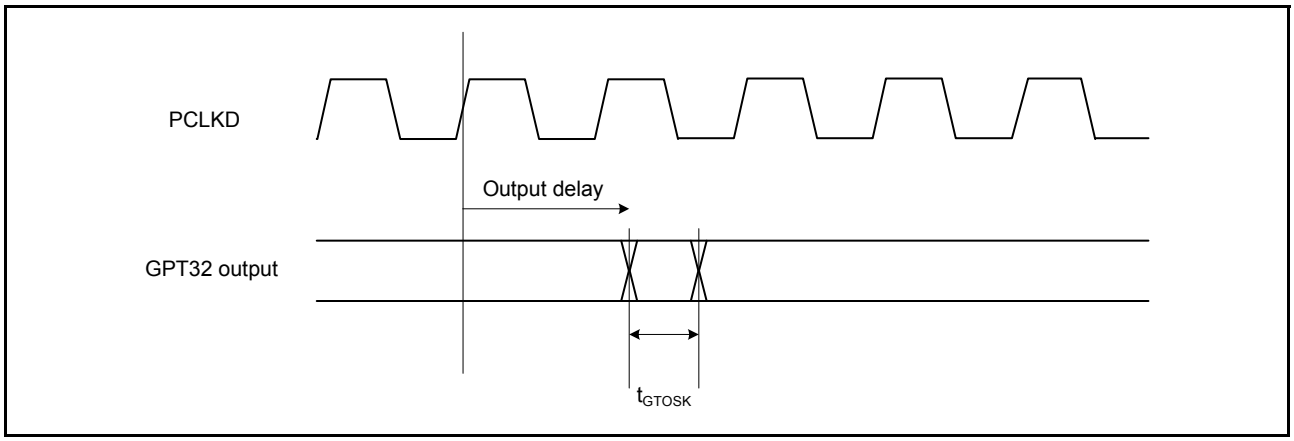


Figure 2.35 GPT32 output delay skew for OPS

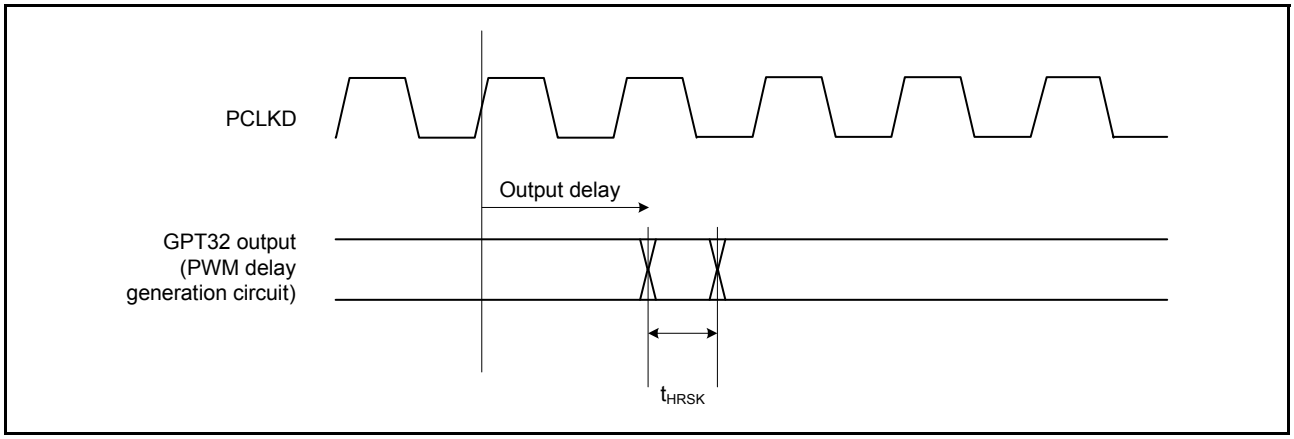


Figure 2.36 GPT32 (PWM Delay Generation Circuit) output delay skew

Note 2. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
Note 4. N is set to an integer from 1 to 8 by the SSLND register.

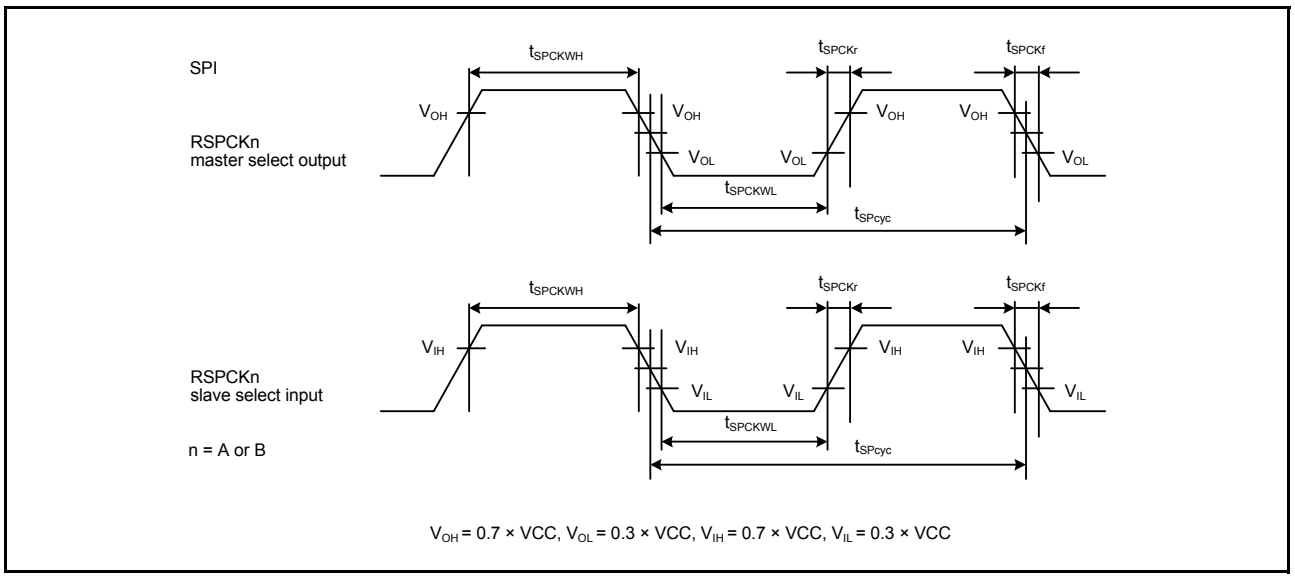


Figure 2.48 SPI clock timing

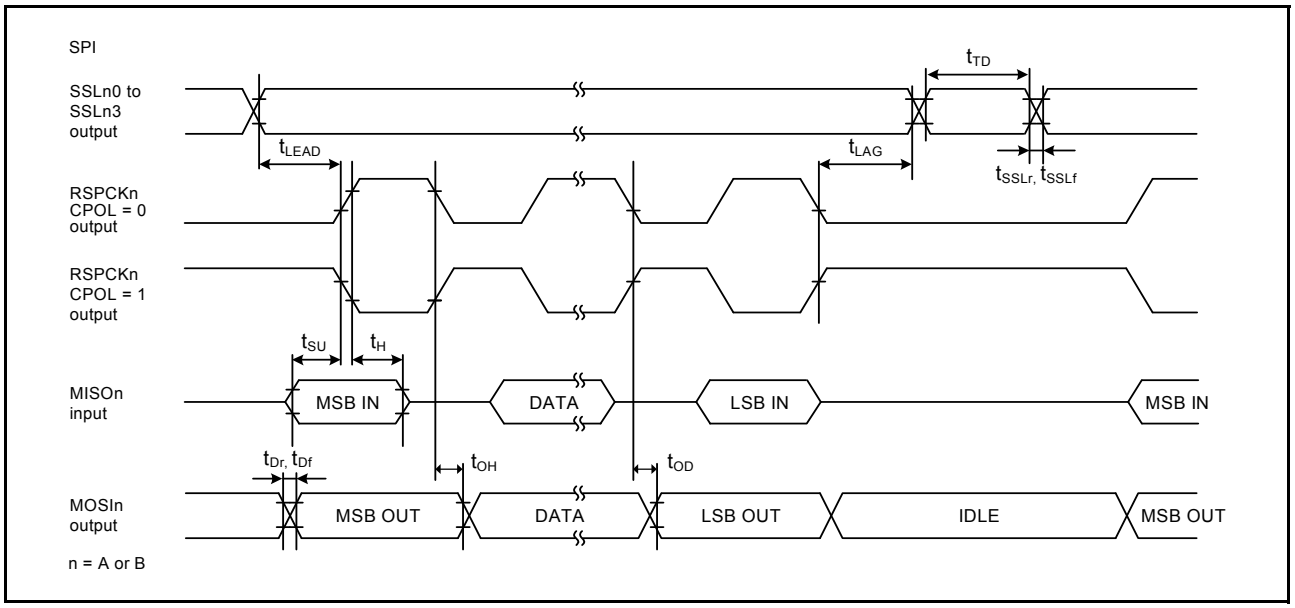


Figure 2.49 SPI timing for master when CPHA = 0

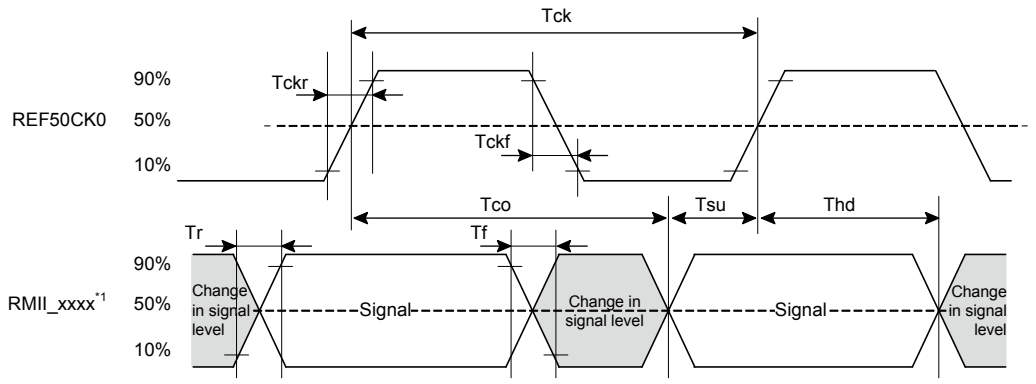
Table 2.27 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Item		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.57
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.
Note 3. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Note 3. The following pins must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group.
REF50CK0_A, REF50CK0_B, RMII0_xxxx_A, RMII0_xxxx_B.



Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Figure 2.64 REF50CK0 and RMII signal timing

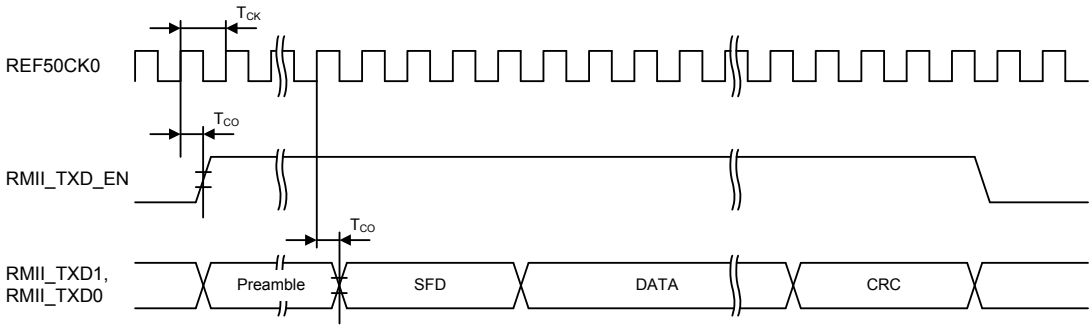


Figure 2.65 RMII transmission timing

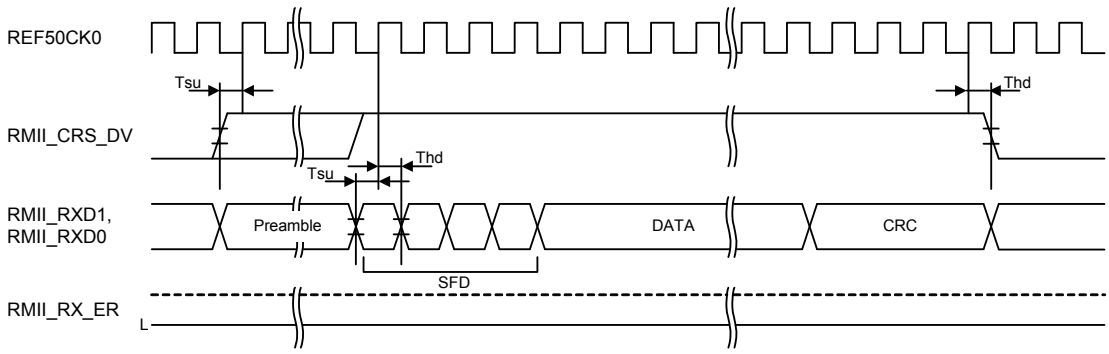


Figure 2.66 RMII reception timing in normal operation

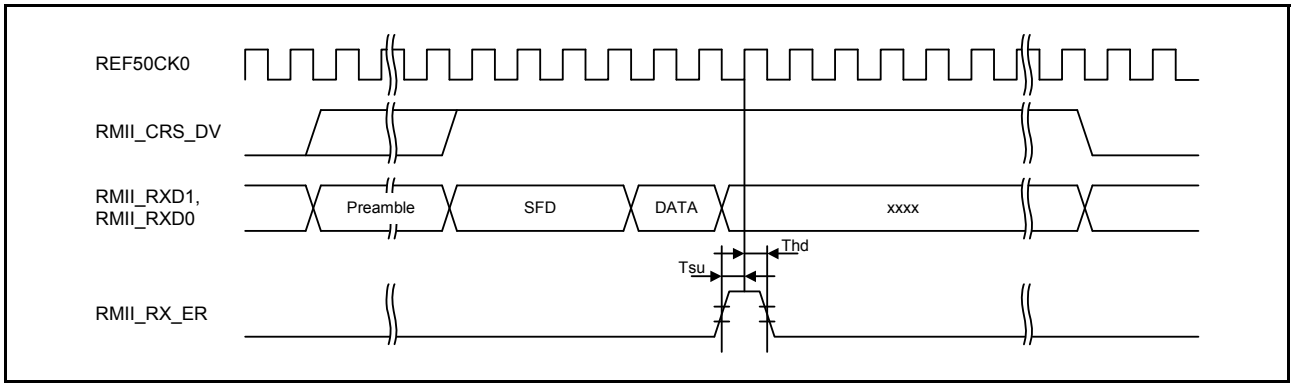


Figure 2.67 RMII reception timing when an error occurs

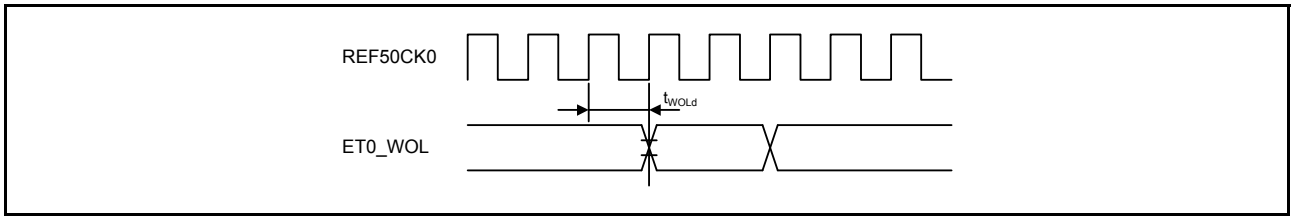


Figure 2.68 WOL output timing for RMII

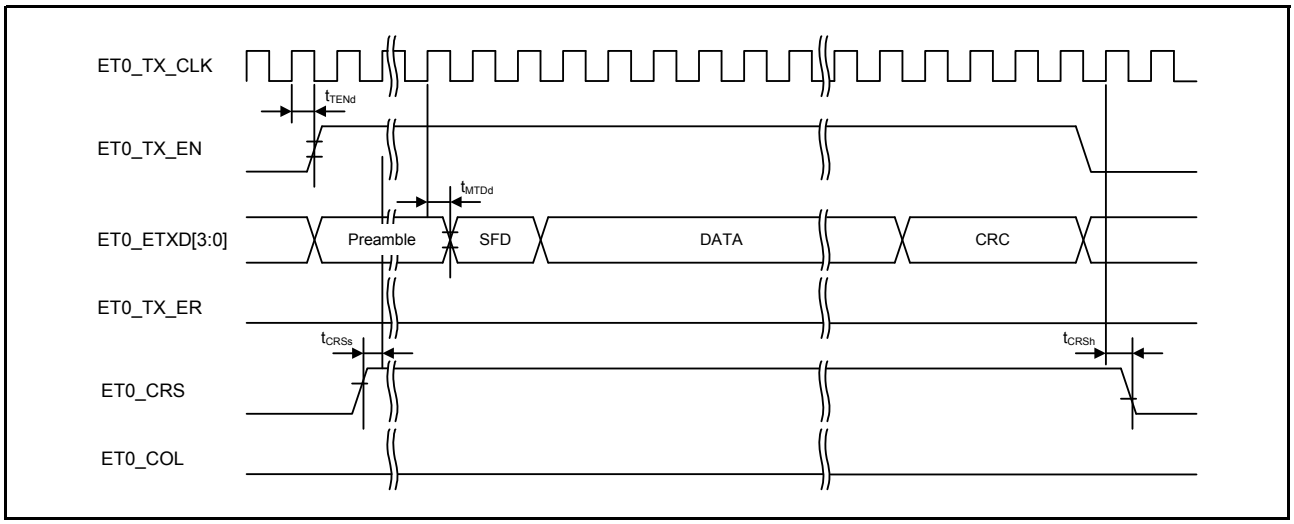


Figure 2.69 MII transmission timing in normal operation

Table 2.37 A/D conversion characteristics for simultaneous use of channel-dedicated sample-and-hold circuits in unit0 and unit1

Conditions: PCLKC = 30/60 MHz

Item		Min	Typ	Max	Test conditions
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±5.0	• PCLKC = 60 MHz • Sampling in 15 states
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±3.5	• PCLKC = 30 MHz • Sampling in 7 states
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit0 and unit1, setting the ADSHMSR.SHMD bit to 1 is recommended.

Table 2.38 A/D internal reference voltage characteristics

Item	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	-
Sampling time	4.15	-	-	μs	-

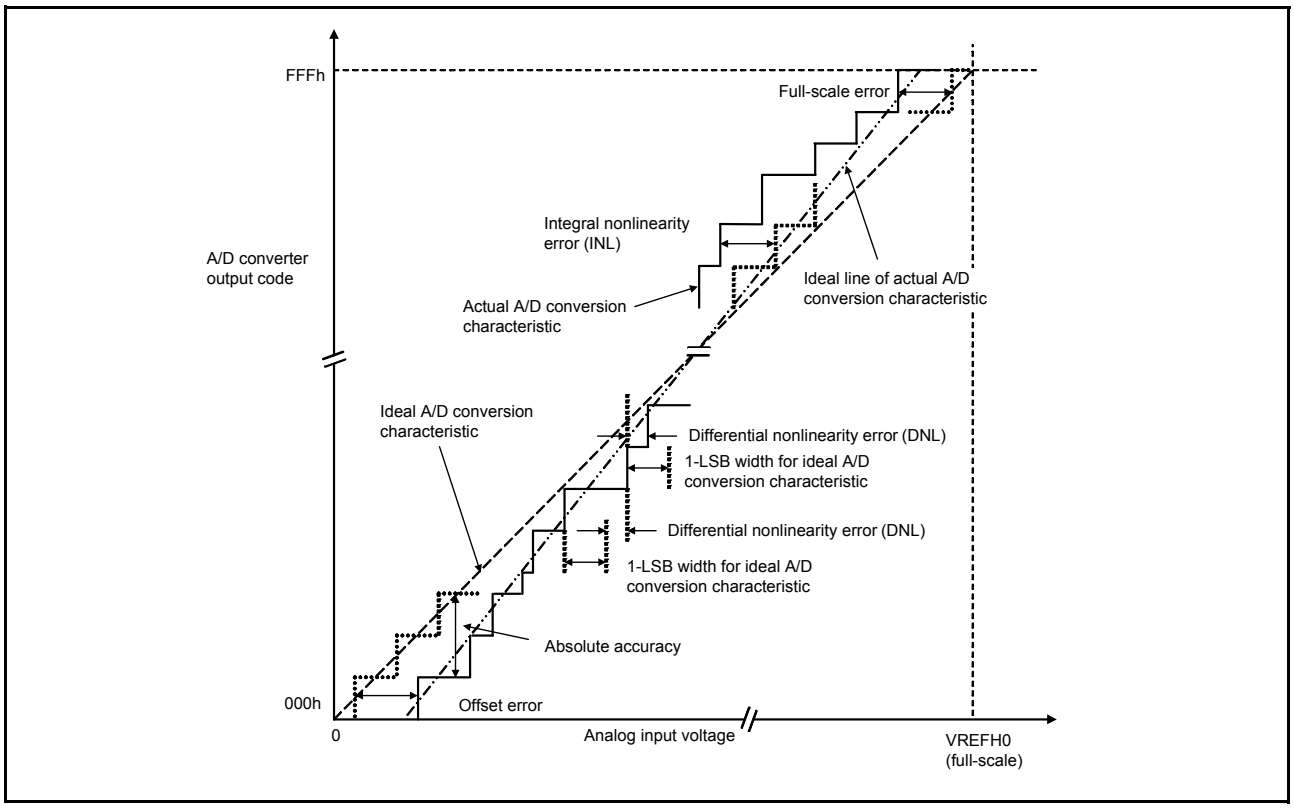


Figure 2.81 Illustration of ADC12 characteristic terms

2.13 Flash Memory Characteristics

2.13.1 Code Flash Memory Characteristics

Table 2.46 Code flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
Suspend delay during programming		t_{SPD}	-	-	264	-	-	120	μs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	-	-	216	-	-	120	μs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	-	-	1.7	-	-	1.7	ms	
Forced stop command		t_{FD}	-	-	32	-	-	20	μs	
Data hold time*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.