Renesas Electronics America Inc - R7FS5D57C3A01CFP#AA0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	109
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs5d57c3a01cfp-aa0

Table 1.7 Timers (2 of 2)

Feature	Functional description
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual.

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 32, Serial Communications Interface (SCI) in User's Manual.
IrDA Interface (IrDA)	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 33, IrDA Interface in User's Manual.
I^2C Bus Interface (IIC)	The 3-channel IIC module conforms with and provides a subset of the NXP I^2C bus (Inter-Integrated Circuit bus) interface functions. See section 34, I^2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 36, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I^2S (Inter-Integrated Sound) 2ch, 4ch, 6ch, 8ch, Word Select (WS) Continue/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 39, Serial Sound Interface Enhanced (SSIE) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 37, Quad Serial Peripheral Interface (QSPI) in User's Manual.
Control Area Network (CAN) module	The Control Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 35, Controller Area Network (CAN) in User's Manual.
USB 2.0 Full-Speed Module (USBFS)	The full-speed USB controller can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 31, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.16 Pin functions (4 of 5)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode.
	RMII0_CRS_DV	Input	Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pin for data transmit enable signal in RMII mode
	RMII0_RX_ER	Input	Indicates an error occurred during reception of data in RMII mode
	ET0_CRS	Input	Carrier detection/data reception enable signal
	ET0_RX_DV	Input	Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0
	ET0_EXOUT	Output	General-purpose external output pin
	ET0_LINKSTA	Input	Input link status from the PHY-LSI
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable signal. Functions as signal indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0
	ET0_TX_ER	Output	Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission
	ET0_RX_ER	Input	Receive error pin. Functions as signal to recognize an error during reception
	ET0_TX_CLK	Input	Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER
	ET0_RX_CLK	Input	Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER
	ET0_COL	Input	Input collision detection signal
	ET0_WOL	Output	Receive Magic packets
	ET0_MDC	Output	Output reference clock signal for information transfer through ET0_MDIO
	ET0_MDIO	I/O	Input or output bidirectional signal for exchange of management data with PHY-LSI
SDHI	SD0CLK, SD1CLK	Output	SD clock output pins
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pins
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins
	SD0CD, SD1CD	Input	SD card detection pins
	SD0WP	Input	SD write-protect signals
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.

Pin number						Extbus		Timers				Communication interfaces										Analog		HMI	
LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	SDHI	ADC12	DAC12, ACMPHS	CTSU	PDC
E1	86	-	CLKOUT/CACREF	-	P611	-	SDCS	-	-	-	-	-	-	CTS7_RTS7/SS7	-	-	-	-	-	-	-	-	-	-
F2	87	-	-	-	P612	D08[A08/D08]	DQ08	-	-	-	-	-	-	SCK7	-	-	-	-	-	-	-	-	-	-
F1	88	-	-	-	P613	D09[A09/D09]	DQ09	-	-	-	-	-	-	TXD7	-	-	-	-	-	-	-	-	-	-
G3	89	-	-	-	P614	D10[A10/D10]	DQ10	-	-	-	-	-	-	RXD7	-	-	-	-	-	-	-	-	-	-
G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	93	-	-	-	P605	D11[A11/D11]	DQ11	-	-	GTIOC8A	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G4	94	-	-	-	P604	D12[A12/D12]	DQ12	-	-	GTIOC8B	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	95	-	-	-	P603	D13[A13/D13]	DQ13	-	-	GTIOC7A	-	-	-	CTS9_RTS9/SS9	-	-	-	-	-	-	-	-	-	-
J1	96	65	-	-	P602	EBCLK	SDCLK	-	-	GTIOC7B	-	-	-	TXD9	-	-	-	-	-	-	-	-	-	-
J2	97	66	-	-	P601	WR/WR0	DQM0	-	-	GTIOC6A	-	-	-	RXD9	-	-	-	-	-	-	-	-	-	-
H4	98	67	CLKOUT/CACREF	-	P600	RD	-	-	-	GTIOC6B	-	-	-	SCK9	-	-	-	-	-	-	-	-	-	-
K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	101	68	-	KR07	P107	D07[A07/D07]	DQ07	AGTOA0	-	GTIOC8A	-	-	CTS8_RTS8/SS8	-	-	-	-	-	-	-	-	-	-	-
K3	102	69	-	KR06	P106	D06[A06/D06]	DQ06	AGTOB0	-	GTIOC8B	-	-	SCK8	-	-	SSLA3_A	-	-	-	-	-	-	-	-
J4	103	70	-	IRQ0/KR05	P105	D05[A05/D05]	DQ05	-	GTETRGA	GTIOC1A	-	-	TXD8/MOSI8/SDA8	-	-	SSLA2_A	-	-	-	-	-	-	-	-
L3	104	71	-	IRQ1/KR04	P104	D04[A04/D04]	DQ04	-	GTETRGB	GTIOC1B	-	-	RXD8/MISO8/SCL8	-	-	SSLA1_A	-	-	-	-	-	-	-	-
L1	105	72	-	KR03	P103	D03[A03/D03]	DQ03	-	GTOWUP	GTIOC2A_A	-	CTX0	CTS0_RTS0/SS0	-	-	SSLA0_A	-	-	-	-	-	-	-	-
M1	106	73	-	KR02	P102	D02[A02/D02]	DQ02	AGTO0	GTOWLO	GTIOC2B_A	-	CRX0	SCK0	-	-	RSPCKA_A	-	-	-	-	ADTRG0	-	-	-
M2	107	74	-	IRQ1/KR01	P101	D01[A01/D01]	DQ01	AGTEE0	GTETRGB	GTIOC5A	-	-	TXD0/MOSI0/SDA0	CTS1_RTS1/SS1	SDA1_B	MOSIA_A	-	-	-	-	-	-	-	-
N1	108	75	-	IRQ2/KR00	P100	D00[A00/D00]	DQ00	AGTIO0	GTETRGA	GTIOC5B	-	-	RXD0/MISO0/SCL0	SCK1	SCL1_B	MISOA_A	-	-	-	-	-	-	-	-
L2	109	-	-	-	P800	D14[A14/D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N2	110	-	-	-	P801	D15[A15/D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC11A	-	USB_VBUSEN	-	-	-	QSPCLK	-	-	-	SD1CLK_A	AN016	IVREF0	-	-
M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC11B	-	USB_OVRCURA	-	TXD5/MOSI5/SDA5	-	QSSL	-	-	-	SD1CMD_A	AN116	IVREF1	-	-
L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC12A	-	USB_OVRCURB	-	RXD5/MISO5/SCL5	-	QIO0	-	-	-	SD1DAT0_A	AN017	IVCMP0	-	-
K5	116	79	-	-	P503	-	-	-	GTETRGC	GTIOC12B	-	USB_EXICEN	CTS6_RTS6/SS6	SCK5	-	QIO1	-	-	-	SD1DAT1_A	AN117	-	-	-
L5	117	80	-	-	P504	ALE	-	-	GTETRGD	GTIOC13A	-	USB_ID	SCK6	CTS5_RTS5/SS5	-	QIO2	-	-	-	SD1DAT2_A	AN018	-	-	-
K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC13B	-	-	RXD6/MISO6/SCL6	-	-	QIO3	-	-	-	SD1DAT3_A	AN118	-	-	-
L6	119	-	-	IRQ15	P506	-	-	-	-	-	-	-	TXD6/MOSI6/SDA6	-	-	-	-	-	-	SD1CD	AN019	-	-	-
N4	120	81	-	-	P508	-	-	-	-	-	-	-	SCK6	SCK5	-	-	-	-	-	SD1DAT3_A	AN020	-	-	-
N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M6	123	84	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-	-
N6	124	85	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-	-
M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 2.4 I/O V_{IH}, V_{IL} (2 of 2)

Item					Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)*2			V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.3	
					ΔV_T	VCC × 0.05	-	-	
		5 V-tolerant ports*3, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3	
					V_{IL}	-	-	V_{BATT} × 0.2	
					ΔV_T	V_{BATT} × 0.05	-	-	
				When VCC power supply is selected	V_{IH}	VCC × 0.8	-	Higher voltage either VCC + 0.3 V or V_{BATT} + 0.3 V	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
			When not using the Battery Backup Function		V_{IH}	VCC × 0.8	-	VCC + 0.3	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
		Other input pins*4			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	
					ΔV_T	VCC × 0.05	-	-	
	Ports	5 V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	V
					V_{IL}	-	-	VCC × 0.2	
		Other input pins*6			V_{IH}	VCC × 0.8	-	-	
					V_{IL}	-	-	VCC × 0.2	

Note 1. SCL0_B (P204), SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B (P408), SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 8 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 22 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 21 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL}

Item			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P009, P201	-	I_{OH}	-	-	–2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713 (total 18 pins)	Low drive*1	I_{OH}	-	-	–2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	–20	mA
			I_{OL}	-	-	20	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	–2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	–16	mA
			I_{OL}	-	-	16	mA
Permissible output current (max value per pin)	Ports P000 to P009, P201	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713 (total 18 pins)	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	–40	mA
			I_{OL}	-	-	40	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	–32	mA
			I_{OL}	-	-	32	mA
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins		$\Sigma I_{OH\ (max)}$	-	-	–80	mA
			$\Sigma I_{OL\ (max)}$	-	-	80	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. Except for P200, which is an input port.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

Item				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	102*2	mA	ICLK = 120 MHz PCLKA = 120 MHz*7 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*5			-	19	-		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		-	26	-		
			All peripheral clocks disabled, while (1) code executing from flash*5, *6		-	12	-		
		Sleep mode*5, *6			-	10	40		
		Increase during BGO operation	Data flash P/E		-	6	-		
			Code flash P/E		-	8	-		
	Low-speed mode*5				-	1.3	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	1.2	-		ICLK = 32.768 kHz
	Software Standby mode				-	1.3	15		Ta ≤ 85°C
					-	1.3	24		Ta ≤ 105°C
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			-	29	67	µA	Ta ≤ 85°C
					-	29	96		Ta ≤ 105°C
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low power function disabled		-	11.6	32.4		Ta ≤ 85°C
					-	11.6	40		Ta ≤ 105°C
			Power-on reset circuit low power function enabled		-	4.9	23.5		Ta ≤ 85°C
					-	4.9	31		Ta ≤ 105°C
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		-	4.4	-		-
			When a crystal oscillator for low clock loads is in use		-	1.0	-		-
			When a crystal oscillator for standard clock loads is in use		-	1.4	-		-
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		-	0.9	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.1	-		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		-	1.0	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.6	-		V_{BATT} = 3.3 V, VCC = 0 V
Analog power supply current	During 12-bit A/D conversion			AI_{CC}	-	0.8	1.1	mA	-
	During 12-bit A/D conversion with S/H amp				-	2.3	3.3	mA	-
	ACMPHS (1 unit)				-	100	150	µA	-
	Temperature sensor				-	0.1	0.2	mA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.2	mA	-
			With AMP output		-	0.6	1.1	mA	-
	Waiting for A/D, D/A conversion (all units)				-	0.9	1.6	mA	-
	ADC12, DAC12 in standby modes (all units)*8				-	2	8	µA	-
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	-	70	120	µA	-
	Waiting for 12-bit A/D conversion (unit 0)				-	0.07	0.5	µA	-
	ADC12 in standby modes (unit 0)				-	0.07	0.5	µA	-
Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)			AI_{REFH}	-	70	120	µA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.4	mA	-
			With AMP ouput		-	0.1	0.4	mA	-
	Waiting for 12-bit A/D (unit 1), D/A (all units) conversion				-	0.07	0.8	µA	-
	ADC12 unit 1 in standby modes				-	0.07	0.8	µA	-

Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL*2	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	-	-	64.7	µs	-
FLL stabilization wait time		t_{FLLWT}	-	-	1.8	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		t_{PLLWT}	-	-	174.9	µs	Figure 2.11

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	-*Note:	s	-

Note: When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

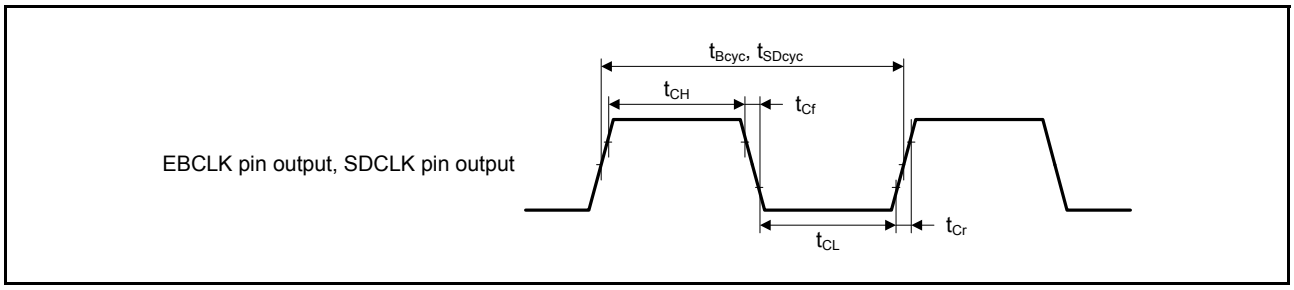

Figure 2.7 EBCLK and SDCLK output timing

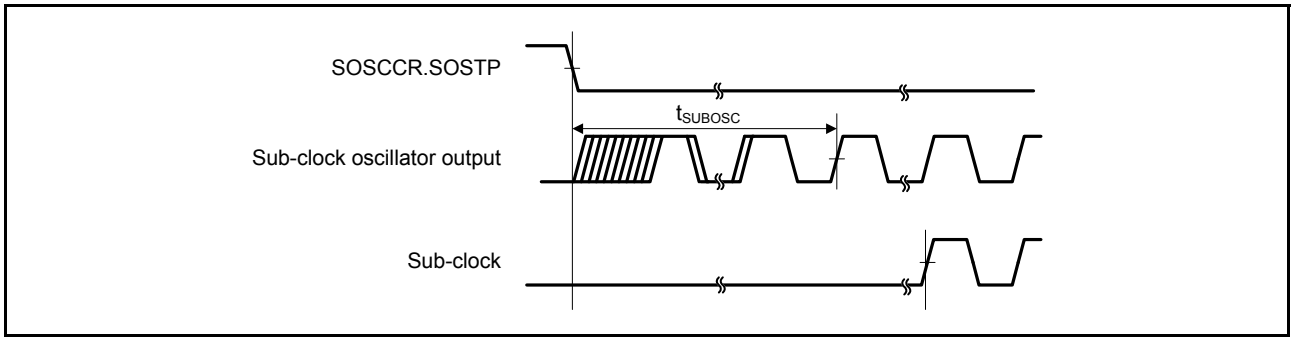

Figure 2.12 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.15 Reset timing

Item		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	1	-	-	ms	Figure 2.13
	Deep Software Standby mode	t_{RESWD}	0.6	-	-	ms	Figure 2.14
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	-	-	ms	
	All other	t_{RESW}	200	-	-	µs	
Wait time after RES cancellation		t_{RESWT}	-	29	32	µs	Figure 2.13
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)		t_{RESW2}	-	320	390	µs	-

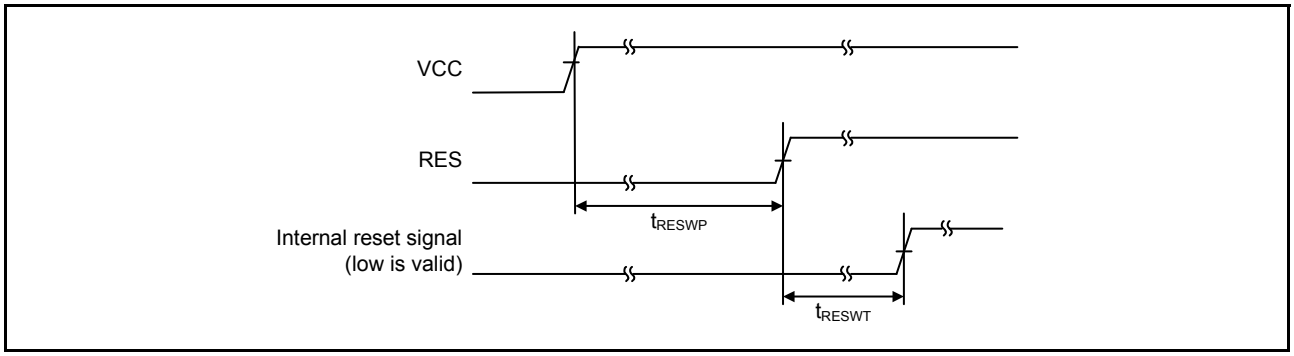

Figure 2.13 Power-on reset timing

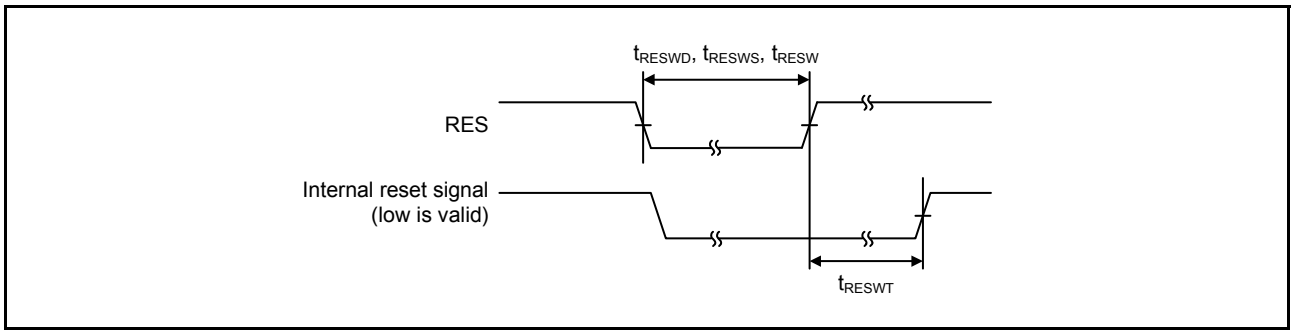

Figure 2.14 Reset input timing

2.3.4 Wakeup Timing

Table 2.16 Timing of recovery from low power modes

Item			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	Figure 2.15 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}	-	230*9	280*9	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}	-	570*9	700*9	µs	
	System clock source is sub-clock oscillator*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	System clock source is LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	System clock source is HOCO clock oscillator*6		t_{SBYHO}	-	240*9, *10	300 *9, *10	µs	
	System clock source is MOCO clock oscillator*7		t_{SBYMO}	-	220*9	300*9	µs	
Recovery time from Deep Software Standby mode			t_{DSBY}	-	0.65	1.0	ms	Figure 2.16
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	34	-	35	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		t_{SNZ}	-	35*9, *10	70 *9, *10	µs	Figure 2.17
	High-speed mode when system clock source is MOCO (8 MHz)		t_{SNZ}	-	11*9	14*9	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).

Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:
STCONR.STCON[1:0] = 00b:16 µs (typical), 34 µs (maximum)
STCONR.STCON[1:0] = 11b:16 µs (typical), 104 µs (maximum).

Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 µs (typical) or 18 µs (maximum) is added as the HOCO wait time.

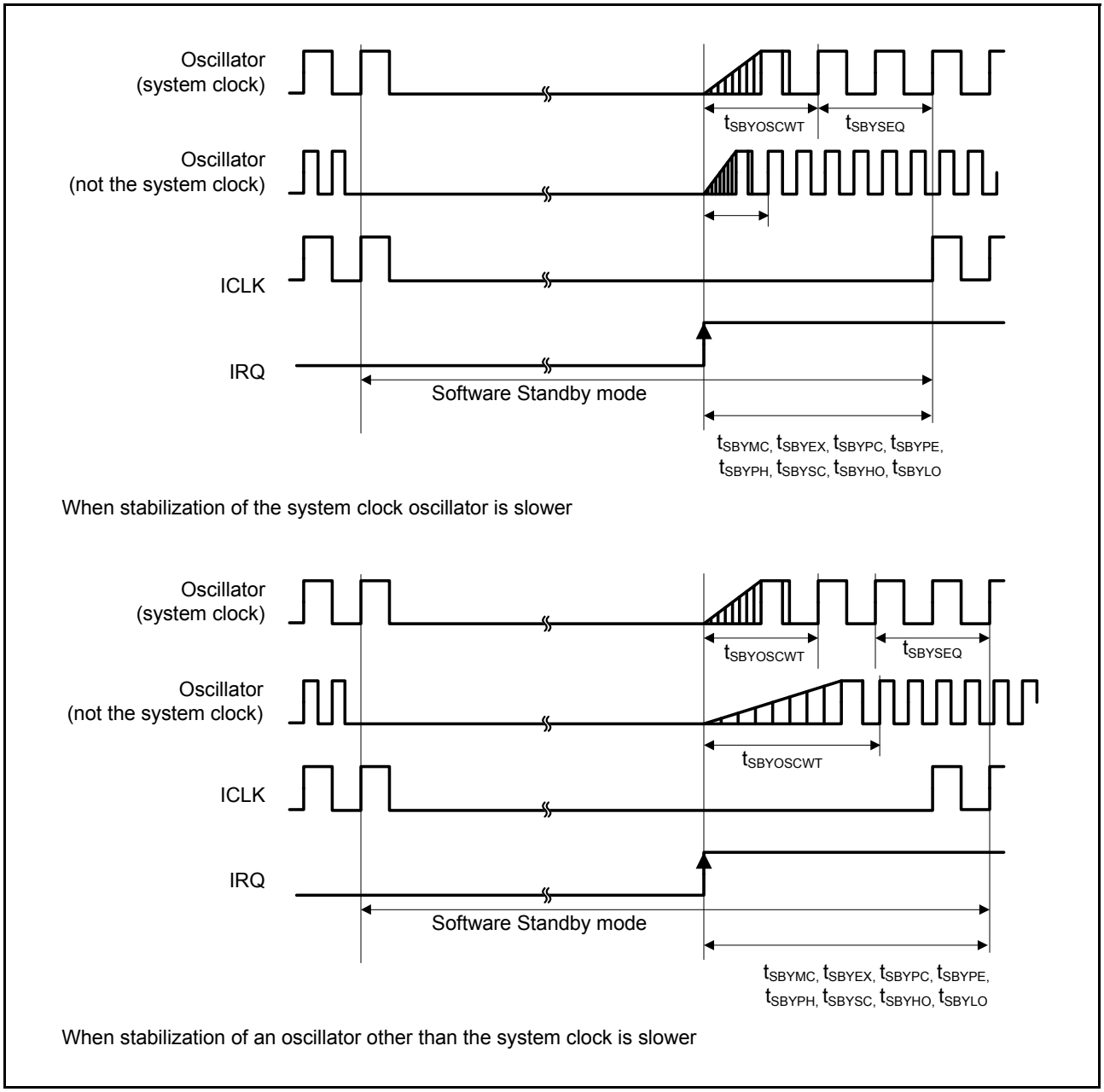

Figure 2.15 Software Standby mode cancellation timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Item			Symbol	Min	Max	Unit	Test conditions
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.33
		Dual edge		2.5	-		
	GTIOCxY output skew (x = 0 to 7, Y= A or B)	Middle drive buffer	t_{GTISK}*2	-	4	ns	Figure 2.34
		High drive buffer		-	4		
	GTIOCxY output skew (x = 8 to 13, Y = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 2.35
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*3	-	2.0	ns	Figure 2.36
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*4	100	-	ns	Figure 2.37
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.38
KINT	Key interrupt input low width		t_{KR}	250	-	ns	Figure 2.39

Note 1. t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 2. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 3. The load is 30 pF.
Note 4. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

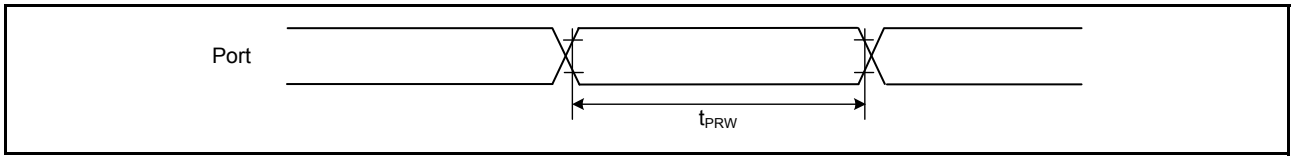

Figure 2.31 I/O ports input timing

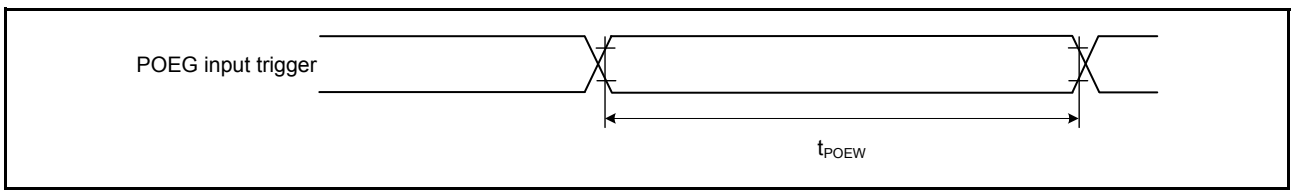

Figure 2.32 POEG input trigger timing

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

2.3.10 SCI Timing

Table 2.22 SCI timing (1)
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK9. For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Item			Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.40
		Clock synchronous		6	-		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	-	5	ns	
	Input clock fall time		t_{SCKf}	-	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous		4	-		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	-	5	ns	
	Output clock fall time		t_{SCKf}	-	5	ns	
	Transmit data delay	Clock synchronous	t_{TXD}	-	25	ns	Figure 2.41
	Receive data setup time	Clock synchronous	t_{RXS}	15	-	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

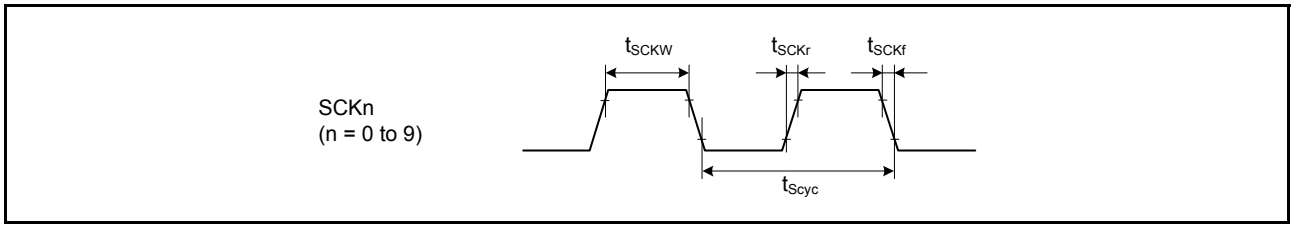

Figure 2.40 SCK clock input/output timing

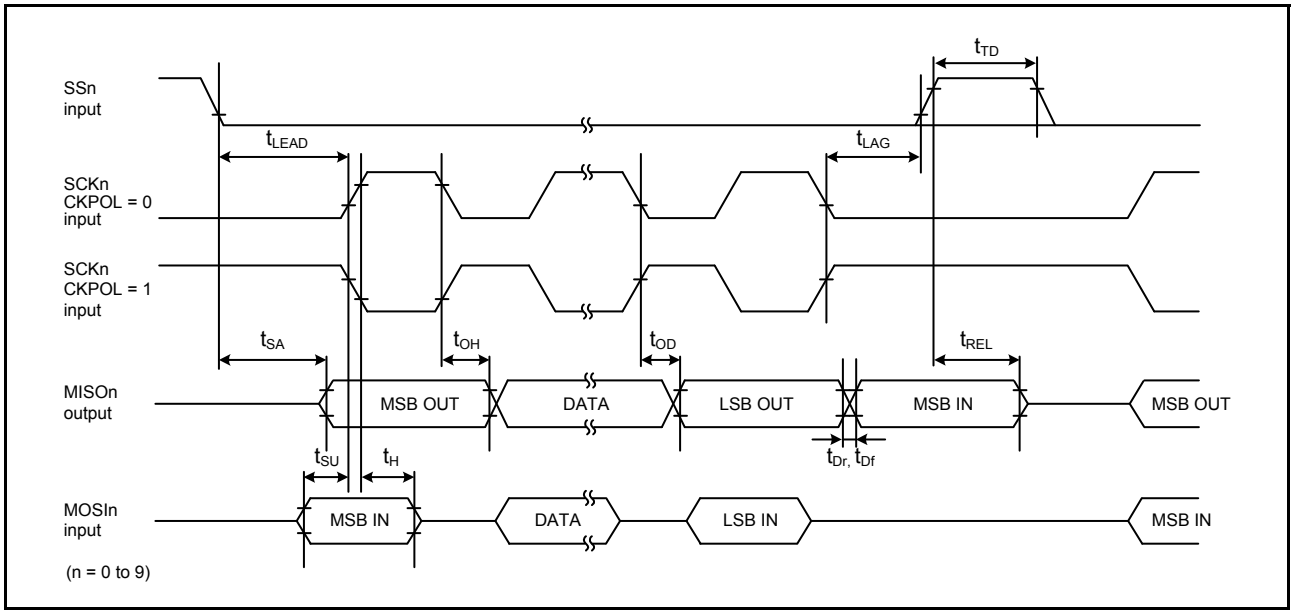

Figure 2.45 SCI simple SPI mode timing for slave when CKPH = 1

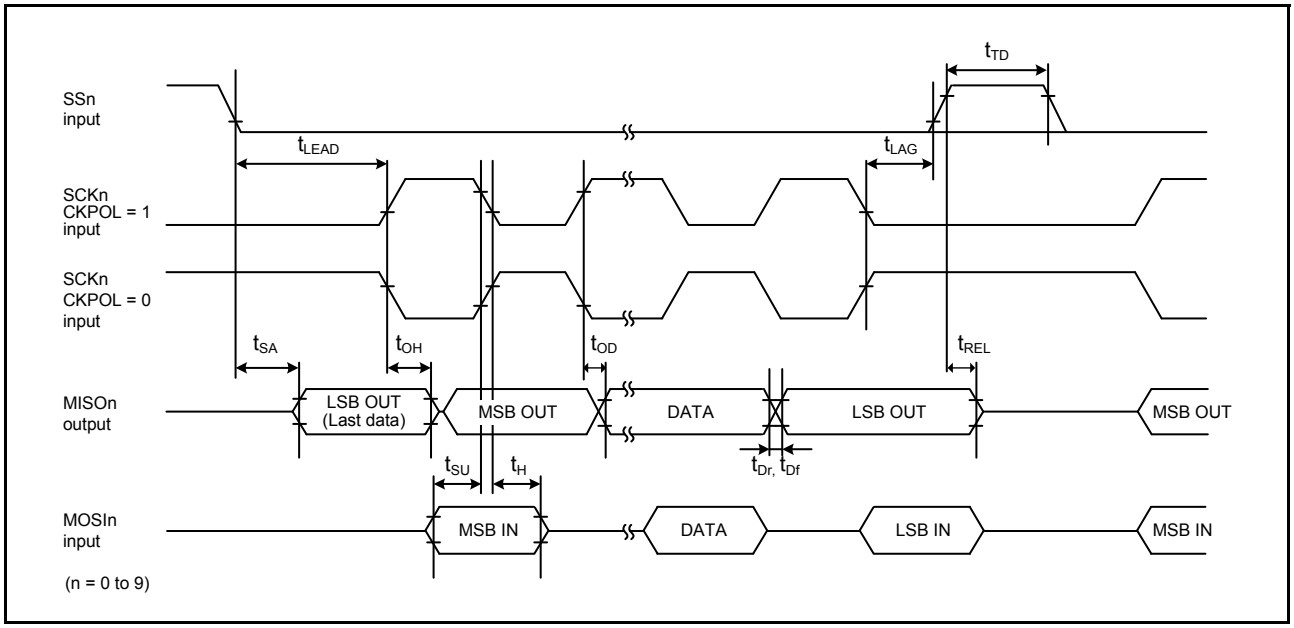

Figure 2.46 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1 of 2)
Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.47
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

2.3.14 SSIE Timing

Table 2.29 SSIE timing

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Item			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCK0	Cycle	Master	t_O	80	-	ns	Figure 2.58
		Slave	t_I	80	-	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	Rising time/falling time	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK0/SSIFS0, SSITXD0, SSIRXD0, SSIDATA0	Input set up time	Master	t_{SR}	12	-	ns	Figure 2.60, Figure 2.61
		Slave		12	-	ns	
	Input hold time	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.60, Figure 2.61
	Output delay time from SSILRCK0/SSIFS0 change	Slave	t_{DTRW}	-	20	ns	Figure 2.62*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 2.59
	High level/ low level		t_{EXL}/ t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA0 pin.

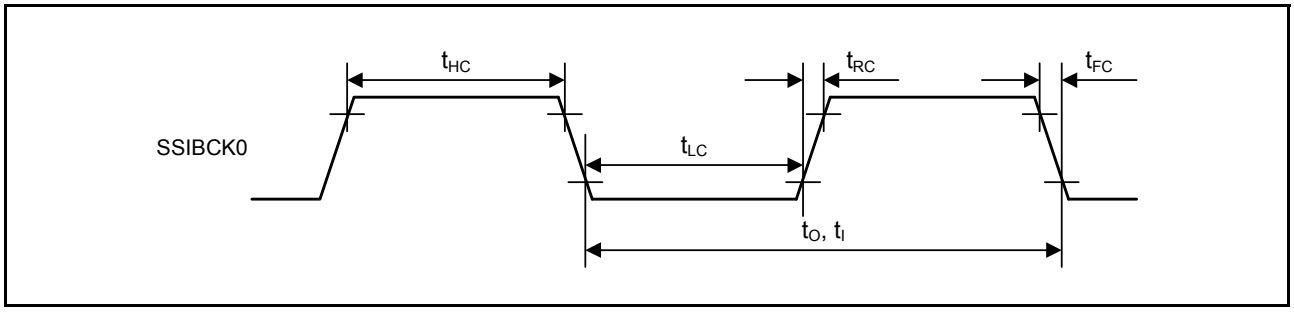

Figure 2.58 SSIE clock input/output timing

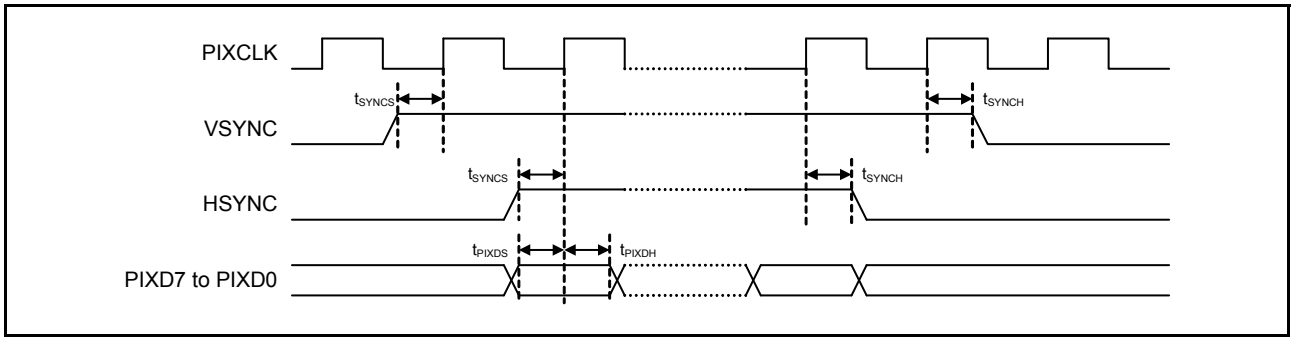

Figure 2.76 PDC AC timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.33 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.77
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

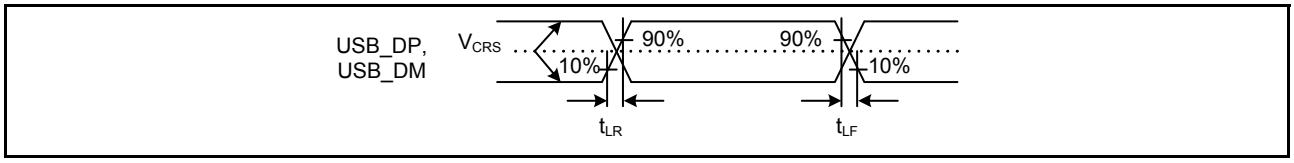

Figure 2.77 USB_DP and USB_DM output timing in low-speed mode

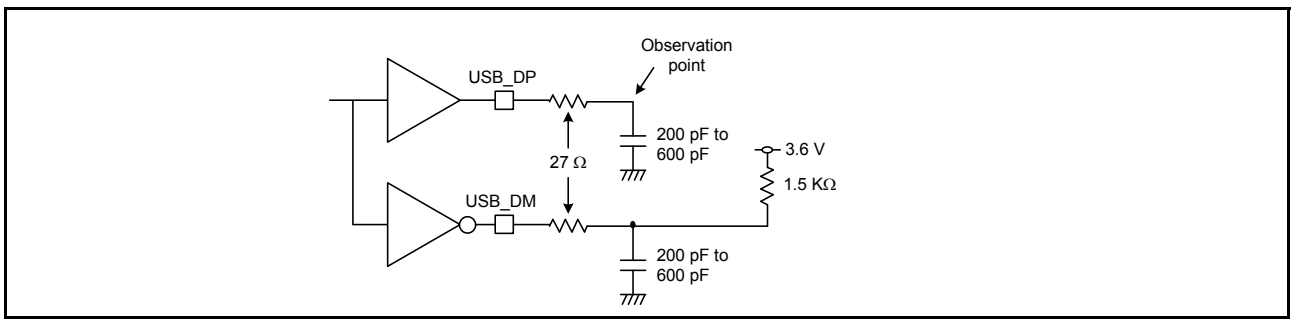

Figure 2.78 Test circuit in low-speed mode

Table 2.34 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.79
	Rise time	t_{LR}	4	-	20	ns	
	Fall time	t_{LF}	4	-	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	-	1.575	kΩ	During idle state
			1.425	-	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

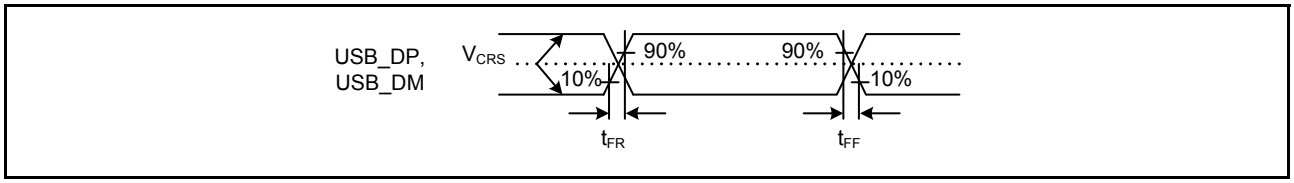

Figure 2.79 USB_DP and USB_DM output timing in full-speed mode

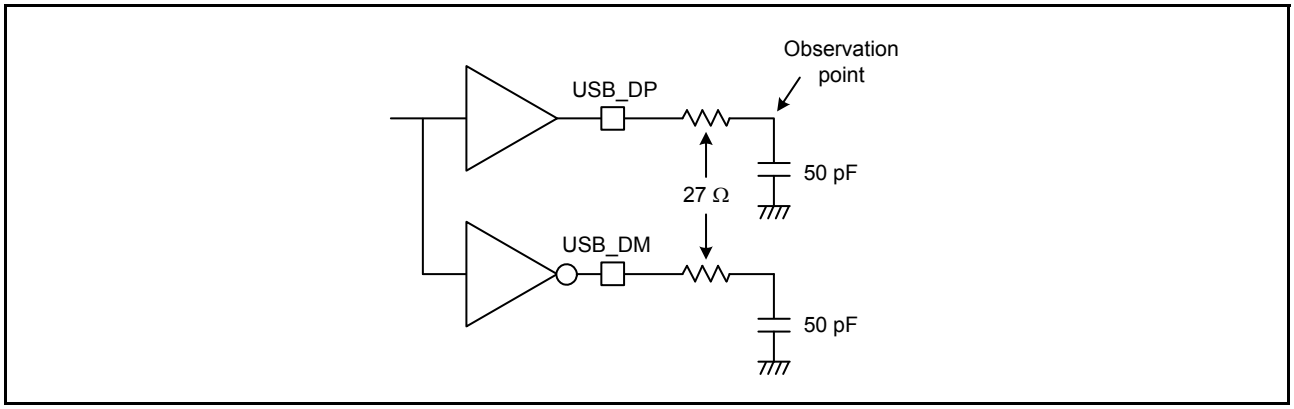

Figure 2.80 Test circuit in full-speed mode

2.5 ADC12 Characteristics

[Normal-precision channel]

Table 2.35 A/D conversion characteristics for unit 0 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Item	Min	Typ	Max	Unit	Test conditions
Frequency	1	-	60	MHz	-
Analog input capacitance	-	-	30	pF	-

Table 2.42 Power-on reset circuit and voltage detection circuit characteristics (2 of 2)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Minimum VCC down time*1	t_{VOFF}	200	-	-	µs	Figure 2.83, Figure 2.84
Response delay	t_{det}	-	-	200	µs	Figure 2.83 to Figure 2.86
LVD operation stabilization time (after LVD is enabled)	$t_{d(E-A)}$	-	-	10	µs	Figure 2.85, Figure 2.86
Hysteresis width (LVD1 and LVD2)	V_{LVH}	-	70	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for POR and LVD.
Note 2. The low power function is disabled and DEEPCUT[1:0] = 00b or 01b.
Note 3. The low power function is enabled and DEEPCUT[1:0] = 11b.

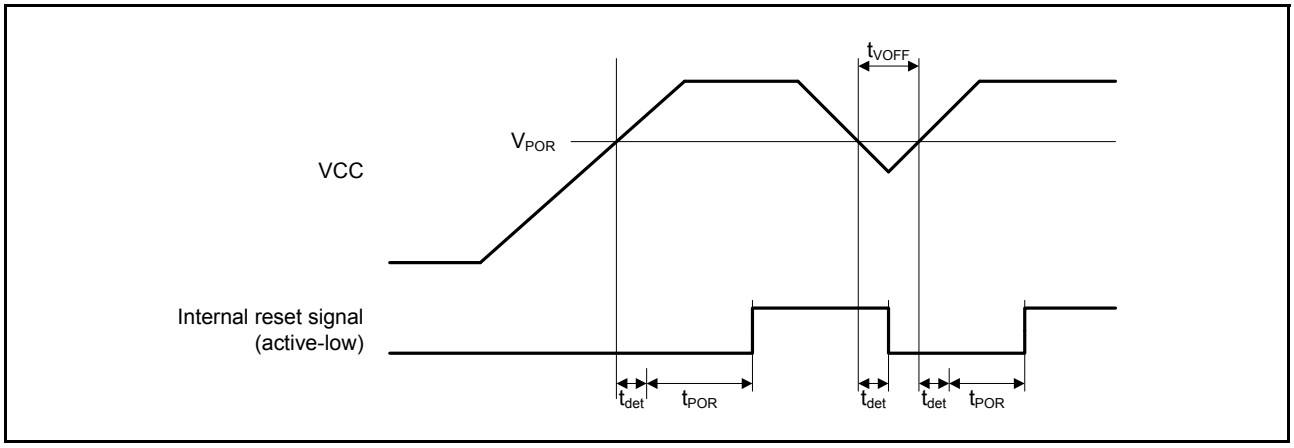

Figure 2.83 Power-on reset timing

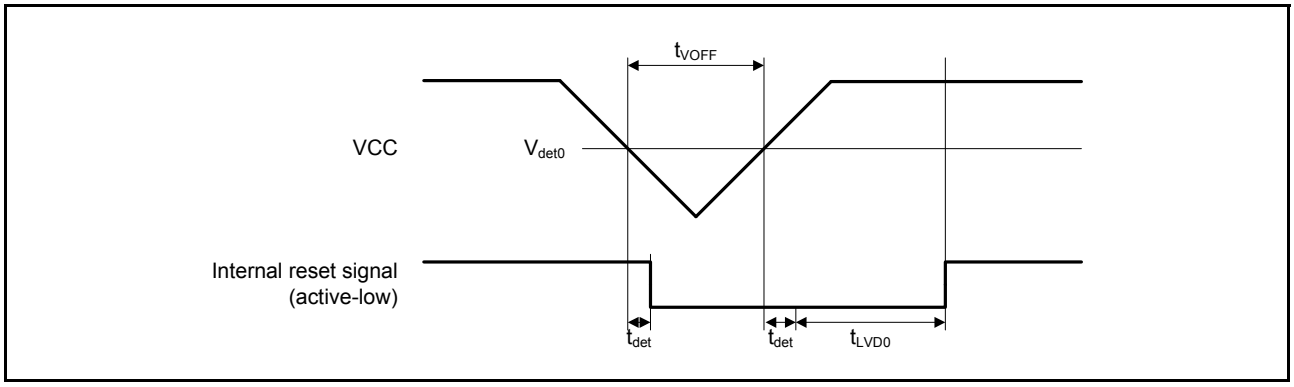

Figure 2.84 Voltage detection circuit timing (V_{det0})

2.15 Joint European Test Action Group (JTAG)

Table 2.49 JTAG

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	-	-	ns	Figure 2.89
TCK clock high pulse width	t_{TCKH}	15	-	-	ns	
TCK clock low pulse width	t_{TCKL}	15	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	8	-	-	ns	Figure 2.90
TMS hold time	t_{TMSH}	8	-	-	ns	
TDI setup time	t_{TDIS}	8	-	-	ns	
TDI hold time	t_{TDIH}	8	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	20	ns	

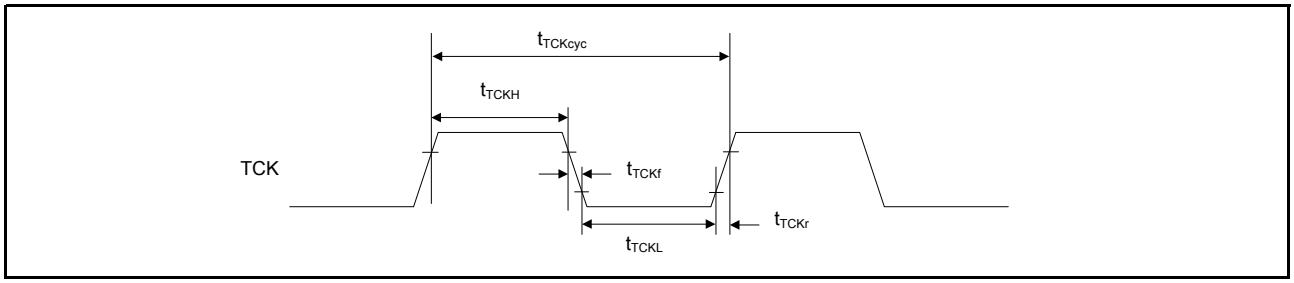

Figure 2.92 JTAG TCK timing

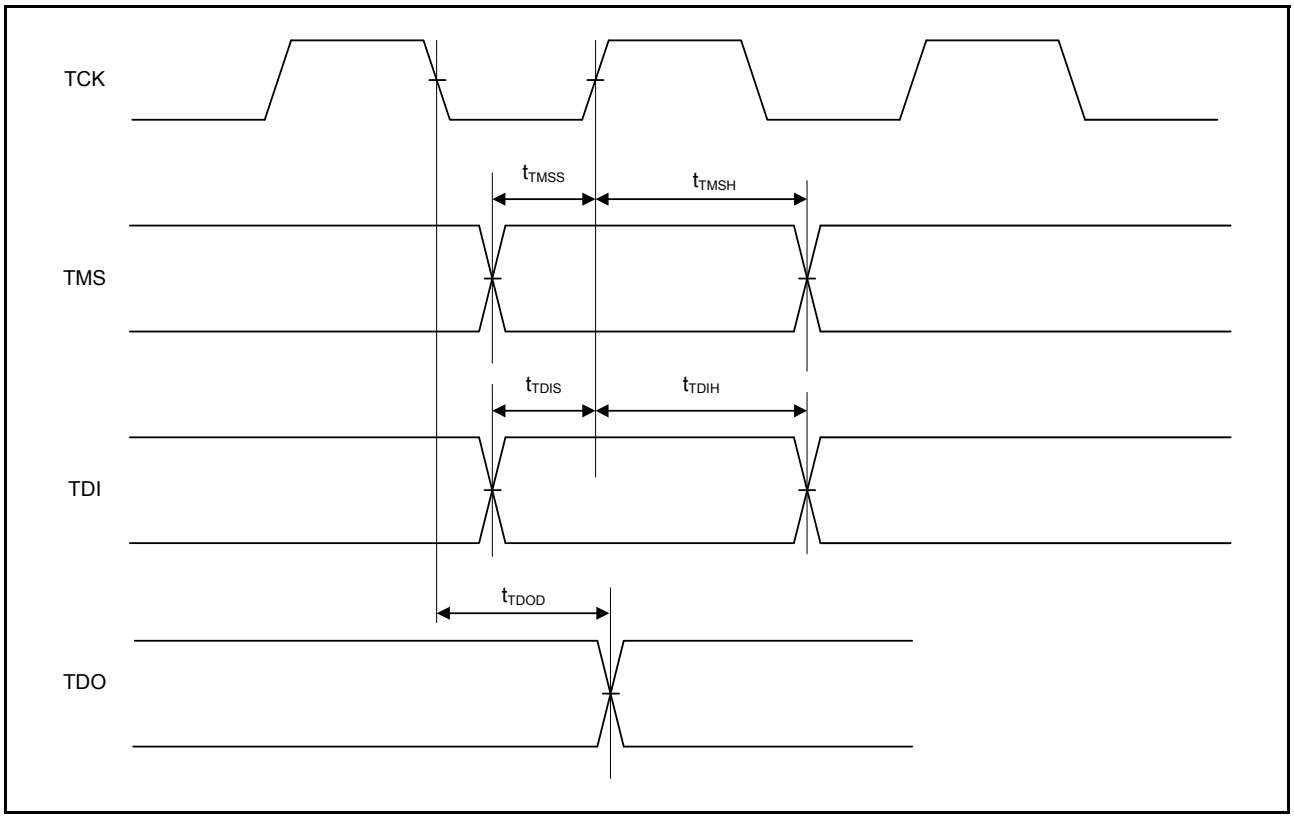

Figure 2.93 JTAG input/output timing

2.16 Serial Wire Debug (SWD)

Table 2.50 SWD

Item	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	-	-	ns	Figure 2.94
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 2.95
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	

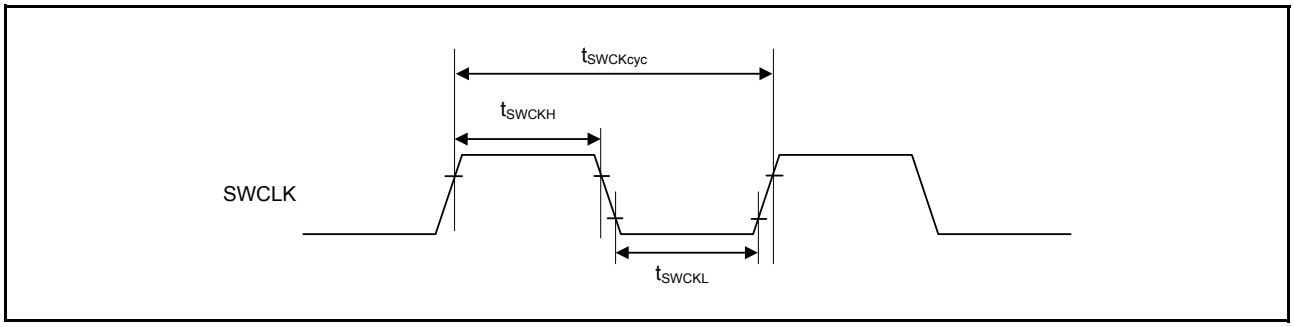

Figure 2.94 SWD SWCLK timing

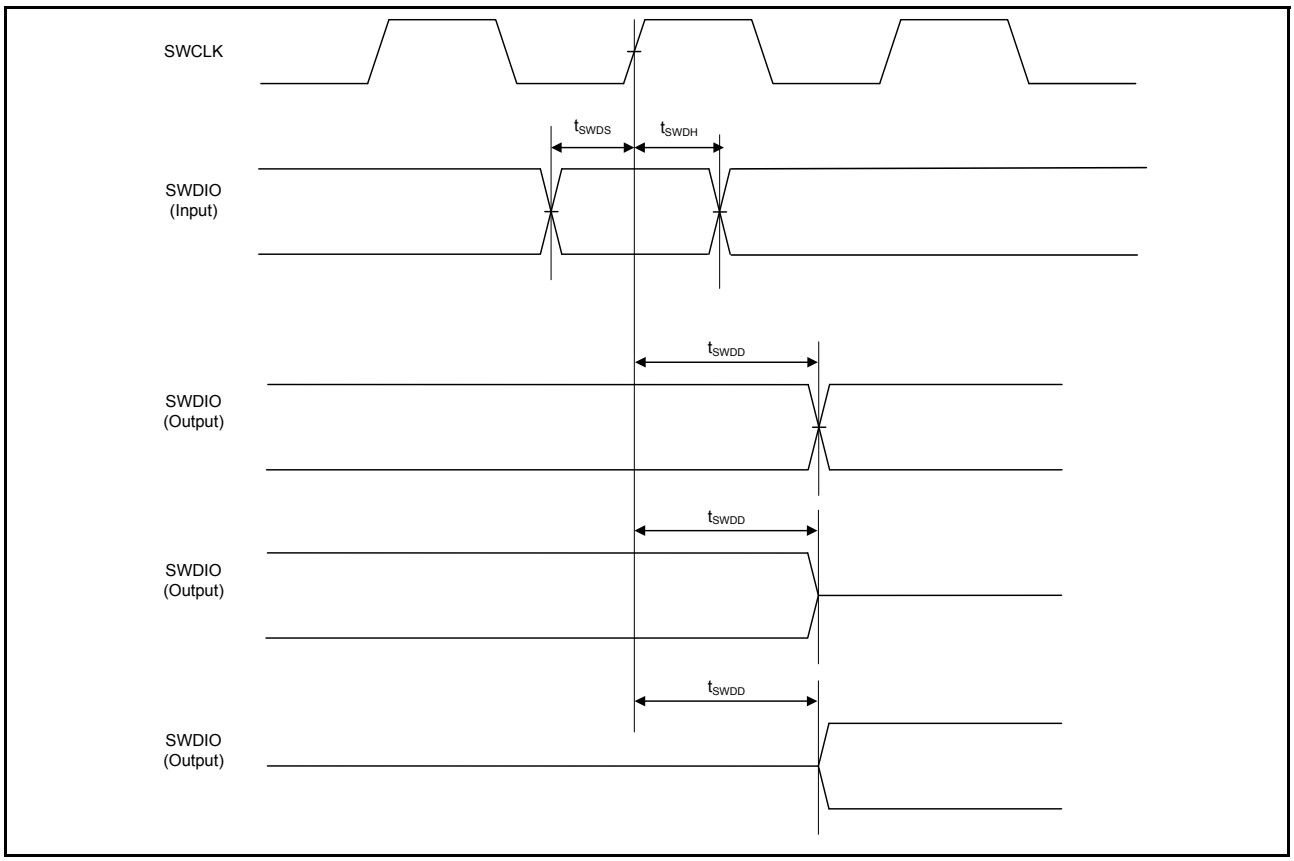

Figure 2.95 SWD input/output timing

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