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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	744kB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56720ag

2 Electrical Characteristics

2.1 Maximum Ratings

Table 2 shows the maximum ratings.

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{DD}). The suggested value for a pull-up or pull-down resistor is 4.7 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	–0.3 to + 1.26	V
	V_{PLLP_VDD}, V_{IO_VDD}, V_{PLLA_VDD},	–0.3 to + 4.0	V
Maximum CORE_VDD power supply ramp time[3]	Tr	10	ms
Input Voltage per pin excluding VDD and GND	V_{IN}	GND –0.3 to 5.5 V	V
Current drain per pin excluding V_{DD} and GND (Except for pads listed below)	I	12	mA
LSYNC_OUT	I_{lsync_out}	16	mA
LCLK	I_{lclk}	16	mA
LALE	I_{ale}	16	mA
TDO	I_{JTAG}	24	mA
Operating temperature range	T_J	–40 to +100	°C

2.4 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f \qquad \textit{Eqn. 1}$$

where C=node/pin capacitance
V=voltage swing
f=frequency of node/pin toggle

Example 1. Power Consumption Example

For a GPIO address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 150 MHz clock, toggling at its maximum possible rate (75 MHz), the current consumption is

$$I = 50x10^{-12}x3.3x75x10^{6} = 12.375mA \qquad \textit{Eqn. 2}$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (for example, to compensate for measured board current not caused by the DSP). Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$\mathbf{I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)} \qquad \textit{Eqn. 3}$$

where : I_{typF2}=current at F2
I_{typF1}=current at F1
F2=high frequency (any specified operating frequency)
F1=low frequency (any specified operating frequency lower than F2)

NOTE

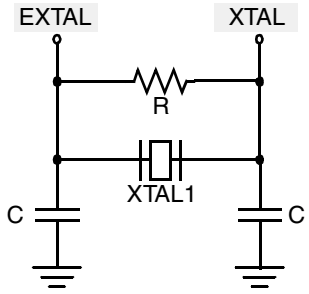
F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

2.5 DC Electrical Characteristics

Table 4 shows the DC electrical characteristics.

Table 4. DC Electrical Characteristics

	Characteristics	Symbol	Min	Typ	Max	Unit
Commercial	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.9	1	1.1	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Automotive	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.95	1	1.05	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Note: To avoid a high current condition and possible system damage, all 3.3 V supplies must rise before the 1.0 V supplies rise.						
Input low voltage		V_{IL}	–0.3	—	0.8	V
Input leakage current		I_{IN}	—	—	± 84	µA
Clock pin Input Capacitance (EXTAL)		C_{IN}	—	18	—	pF
High impedance (off-state) input current (@ 3.3 V or 0 V)		I_{TSI}	–10	—	10	µA
Output high voltage I_{OH} = -12 mA LSYNC_OUT, LALE, LCLK Pins I_{OH} = -16 mA, TDO Pin I_{OH} = -24 mA		V_{OH}	2.4	—	—	V
Output low voltage I_{OL} = 12 mA LSYNC_OUT, LALE, LCLK Pins I_{OL} = 16 mA, TDO Pins I_{OL} = 24 mA		V_{OL}	—	—	0.4	V
Internal pull-up resistor		R_{PU}	64	92	142	kΩ
Internal pull-down resistor		R_{PD}	57	90	157	kΩ
Commercial	Internal supply current[1] (core only) at internal clock of 200 MHz					
	• In Normal mode	I_{CCI}	—	224	445	mA
	• In Wait mode	I_{CCW}	—	121	353	mA
	• In Stop mode[2]	I_{CCS}	—	90	327	mA



Suggested component values:

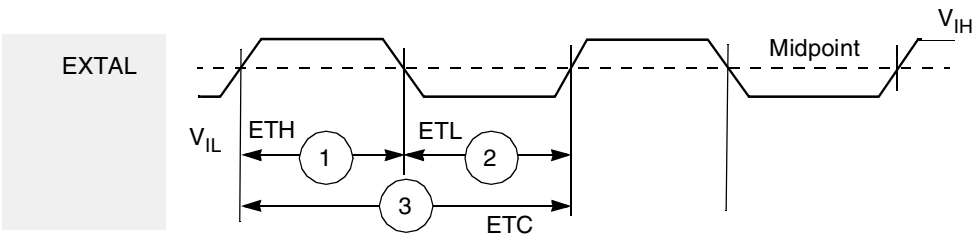
Fosc = 24.576 MHz
R = 1 M ±10%
C (EXTAL)= 18 pF
C (XTAL) = 18 pF

Calculations are for a 5 – 30 MHz crystal with the following parameters:

- Shunt capacitance (C_0) of 10 pF – 12 pF
- Series resistance 40 Ohm
- Drive level of 10 µW

Figure 9. Using the On-Chip Oscillator

If the DSP56720/DSP56721 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 10). When the external square wave source is connected to EXTAL, the XTAL pin is not used.



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 10. External Clock Timing

Table 6 lists the clock operation.

Table 6. Clock Operation

No.	Characteristics	Symbol	Min	Max	Units
1	EXTAL input high [1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Eth	 16.67 2.5	 100 inf	ns
2	EXTAL input low[1] (40% to 60% duty cycle) • Crystal oscillator • Square wave input	Etl	 16.67 2.5	 100 inf	ns
3	EXTAL cycle time • With PLL disabled • With PLL enabled	Etc	 5 33.3	 inf 500	ns
4	Instruction cycle time • With PLL disabled • With PLL enabled	Tc	 5.00 5.00	 inf 5120	ns

Notes:

1. Measured at 50% of the input transition.
2. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.9 Reset, Stop, Mode Select, and Interrupt Timing

Table 7 shows the reset, stop, mode select, and interrupt timing.

Table 7. Reset, Stop, Mode Select, and Interrupt Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled	 $2 \times T_C$ $2 \times T_C$	 10 10	 — —	 ns ns
13	Syn reset deassert delay time • Minimum • Maximum (PLL enabled)	 $2 \times T_C$ $(2 \times T_C) + T_{LOCK}$	 10 200	 — —	 ns us
14	Mode select setup time	—	10.0	—	ns
15	Mode select hold time	—	12	—	ns
16	Minimum edge-triggered interrupt request assertion width	—	7	—	ns
17	Minimum edge-triggered interrupt request deassertion width	—	4	—	ns
18	Delay from interrupt trigger to interrupt code execution	$10 \times T_{C+4}$	54	—	ns
19	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[1, 2, 3] • PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0) • PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1) • PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0) • PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	 $(128\ \text{Kbytes} \times T_C)$ $25 \times T_C$ $(128\ \text{Kbytes} \times T_C) + T_{LOCK}$ $(25 \times T_C) + T_{LOCK}$	 655 125 855 200	 — — — —	 µs ns µs µs
20	• Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution[1]	$10 \times T_C + 3.8$	—	53.8	ns
21	Interrupt Requests Rate[1] • ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1, Timer, Timer_1 • DMA • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger) • $\overline{\text{IRQ}}$ (level trigger)	 $12 \times T_C$ $8 \times T_C$ $8 \times T_C$ $12 \times T_C$	 — — — —	 60.0 40.0 40.0 60.0	 ns ns ns ns

Table 7. Reset, Stop, Mode Select, and Interrupt Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$6 \times T_C$	—	30.0	ns
	• Data write to ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$7 \times T_C$	—	35.0	ns
	• Timer, Timer_1	$2 \times T_C$	—	10.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$3 \times T_C$	—	15.0	ns

Notes:

1. When using fast interrupts and when $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, if using an external clock (PCTL Bit 13 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.
   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shut down during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 200 µs.
3. Periodically sampled and not 100% tested.
4. $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When V_{DD} is valid, but the other "required $\overline{RESET}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

Figure 11 shows the reset timing diagram.

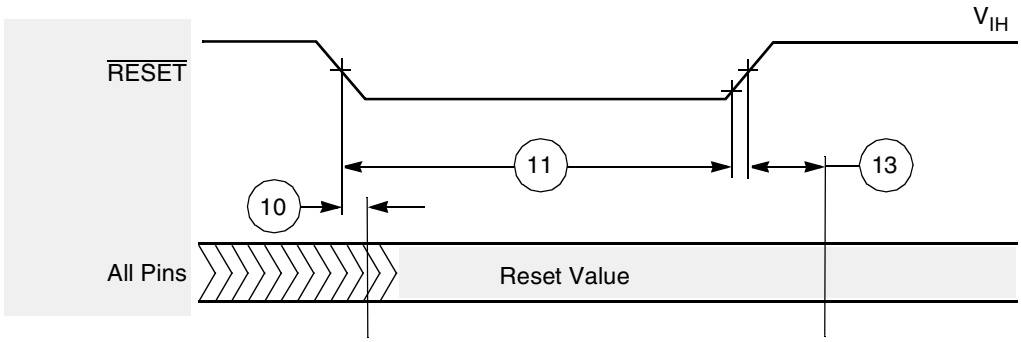


Figure 11. Reset Timing Diagram

Table 8. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	$3.0 \times T_C + 30$	—	45	ns
			Very Narrow	$3.0 \times T_C + 95$	—	110	ns
			Narrow	$3.0 \times T_C + 120$	—	135	ns
			Wide	$3.0 \times T_C + 210$	—	225	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	$2.0 \times T_C$	10	—	ns
			Very Narrow	$2.0 \times T_C + 5$	15	—	ns
			Narrow	$2.0 \times T_C + 45$	55	—	ns
			Wide	$2.0 \times T_C + 95$	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	14.0	ns
36	First SCK sampling edge to $\overline{HREQ}$ output deassertion	Slave	Bypassed	$3.0 \times T_C + 30$	45	—	ns
			Very Narrow	$3.0 \times T_C + 40$	55	—	ns
			Narrow	$3.0 \times T_C + 80$	95	—	ns
			Wide	$3.0 \times T_C + 130$	145	—	ns
37	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted (CPHA = 1)	Slave	Bypassed	$4.0 \times T_C + 30$	50.0	—	ns
			Very Narrow	$4.0 \times T_C + 40$	60.0	—	ns
			Narrow	$4.0 \times T_C + 80$	100.0	—	ns
			Wide	$4.0 \times T_C + 130$	150.0	—	ns
38	$\overline{SS}$ deassertion to $\overline{HREQ}$ output not deasserted (CPHA = 0)	Slave	—	$3.0 \times T_C + 30$	45.0	—	ns
39	$\overline{SS}$ deassertion pulse width (CPHA = 0)	Slave	—	$2.0 \times T_C$	10.0	—	ns
40	$\overline{HREQ}$ in assertion to first SCK edge	Master	Bypassed	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Very Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	111.5	—	ns
			Wide	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	206.5	—	ns

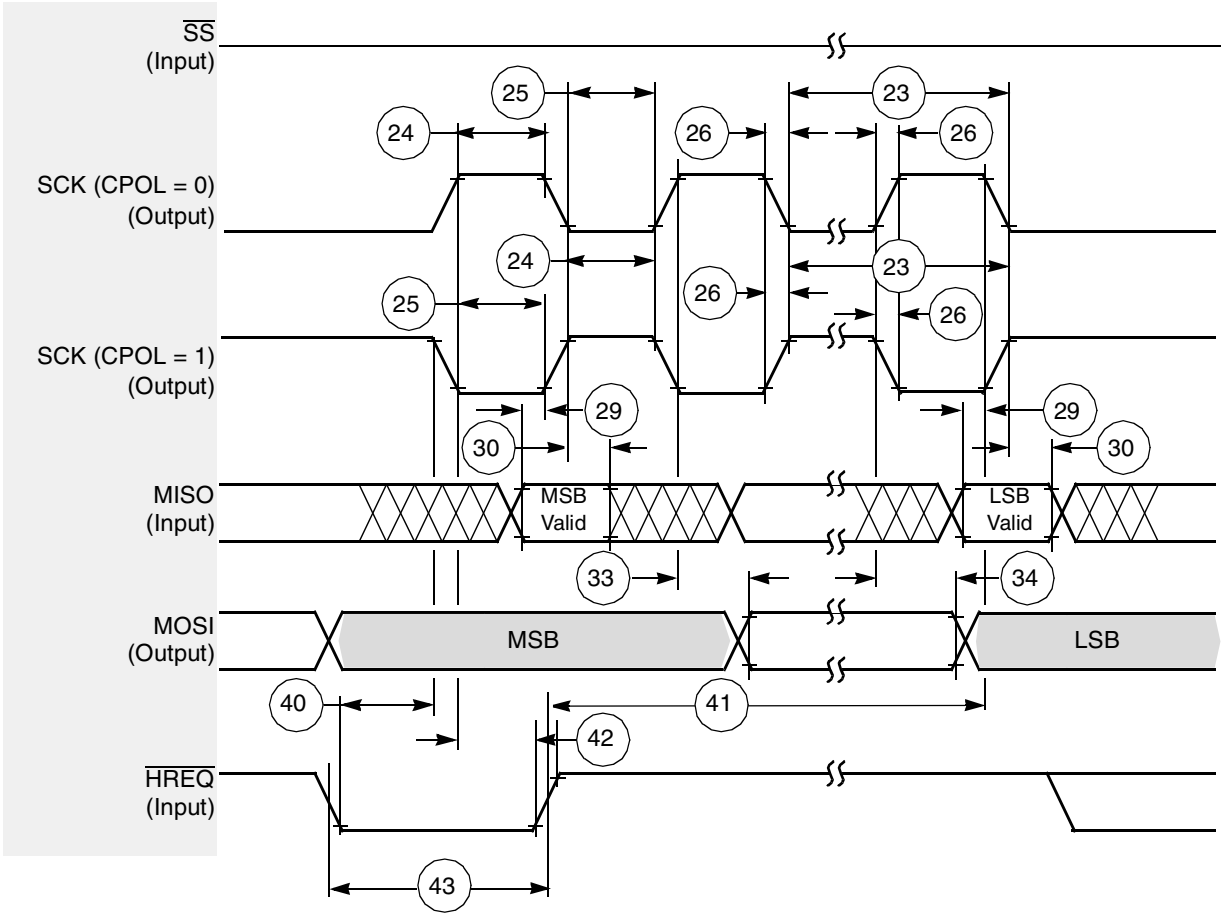


Figure 16. SPI Master Timing Diagram (CPHA = 1)

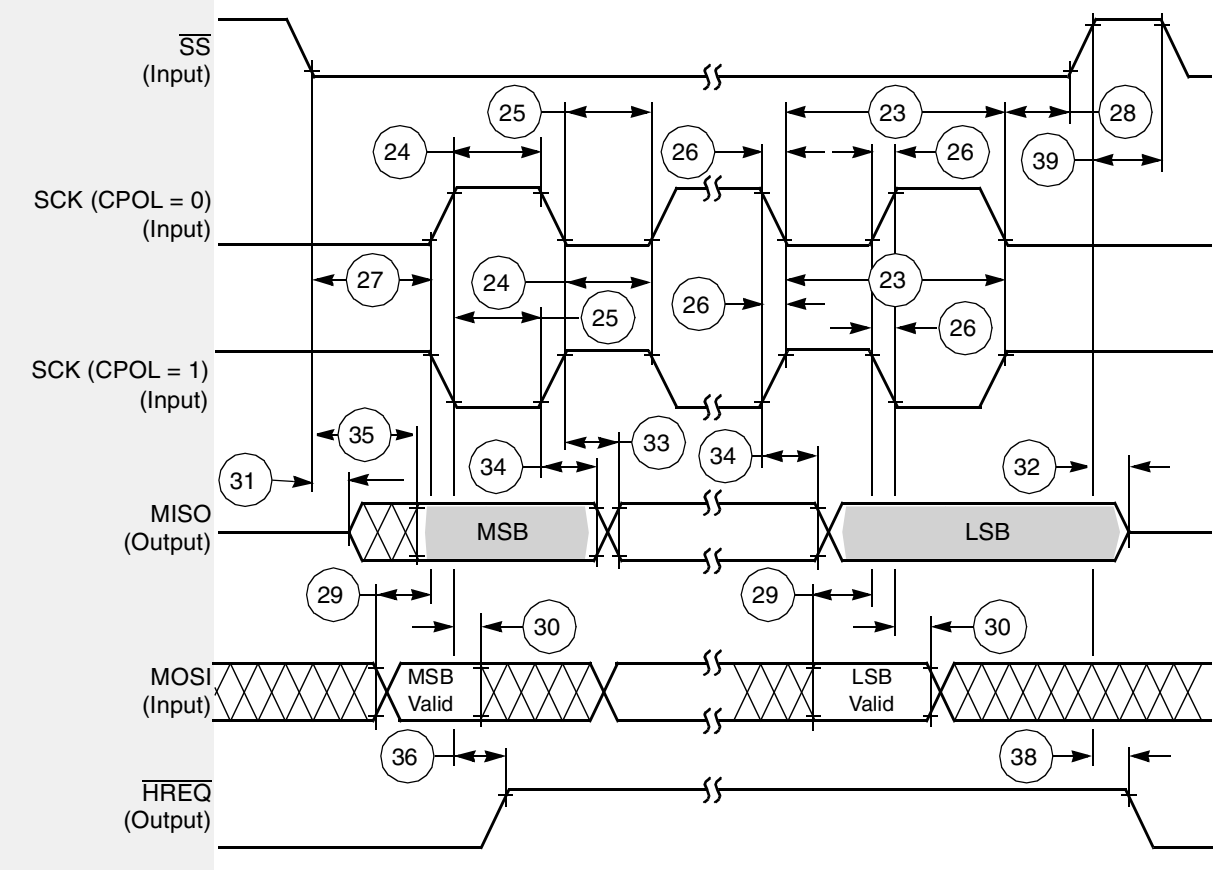


Figure 17. SPI Slave Timing Diagram (CPHA = 0)

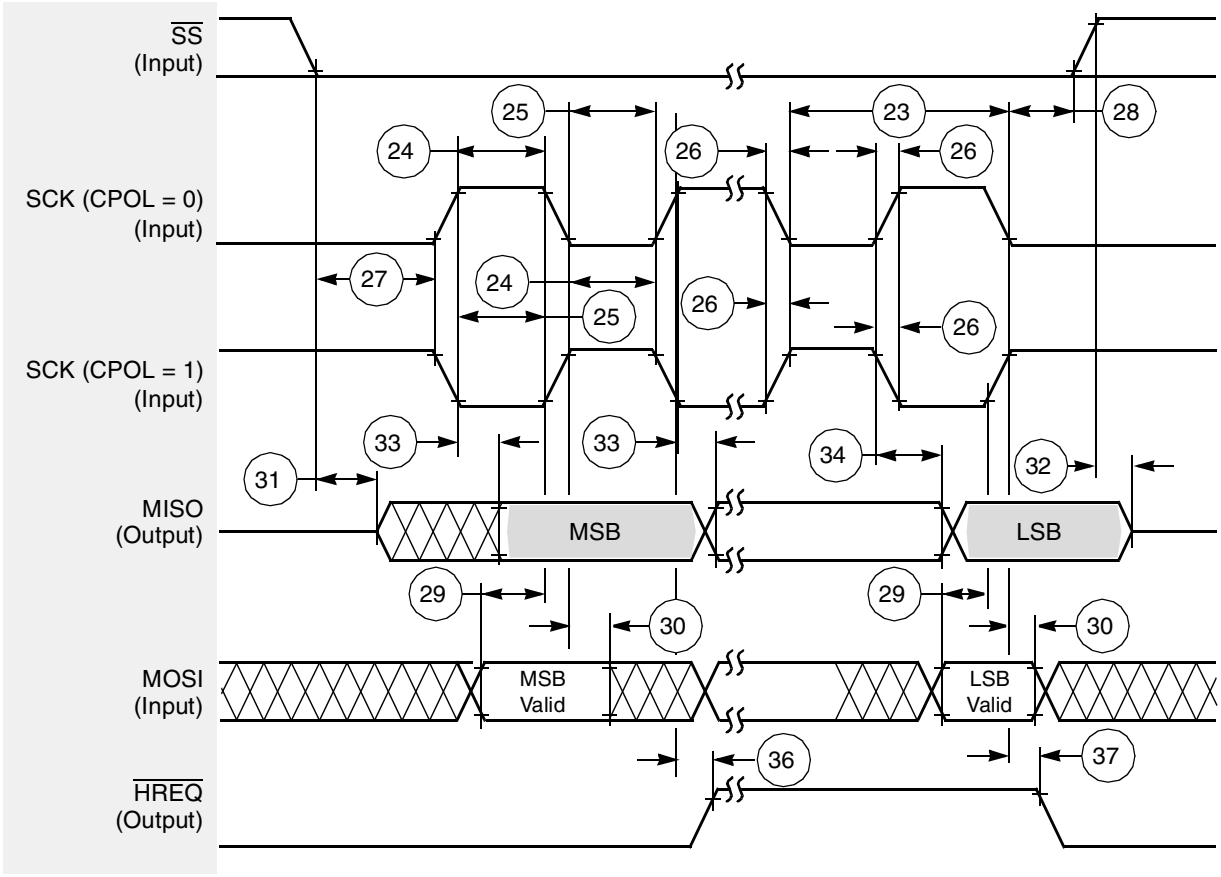


Figure 18. SPI Slave Timing Diagram (CPHA = 1)

2.11 Serial Host Interface (SHI) I²C Protocol Timing

Table 9 lists the SHI I²C protocol timing parameters and Figure 19 shows the timing diagram.

Table 9. SHI I²C Protocol Timing Parameters

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	—	 — — — —	 0 10 50 100	 — — — —	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs

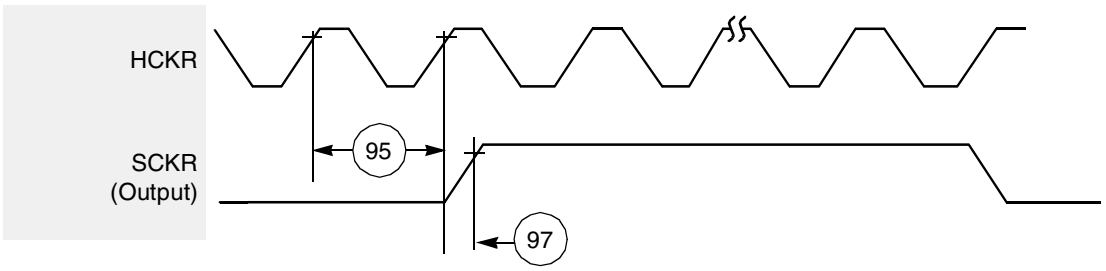


Figure 23. ESAI HCKR Timing

2.14 Timer Timing

Table 11 lists the timer timing parameters and Figure 24 shows the timing diagram.

Table 11. Timer Timing Parameters

No.	Characteristics	Expression			Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	12.0	—	ns
99	TIO High	$2 \times T_C + 2.0$	12.0	—	ns

Notes:
1. V_{CORE_VDD} = 1.00 V ± 0.10 V; T_J = –40°C to 100°C, C_L = 50 pF
2. TIMER_1 specs match those of TIMER

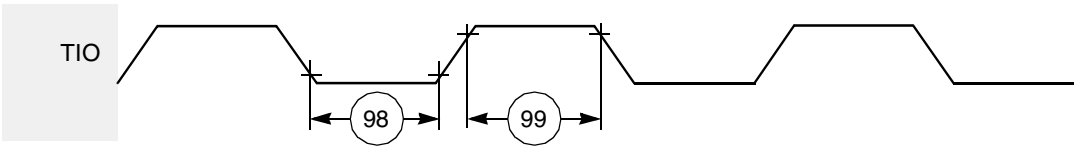


Figure 24. TIO Timer Event Input Restrictions Diagram

2.15 GPIO Timing

Table 12 lists the general purpose input and output (GPIO) timing and Figure 25 shows the timing diagram.

Table 12. GPIO Timing Parameters

No.	Characteristics[1]	Expression	Min	Max	Unit
100	Fsys edge to GPIO out valid (GPIO out delay time)[2]	—	—	7	ns
101	Fsys edge to GPIO out not valid (GPIO out hold time)[2]	—	—	7	ns
102	Fsys In valid to EXTAL edge (GPIO in set-up time)[2]	—	2	—	ns
103	Fsys edge to GPIO in not valid (GPIO in hold time)[2]	—	0	—	ns
104	Minimum GPIO pulse high width	2 × TC	10	—	ns

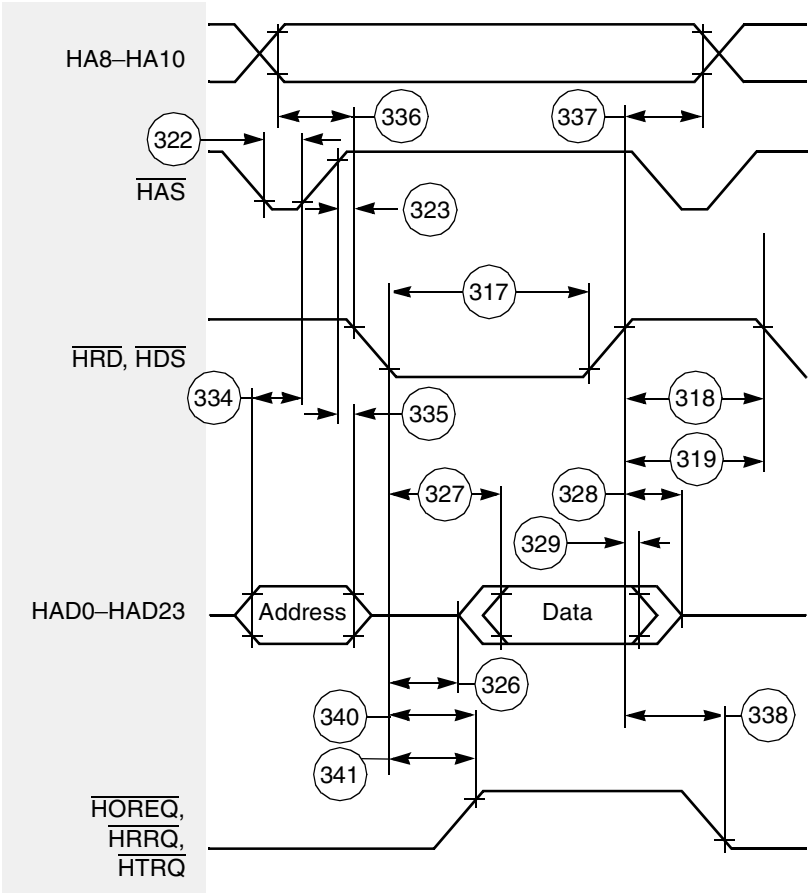


Figure 32. HDI24 Read Timing Diagram, Multiplexed Bus

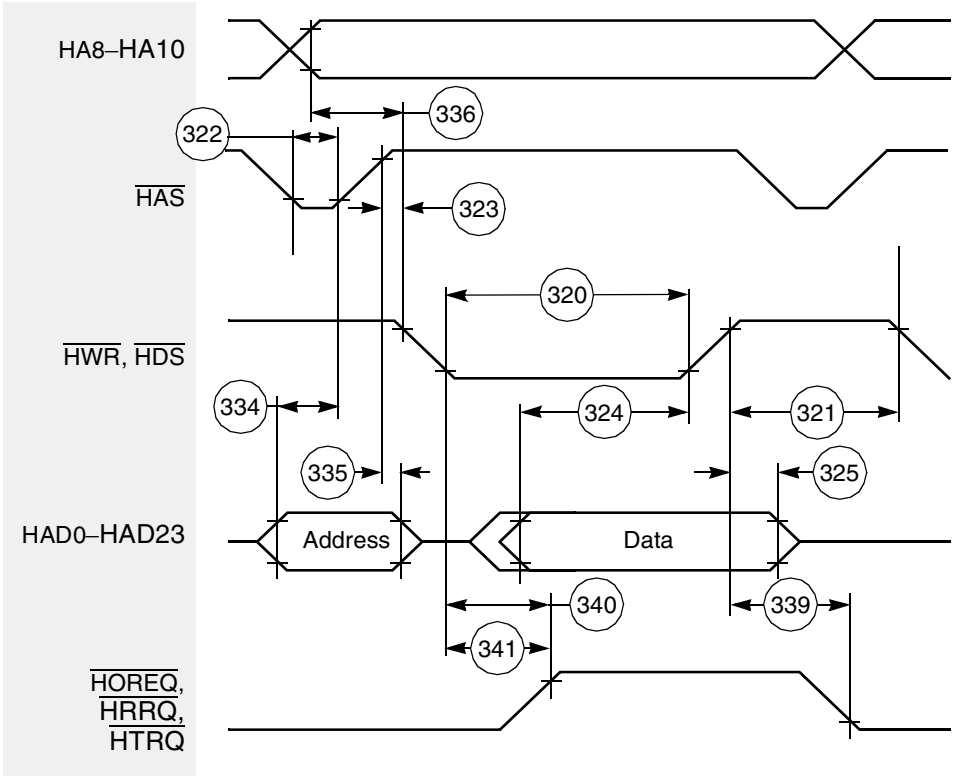


Figure 33. HDI24 Write Timing Diagram, Multiplexed Bus

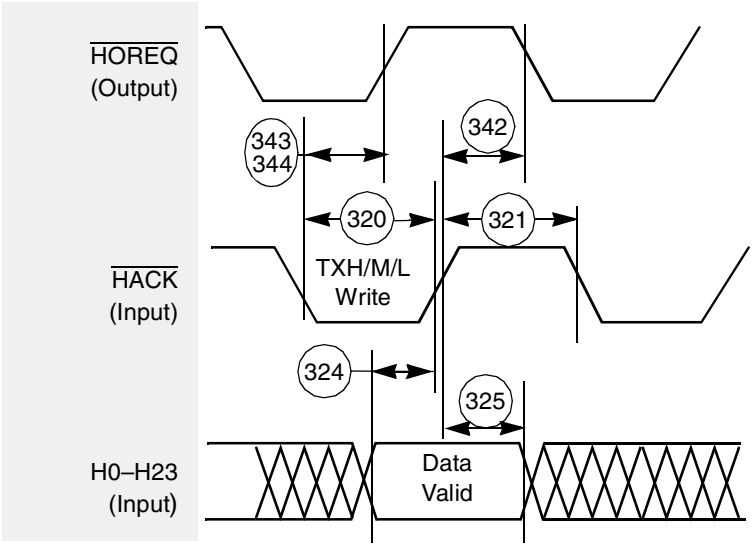


Figure 34. HDI24 Host DMA Write Timing Diagram

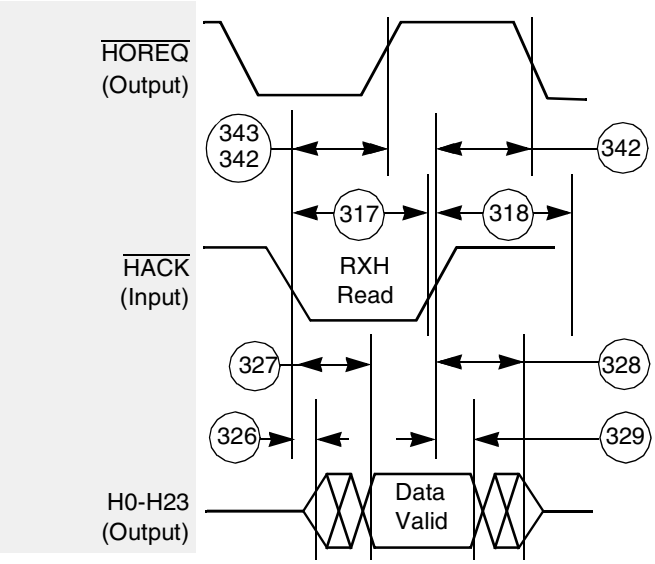


Figure 35. HDI24 Host DMA Read Timing Diagram

2.19 S/PDIF Timing

Table 16 lists the Sony/Philips Digital Interconnect Format (S/PDIF) timing parameters and Figure 36 and Figure 37 show the timing diagrams.

Table 16. S/PDIF Timing Parameters

Characteristics	Symbol	All Frequency		Unit
		Min	Max	
SPDIFIN1, SPDIFIN2, SPDIFIN3, SPDIFIN4 Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT1,SPDIFOUT2 output (Load = 50 pf) • Skew • Transition Risng • Transition Falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1, SPDIFOUT2 output (Load = 30 pf) • Skew • Transition Risng • Transition Falling	 — — —	 — — —	 1.5 13.6 18.0	ns
SRCK period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
STCLK period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

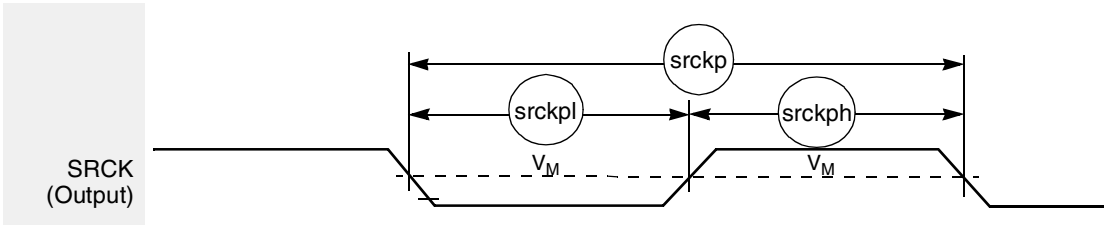


Figure 36. S/PDIF SRCK Timing Diagram

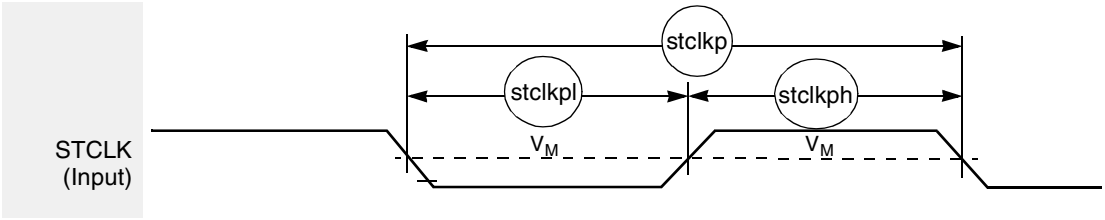


Figure 37. S/PIDF STCLK Timing Diagram

2.20 EMC Timing (DSP56720 Only)

The DSP56721 device does not have an EMC module. For EMC timing parameters in DSP56720 devices, see Table 17, through Table 19; for timing diagrams, see Figure 38 through Figure 40.

Table 17. EMC Timing Parameters (EMC PLL Enabled; LCRR[CLKDIV] = 2)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	10	—	ns
LCLK skew to LSYNC_OUT	T_{clk_skew}	—	160	ps
Input setup to LSYNC_IN (except $\overline{\text{LGTA}}$/LUPWAIT)	T_{in_s}	3	—	ns
Input hold from LSYNC_IN (except $\overline{\text{LGTA}}$/LUPWAIT)	T_{in_h}	2	—	ns
$\overline{\text{LGTA}}$ valid time	T_{gta}	12	—	ns
LUPWAIT valid time	T_{upwait}	12	—	ns
LALE negedge to LAD(address phase) invaild (address latch hold time)	T_{ale_h}	3	—	ns
LALE valid time	T_{ale}	3.8	—	ns
Output setup from LSYNC_IN (except LAD[23:0] and LALE)	T_{out_s}	4	—	ns
Output hold from LSYNC_IN (except LAD[23:0] and LALE)	T_{out_h}	2	—	ns
LAD[23:0] output setup from LSYNC_IN	T_{ad_s}	3.5	—	ns
LAD[23:0] output hold from LSYNC_IN	T_{ad_h}	1.5	—	ns
LSYNC_IN to output high impedance for LAD[23:0]	T_{ad_z}	—	4.3	ns

Chapter 22, “External Memory Controller (EMC),” in the *Symphony DSP56720/DSP56721 Multi-Core Audio Processors Reference Manual* explains in detail the interfacing and features of EMC. The applicable sections are as follows:

- Section 22.4.4.3, “UPM Signal Timing”
- Section 22.4.4.7, “Memory System Interface Example Using UPM”

Table 19. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8) (Continued)

Parameter	Symbol	Min	Max	Unit
LAD[23:0] output setup from LCLK	T_{ad_s}	12	—	ns
LAD[23:0] output hold from LCLK	T_{ad_h}	17	—	ns
LCLK to output high impedance for LAD[23:0]	T_{ad_z}	—	17.1	ns

Notes:
1. A negative hold time means that the signal could be invalid before the LCLK rising edge.

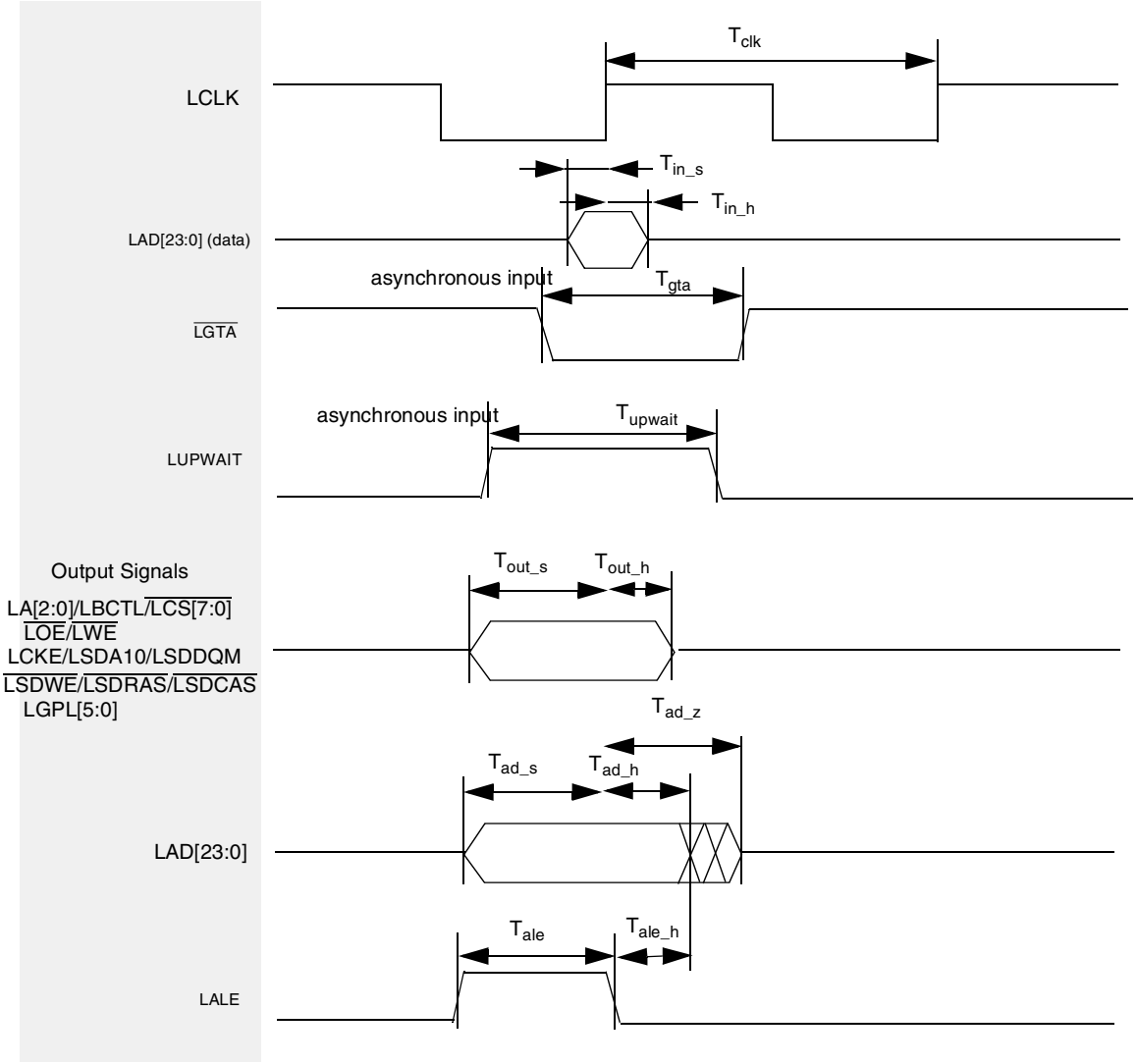


Figure 40. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

3 Functional Description and Application Information

See the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manual* (DSP56720RM) for detailed functional and applications information.

4 Ordering Information

Table 20 provides ordering information for both the DSP56720 and DSP56721.

Table 20. Ordering Information

Device	Device Marking	Ambient Temp.	LQFP Package
DSP56720 Commercial	DSPA56720AG	0°C–70°C	20 mm × 20 mm
	DSPB56720AG	0°C–70°C	20 mm × 20 mm
	DSPC56720AG	0°C–70°C	20 mm × 20 mm
DSP56720 Automotive	DSPA56720CAG	–40°C–85°C	20 mm × 20 mm
	DSPB56720CAG	–40°C–85°C	20 mm × 20 mm
	DSPC56720CAG	–40°C–85°C	20 mm × 20 mm
DSP56721 Commercial	DSPA56721AG	0°C–70°C	20 mm × 20 mm
	DSPB56721AG	0°C–70°C	20 mm × 20 mm
	DSPC56721AG	0°C–70°C	20 mm × 20 mm
	DSPA56721AF	0°C–70°C	14 mm × 14 mm
	DSPB56721AF	0°C–70°C	14 mm × 14 mm
	DSPC56721AF	0°C–70°C	14 mm × 14 mm
DSP56721 Automotive	DSPA56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPB56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPC56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPA56721CAF	–40°C–85°C	14 mm × 14 mm
	DSPB56721CAF	–40°C–85°C	14 mm × 14 mm
	DSPC56721CAF	–40°C–85°C	14 mm × 14 mm

5 Package Information

For the outline drawings of available device packages, see Table 21 and sections 5.1–5.2.

Table 21. Package Outline Drawings

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52
DSP56721	80-pin plastic LQFP	Figure 43 on page 51 and Figure 42 on page 50
	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52

Figure 44. 144-Pin Package Outline Drawing (2 of 2)

NOTES

1. All dimensinos are in millimeters
2. Interpret dimensions and tolerances per ASME Y14.5M-1994.
3. Datums B, C and D to be determined at datum plane H.
4. The top ppackage body size may be smaller than the bottom package size by a maximum of 0.1 mm.
5. These dimensions do not include mold protrusions. The maximum allowable protrusion is 0.25 mm per side. These dimensions are maximum body size dimensions including mold mismatch.
6. This dimension does not include dambar protrusion. Protrusions shall not cause the lead width to exceed 0.35 mm minimum space between protrusion and an adjacent lead shall be 0.07 mm.

7 These dimensions are determined at the seating plane, datum A.

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com. Documentation is available from a local Freescale Semiconductor, Inc. distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

DSP56300 Family Manual (document number DSP56300FM). Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set.

Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manual (document number DSP56720RM). Detailed description of memory, peripherals, and interfaces.

DSP56720 Product Brief (DSP56720PB). Brief description of the DSP56720 device.

DSP56721 Product Brief (DSP56721PB). Brief description of the DSP56721 device.

7 Revision History

Table 22 summarizes revisions to this document.

Table 22. Revision History

Revision	Date	Description
5	02/2009	• Updated values and added Commercial and Automotive columns in Table 4, “DC Electrical Characteristics.” • Updated values in the following tables: Table 7, Table 9, Table 10, Table 11, Table 12, Table 13, Table 15, Table 17, Table 18, and Table 19. • In Table 10, “Enhanced Serial Audio Interface Timing Parameters,” changed value for 87 to “13”. • Added Section 2.4, “Power Consumption Considerations.” • In Section 2.20, “EMC Timing (DSP56720 Only),” added text regarding the EMC chapter and applicable sections. • Added automotive information to Table 20, “Ordering Information.”
4	04/2008	• Added formula for thermal characteristics on page 10. • Added values for pull-up and pull-down resistors on page 12.
3	03/2008	• Updated order information on page 1 to include additional parts with temperature specification.
2	02/2008	• Timing updates.
1	12/2007	• Initial release

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