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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	744kB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56720cag

1 Pin Assignments

DSP56720 devices are available in one package type; DSP56721 devices are available in two package types. For the pin assignments of a specific device in a specific package, refer to Section 1.1, “Pinout for DSP56720 144-Pin Plastic LQFP Package,” through Section 1.3, “Pinout for DSP56721 144-Pin Plastic LQFP Package.”

Table 1. Pin Assignments by Package

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 3 on page 5
DSP56721	80-pin plastic LQFP	Figure 4 on page 6
	144-pin plastic LQFP	Figure 5 on page 7

For more detailed information about signals, refer to the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manuall* (DSP56720RM).

1.2 Pinout for DSP56721 80-Pin Plastic LQFP Package

Figure 4 shows the pinout of the DSP56721 80-pin plastic LQFP package.

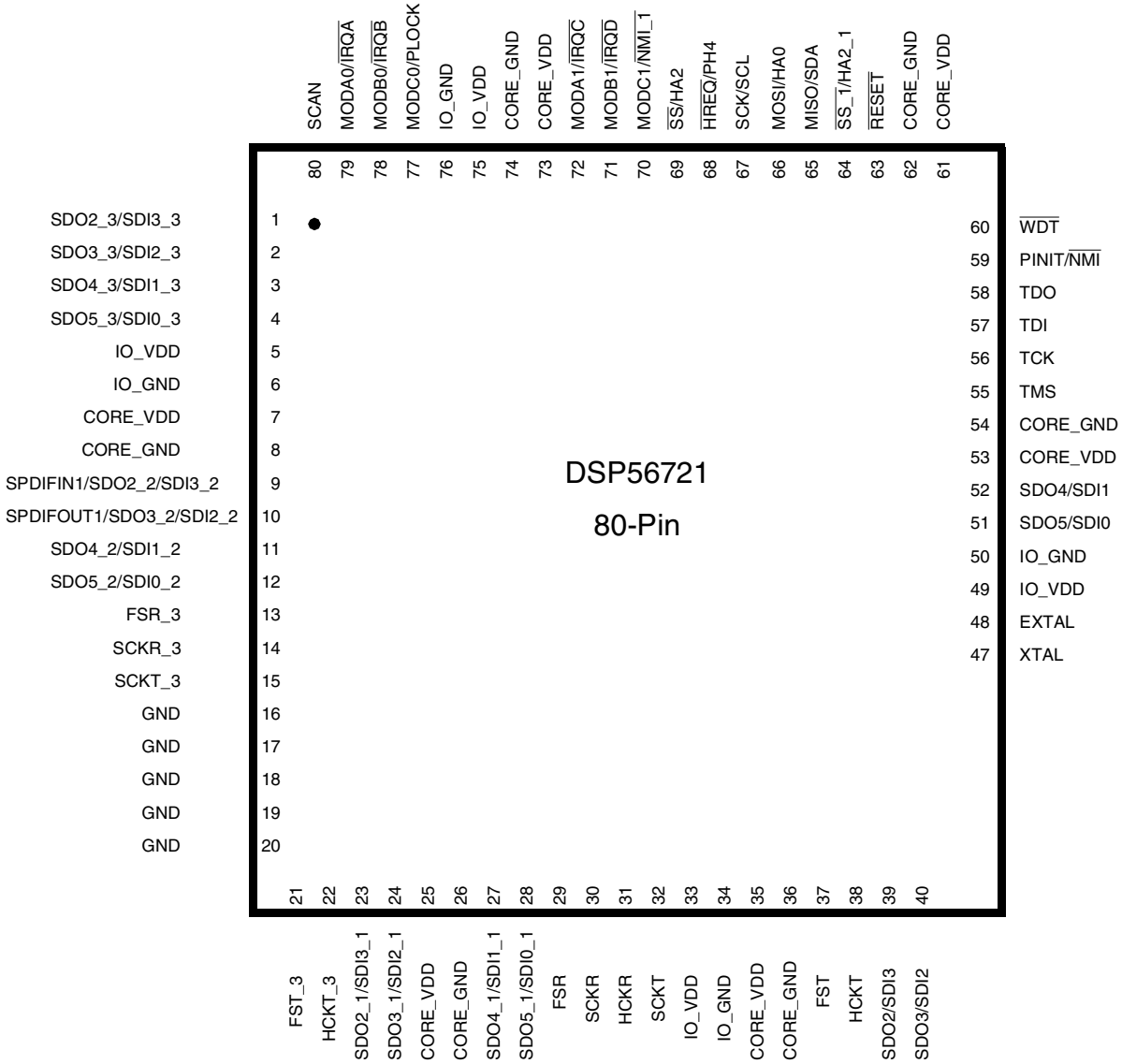

Figure 4. DSP56721 80-Pin Package

1.3 Pinout for DSP56721 144-Pin Plastic LQFP Package

Figure 5 shows the pinout of the DSP56721 144-pin plastic LQFP package.

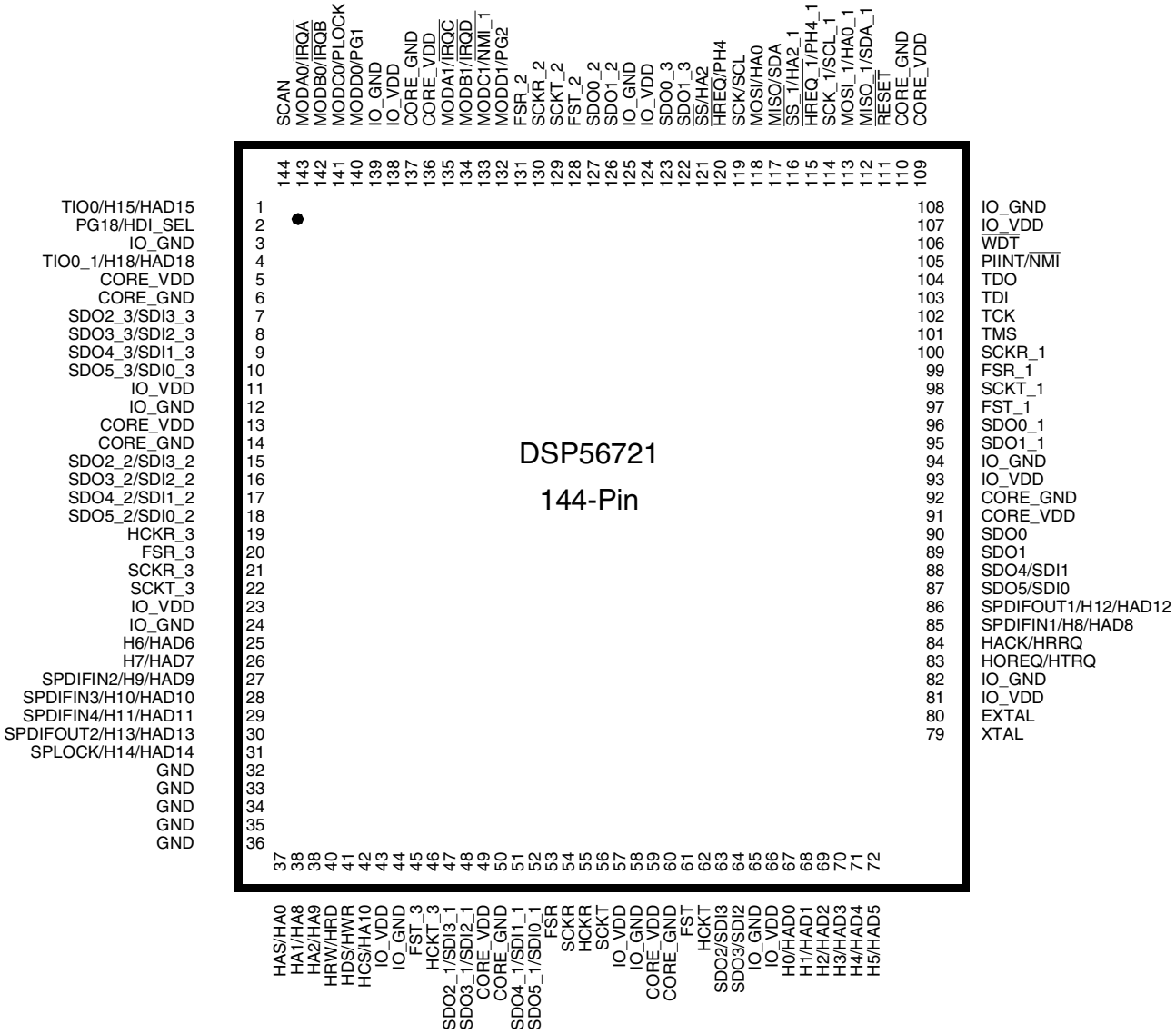

Figure 5. DSP56721 144-Pin Package Pinout

1.4 Pin Multiplexing

Many pins are multiplexed. For more about pin multiplexing, refer to the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manual* (DSP56720RM).

Table 4. DC Electrical Characteristics (Continued)

	Characteristics	Symbol	Min	Typ	Max	Unit
Automotive	• In Normal Mode	I_{CCI}	—	242	496	mA
	• In Wait Mode	I_{CCW}	—	125	409	mA
	• In Stop mode	I_{CCS}	—	107	376	mA
Input capacitance		C_{IN}	—	—	10	pF

Notes:
1. The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CORE_VDD} = 1.0 V, V_{DD_IO} = 3.3 V at T_J = 25° C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.10 V, $V_{IO\_VDD)}$ = 3.4 V at T_J = 100°C.
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

2.6 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56720/DSP56721 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

2.7 Internal Clocks

Internal clock characteristics are listed in Table 5.

Table 5. Internal Clocks

No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
1	Comparison Frequency	Fref	2	—	8	MHz	Fref = Fin/NR
2	Input Clock Frequency	Fin	Max = 200 MHz				—
3	PLL VCO Frequency	Fvco	200	—	400	MHz	Fvco = (Fin × NF)/NR
4	Output Clock Frequency[1] • with PLL enabled • with PLL disabled	Fout	 25 —	—	 200 200	MHz	 Fout= Fvco/NO Fout = Fin
5	Duty Cycle	—	40	50	60	%	Fvco= 200 MHz–400 MHz

Notes:
Fin = External frequency, NF = Multiplication Factor, NR = Predivision Factor, NO = Output Divider

2.8 External Clock Operation

The DSP56720/DSP56721 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; see the example in Figure 9.

Figure 12 shows the external fast interrupt timing diagram.

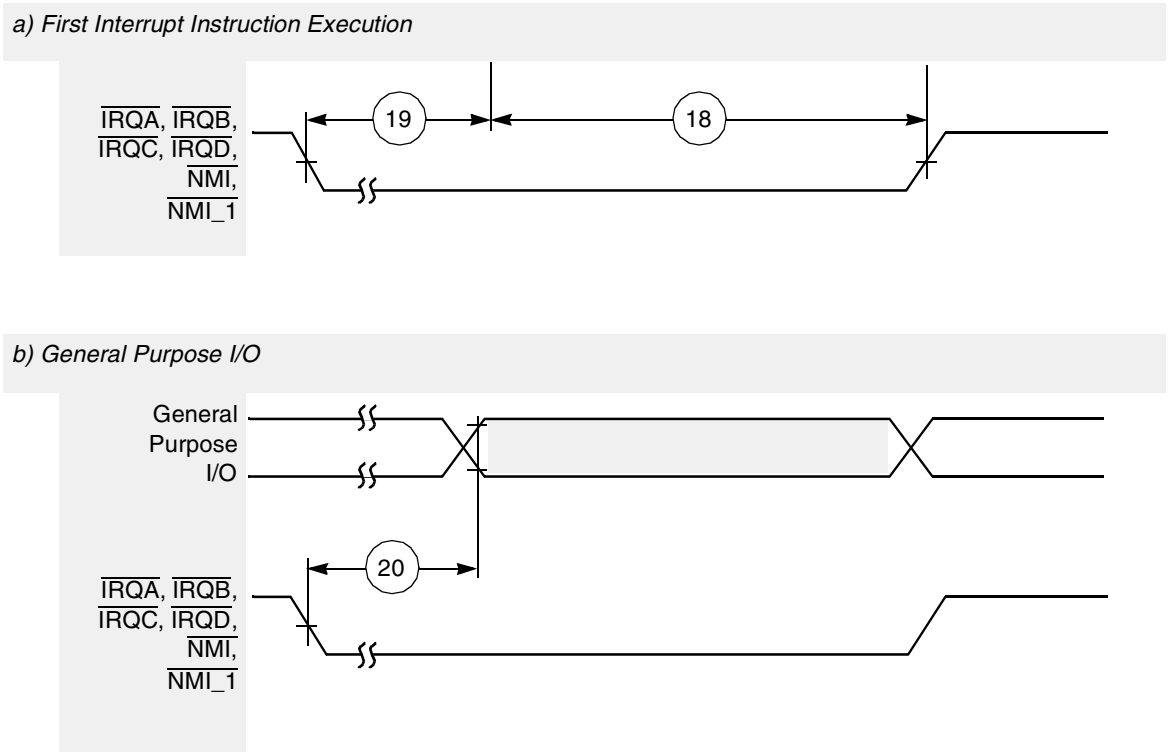

Figure 12. External Fast Interrupt Timing Diagram

Figure 13 shows the negative edge-triggered external interrupt timing diagram.

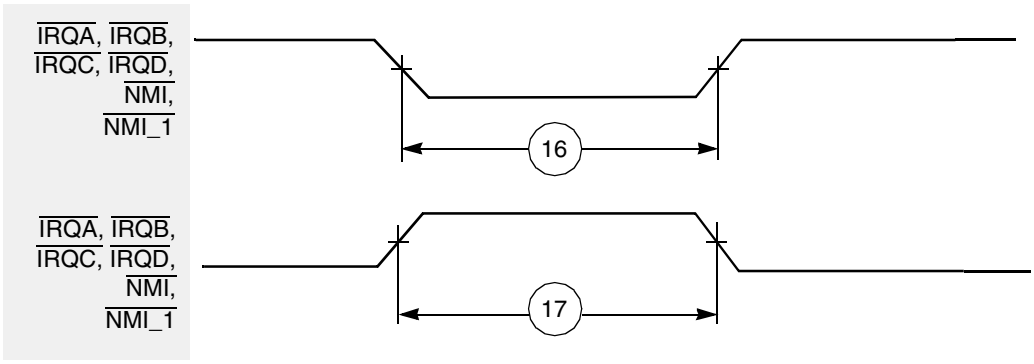

Figure 13. External Interrupt Timing Diagram (Negative Edge-Triggered)

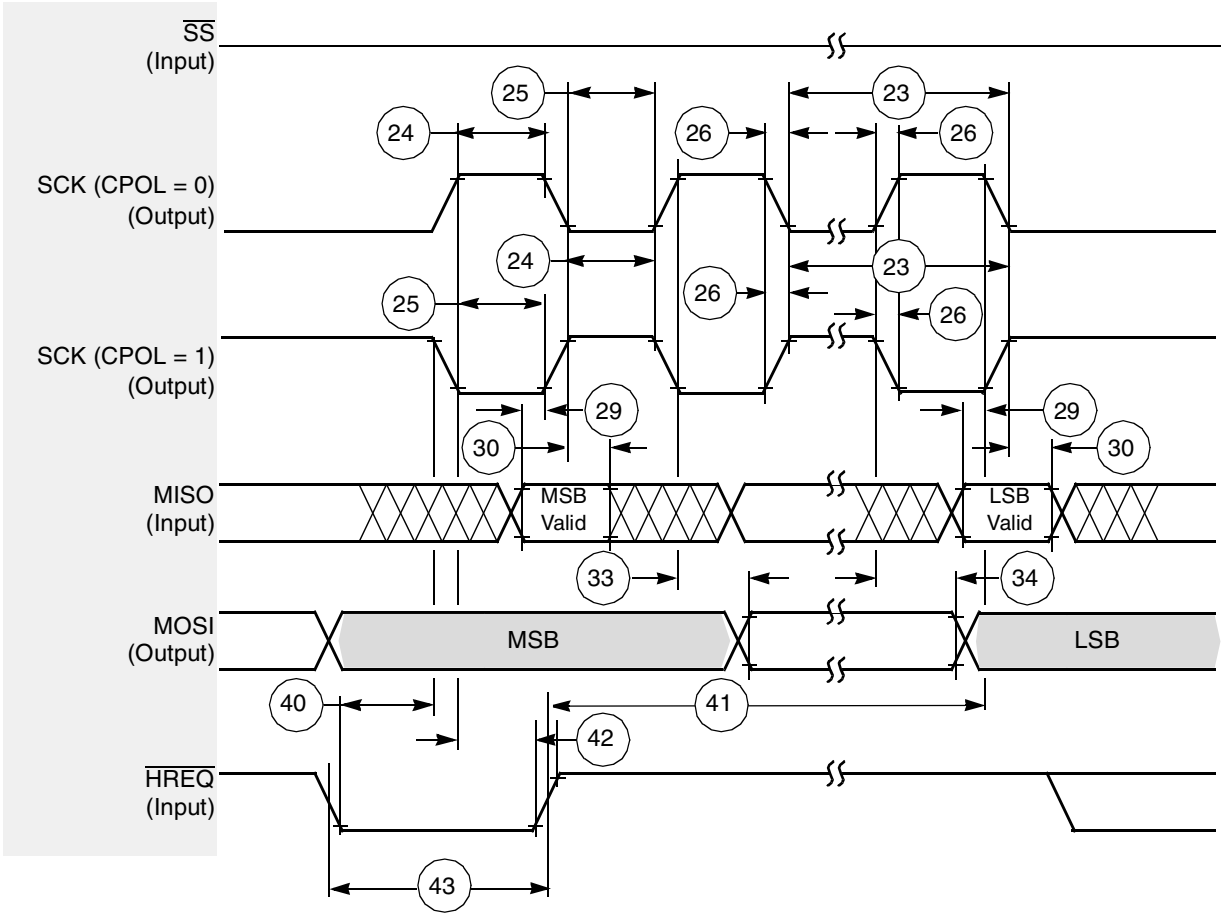

Figure 16. SPI Master Timing Diagram (CPHA = 1)

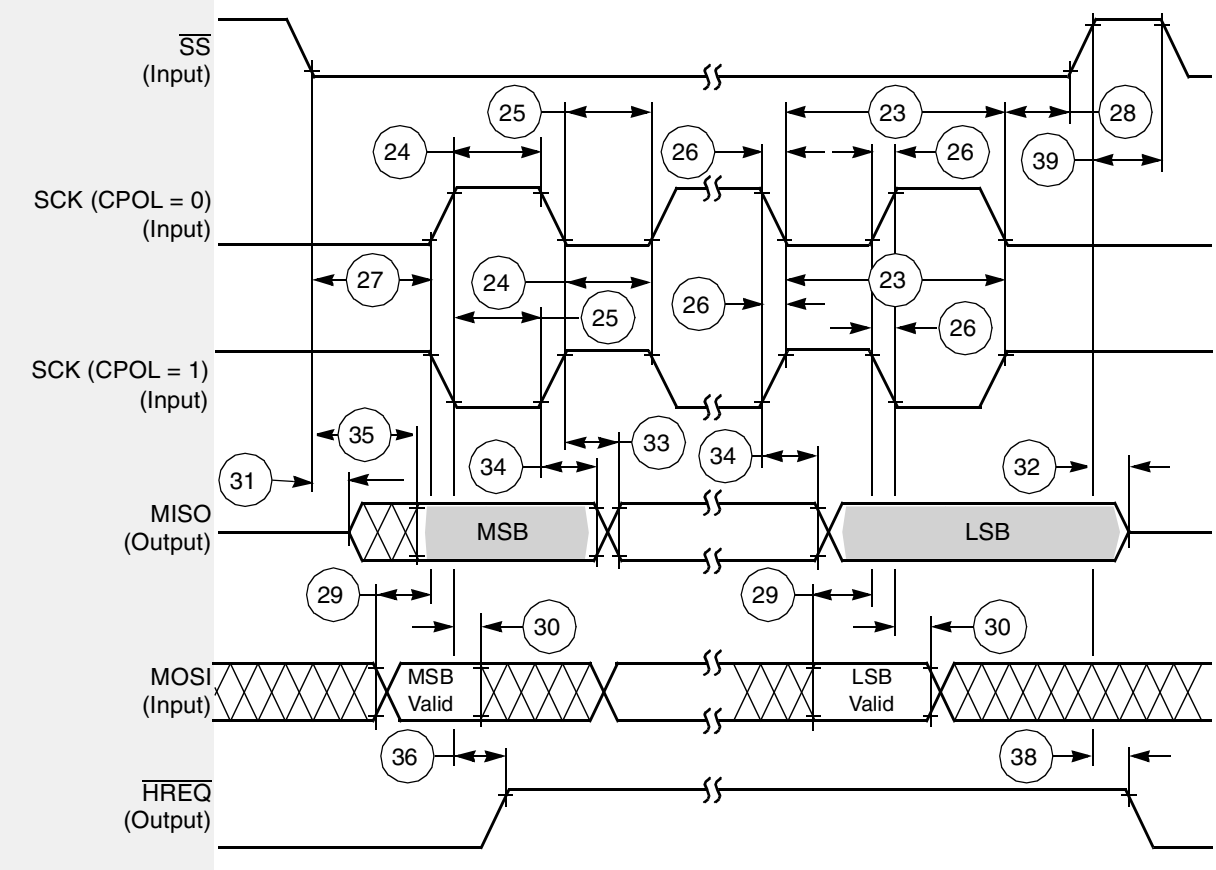

Figure 17. SPI Slave Timing Diagram (CPHA = 0)

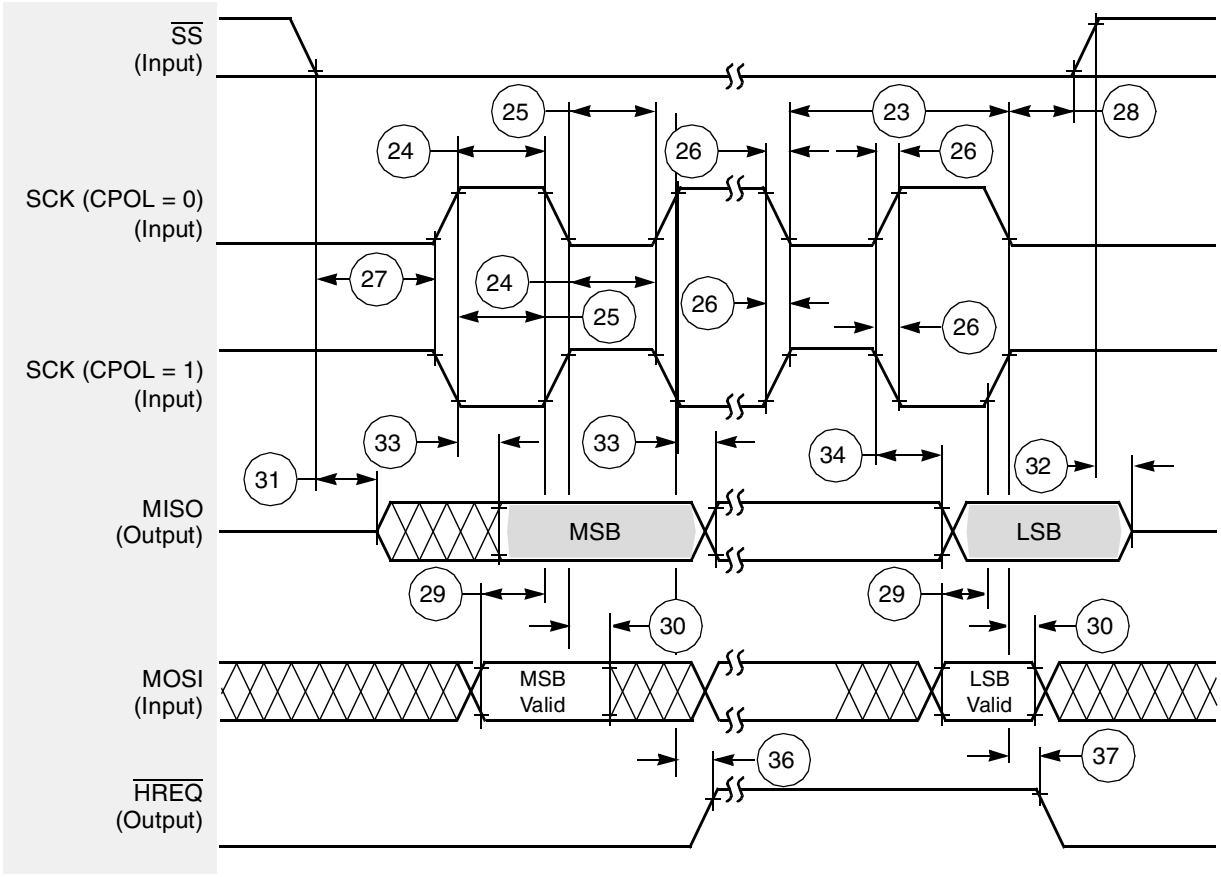

Figure 18. SPI Slave Timing Diagram (CPHA = 1)

2.11 Serial Host Interface (SHI) I²C Protocol Timing

Table 9 lists the SHI I²C protocol timing parameters and Figure 19 shows the timing diagram.

Table 9. SHI I²C Protocol Timing Parameters

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	—	 — — — —	 0 10 50 100	 — — — —	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs

Table 9. SHI I²C Protocol Timing Parameters (Continued)

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
60	$\overline{HREQ}$ in assertion to first SCL edge • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	$T_{AS;RQI}$	 4327 4317 4282 4227	 — — — —	 927 917 877 827	 — — — —	 ns ns ns ns
61	First SCL edge to $\overline{HREQ}$ is not asserted ($\overline{HREQ}$ in hold time.)	$t_{HO;RQI}$	0.0	—	0.0	—	ns

Notes:
1. V_{CORE_VDD} = 1.00± 0.10 V; T_J = –40°C to 100°C; C_L = 50 pF.
2. Pull-up resistor: R_P(min) = 1.5kΩ.
3. Capacitive load: C_b(max) = 50 pF.
4. All times assume noise free inputs.
5. All times assume internal clock frequency of 200 MHz.
6. SHI_1 specs match those of SHI.
7. Master Mode

2.12 Programming the SHI I²C Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)] \quad \textit{Eqn. 4}$$

where

— HRS is the pre scaler rate select bit. When HRS is cleared, the fixed divide-by-eight pre scaler is operational. When HRS is set, the pre scaler is bypassed.

— HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I²C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \quad \text{(if HDM[7:0] = \$02 and HRS = 1)} \quad \textit{Eqn. 5}$$

to

$$4096 \times T_C \quad \text{(if HDM[7:0] = \$FF and HRS = 0)} \quad \textit{Eqn. 6}$$

The programmed serial clock cycle (T_{I^2CCP}) should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Equation 4.

$$T_{I^2CCP} + 3 \times T_C + 45ns + T_R \quad \text{(Nominal, SCL Serial Clock Cycle (TSCL) generated as master)} \quad \textit{Eqn. 7}$$

Table 10. Enhanced Serial Audio Interface Timing Parameters (Continued)

No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	5 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge [6]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT rising edge to FST out (bl) high	—	—	— —	14 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[6]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	14 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	14 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	17.0 11.0	x ck i ck	ns
86	SCKT rising edge to data out valid	—	—	— —	13 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance[7]	—	—	— —	13 16.0	x ck i ck	ns
88	SCKT rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	14.0 9.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	—	—	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	—	—	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	—	—	4.0 5.0	— —	x ck i ck	ns

Table 10. Enhanced Serial Audio Interface Timing Parameters (Continued)

No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
92	FST input (wl) to data out enable from high impedance	—	—	—	21.0	—	ns
93	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	14.0	—	ns
94	Flag output valid after SCKT rising edge	—	—	— —	14.0 9.0	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	$2 \times T_C$	10	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

Notes:

1. V_{CORE_VDD} = 1.00 ± 0.10 V; T_J = –40°C to 100°C; C_L = 50 pF.
2. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, asynchronous mode
   (Asynchronous implies that SCKT and SCKR are two different clocks.)
   i ck s = internal clock, synchronous mode
   (Synchronous implies that SCKT and SCKR are the same clock.)
3. bl = bit length
   wl = word length
   wr = word length relative
4. SCKT(SCKT pin) = transmit clock
   SCKR(SCKR pin) = receive clock
   FST(FST pin) = transmit frame sync
   FSR(FSR pin) = receive frame sync
   HCKT(HCKT pin) = transmit high frequency clock
   HCKR(HCKR pin) = receive high frequency clock
5. For the internal clock, the external clock cycle is defined by Tc and the ESAI control register.
6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
7. Periodically sampled and not 100% tested.
8. ESAI_1, ESAI_2, ESAI_3 specs match those of ESAI.

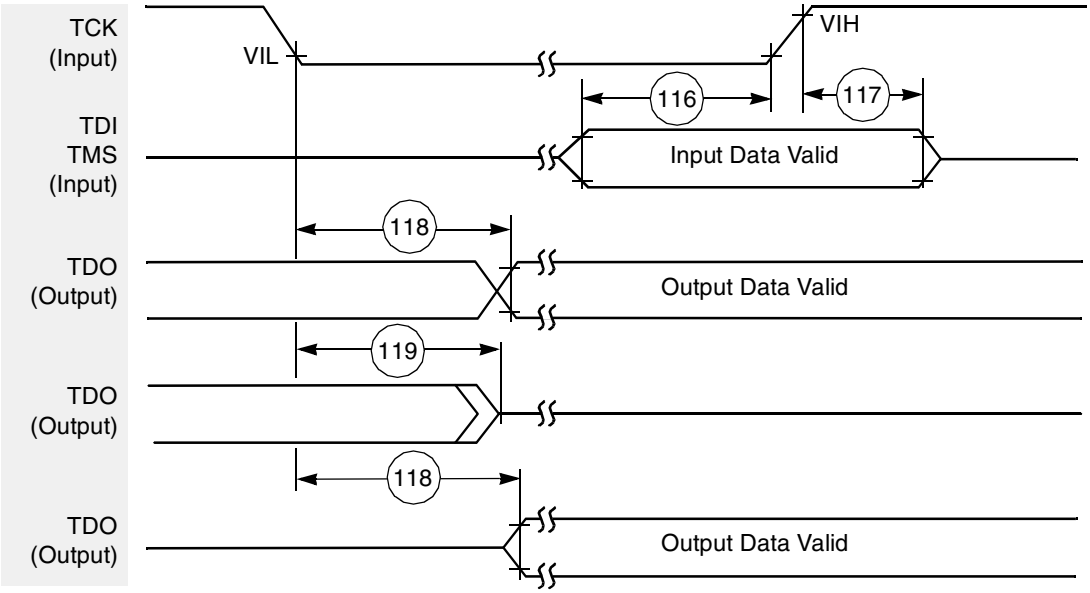

Figure 28. Test Access Port Timing Diagram

2.17 Watchdog Timer Timing

Table 14 lists the watchdog timer timing.

Table 14. Watchdog Timer Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
120	Delay from time-out to fall of $\overline{WDT}$, $\overline{WDT\_1}$	$2 \times T_C$	10.0	—	ns
121	Delay from timer clear to rise of $\overline{WDT}$, $\overline{WDT\_1}$	$2 \times Tc$	10.0	—	ns

2.18 Host Data Interface (HDI24) Timing

The HDI24 module is only on the DSP56721 device; the DSP56720 device does not have a HDI24 module. Also, only 16 bits of the HDI24 interface are pinned out on the DSP56721 device. Table 15 lists HDI24 timing and Figure 29 through Figure 35 show the timing diagrams.

Table 15. HDI24 Timing Parameters

No.	Characteristics[2]	Expression	200 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[3] $\overline{HACK}$ read assertion width	$T_C + 9.9$	14.9	—	ns
318	Read data strobe deassertion width[3] $\overline{HACK}$ read deassertion width	—	9.9	—	ns
319	Read data strobe deassertion width[3] after “Last Data Register” reads[4,5], or between two consecutive CVR, ICR, or ISR reads[6] $\overline{HACK}$ deassertion width after “Last Data Register” reads[4,5]	$2 \times T_C + 6.6$	16.6	—	ns

Table 15. HDI24 Timing Parameters (Continued)

No.	Characteristics[2]	Expression	200 MHz		Unit
			Min	Max	
339	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[4, 7, 9]	$2 \times T_C$	10.0	—	ns
340	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0)[4, 8, 9]	—	—	19.1	ns
341	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain Host Request)[4, 8, 9, 10]	—	—	300.0	ns
342	Delay from DMA $\overline{\text{HACK}}$ deassertion to HOREQ assertion				ns
	• For “Last Data Register” read[4]	$2 \times T_C + 19.1$	29.1	—	
	• For “Last Data Register” write[4]	$1 \times T_C + 19.1$	24.1	—	
	• For other cases	—	0.0	—	
343	Delay from DMA $\overline{\text{HACK}}$ assertion to HOREQ deassertion • HROD = 0[4]	—	—	20.2	ns
344	Delay from DMA $\overline{\text{HACK}}$ assertion to HOREQ deassertion for “Last Data Register” read or write • HROD = 1, open drain Host Request[4, 10]	—	—	300.0	ns

Notes:

1. In the timing diagrams that follow, the controls pins are drawn as active low. The pin polarity is programmable.
2. V_{CC} = 1.0 V ± 10%; T_J = —40°C to +100°C; C_L = 50 pF.
3. The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.
4. The “last data register” is the register at address $7, which is the last location to be read or written in data transfers.
5. This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HOREQ signal.
6. This timing is applicable only if two consecutive reads from one of these registers are executed.
7. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
8. The data strobe is host read (HRD) or host write (HWR) in the dual data strobe mode and host data strobe (HDS) in the single data strobe mode.
9. The host request is HOREQ in the single host request mode and HRRQ and HTRQ in the double host request mode.
10. In this calculation, the host request signal is pulled up by a 4.7 kW resistor in the open-drain mode.
11. HDI24_1 specs match those of HDI24.

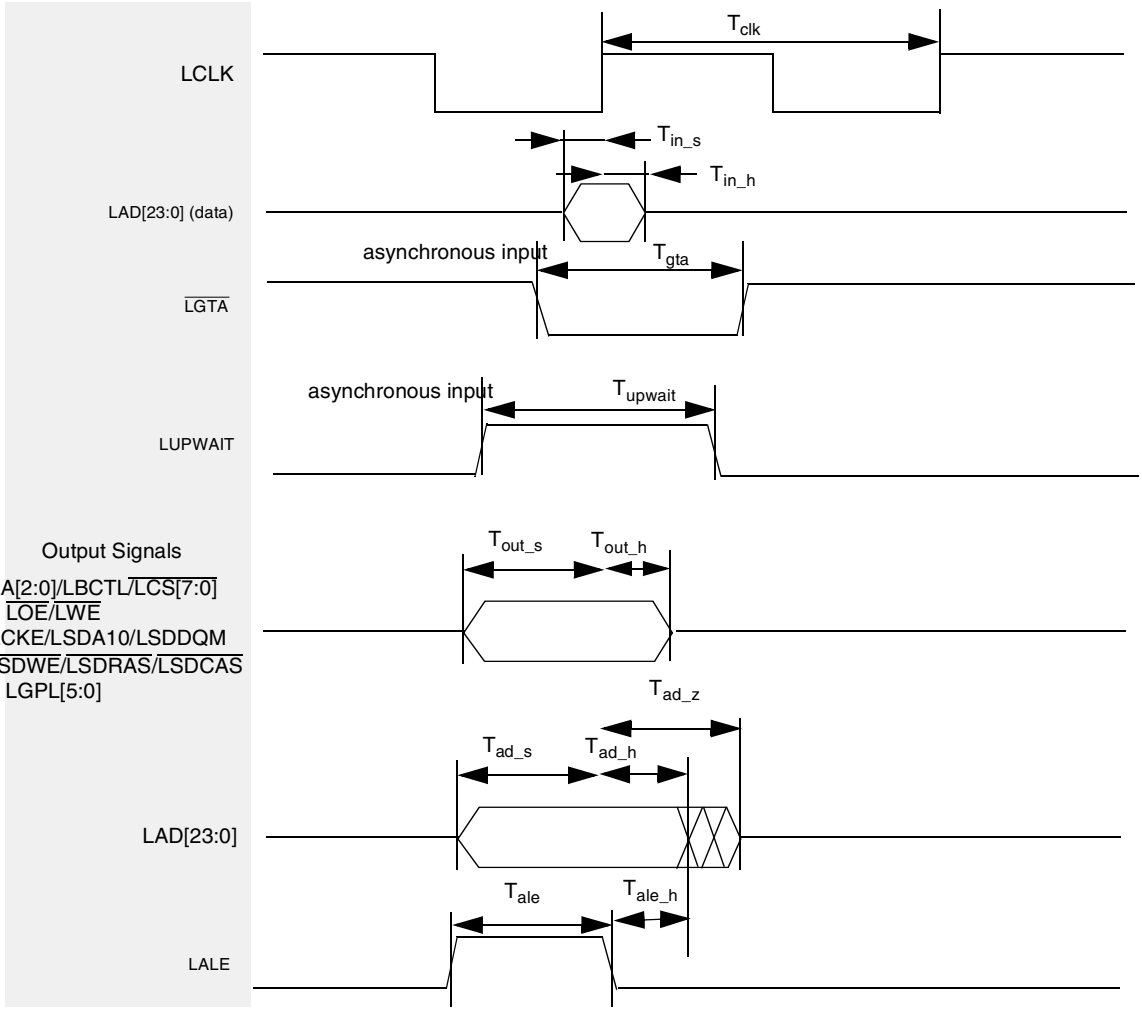

Figure 39. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 4)

Table 19. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	40	—	ns
Input setup to LCLK (except LGTA/LUPWAIT)	T_{in_s}	8	—	ns
Input hold from LCLK (except LGTA/LUPWAIT)[1]	T_{in_h}	–1	—	ns
LGTA valid time	T_{gta}	42	—	ns
LUPWAIT valid time	T_{upwait}	42	—	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	5	—	ns
LALE valid time	T_{ale}	34	—	ns
Output setup from LCLK (except LAD[23:0] and LALE)	T_{out_s}	19	—	ns
Output hold from LCLK (except LAD[23:0] and LALE)	T_{out_h}	18	—	ns

5.1 80-Pin Package Outline Drawing

Figure 41 and Figure 42 show the 80-pin package outline drawings.

Figure 41. 80-Pin Package Outline Drawing (1 of 2)

Figure 42. 80-Pin Package Outline Drawing (2 of 2)

NOTES

1. Dimensioning and tolerancing per asme Y14.5M-1994.
2. Controlling dimension: millimeter
3. Datum plane H is located at the bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datum E, F and D to be determined at datum plane H.
5. Dimensions to be determined at seating plane C.
6. Dimensions do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions include mold mismatch and are determined at datum plane H.
7. Dimension does not include dambar protrusion. Dambar protrusion shall not cause the lead width to exceed 0.46 mm. Minimnum space between protrusion and adjacent lead or protrusion 0.07 mm.

5.2 144-Pin Package Outline Drawing

Figure 43 and Figure 44 show the 144-pin package drawings.

Figure 43. 144-Pin Package Outline Drawing (1 of 2)

Figure 44. 144-Pin Package Outline Drawing (2 of 2)

NOTES

1. All dimensinos are in millimeters
2. Interpret dimensions and tolerances per ASME Y14.5M-1994.
3. Datums B, C and D to be determined at datum plane H.
4. The top ppackage body size may be smaller than the bottom package size by a maximum of 0.1 mm.
5. These dimensions do not include mold protrusions. The maximum allowable protrusion is 0.25 mm per side. These dimensions are maximum body size dimensions including mold mismatch.
6. This dimension does not include dambar protrusion. Protrusions shall not cause the lead width to exceed 0.35 mm minimum space between protrusion and an adjacent lead shall be 0.07 mm.

7 These dimensions are determined at the seating plane, datum A.

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com. Documentation is available from a local Freescale Semiconductor, Inc. distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

DSP56300 Family Manual (document number DSP56300FM). Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set.

Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manual (document number DSP56720RM). Detailed description of memory, peripherals, and interfaces.

DSP56720 Product Brief (DSP56720PB). Brief description of the DSP56720 device.

DSP56721 Product Brief (DSP56721PB). Brief description of the DSP56721 device.

7 Revision History

Table 22 summarizes revisions to this document.

Table 22. Revision History

Revision	Date	Description
5	02/2009	• Updated values and added Commercial and Automotive columns in Table 4, “DC Electrical Characteristics.” • Updated values in the following tables: Table 7, Table 9, Table 10, Table 11, Table 12, Table 13, Table 15, Table 17, Table 18, and Table 19. • In Table 10, “Enhanced Serial Audio Interface Timing Parameters,” changed value for 87 to “13”. • Added Section 2.4, “Power Consumption Considerations.” • In Section 2.20, “EMC Timing (DSP56720 Only),” added text regarding the EMC chapter and applicable sections. • Added automotive information to Table 20, “Ordering Information.”
4	04/2008	• Added formula for thermal characteristics on page 10. • Added values for pull-up and pull-down resistors on page 12.
3	03/2008	• Updated order information on page 1 to include additional parts with temperature specification.
2	02/2008	• Timing updates.
1	12/2007	• Initial release

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