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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	744kB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56721af

1 Pin Assignments

DSP56720 devices are available in one package type; DSP56721 devices are available in two package types. For the pin assignments of a specific device in a specific package, refer to Section 1.1, “Pinout for DSP56720 144-Pin Plastic LQFP Package,” through Section 1.3, “Pinout for DSP56721 144-Pin Plastic LQFP Package.”

Table 1. Pin Assignments by Package

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 3 on page 5
DSP56721	80-pin plastic LQFP	Figure 4 on page 6
	144-pin plastic LQFP	Figure 5 on page 7

For more detailed information about signals, refer to the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manuall* (DSP56720RM).

1.2 Pinout for DSP56721 80-Pin Plastic LQFP Package

Figure 4 shows the pinout of the DSP56721 80-pin plastic LQFP package.

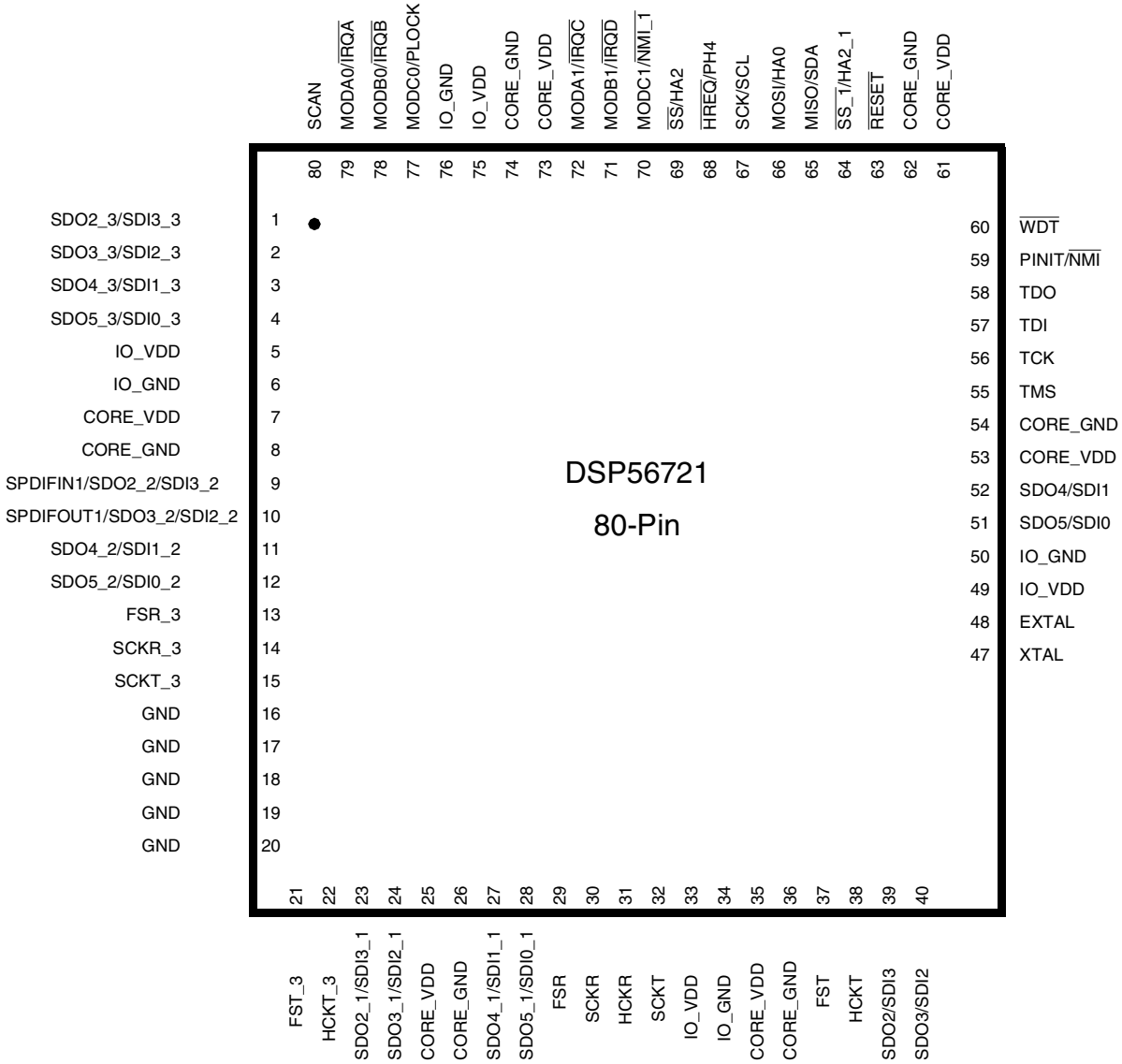

Figure 4. DSP56721 80-Pin Package

1.3 Pinout for DSP56721 144-Pin Plastic LQFP Package

Figure 5 shows the pinout of the DSP56721 144-pin plastic LQFP package.

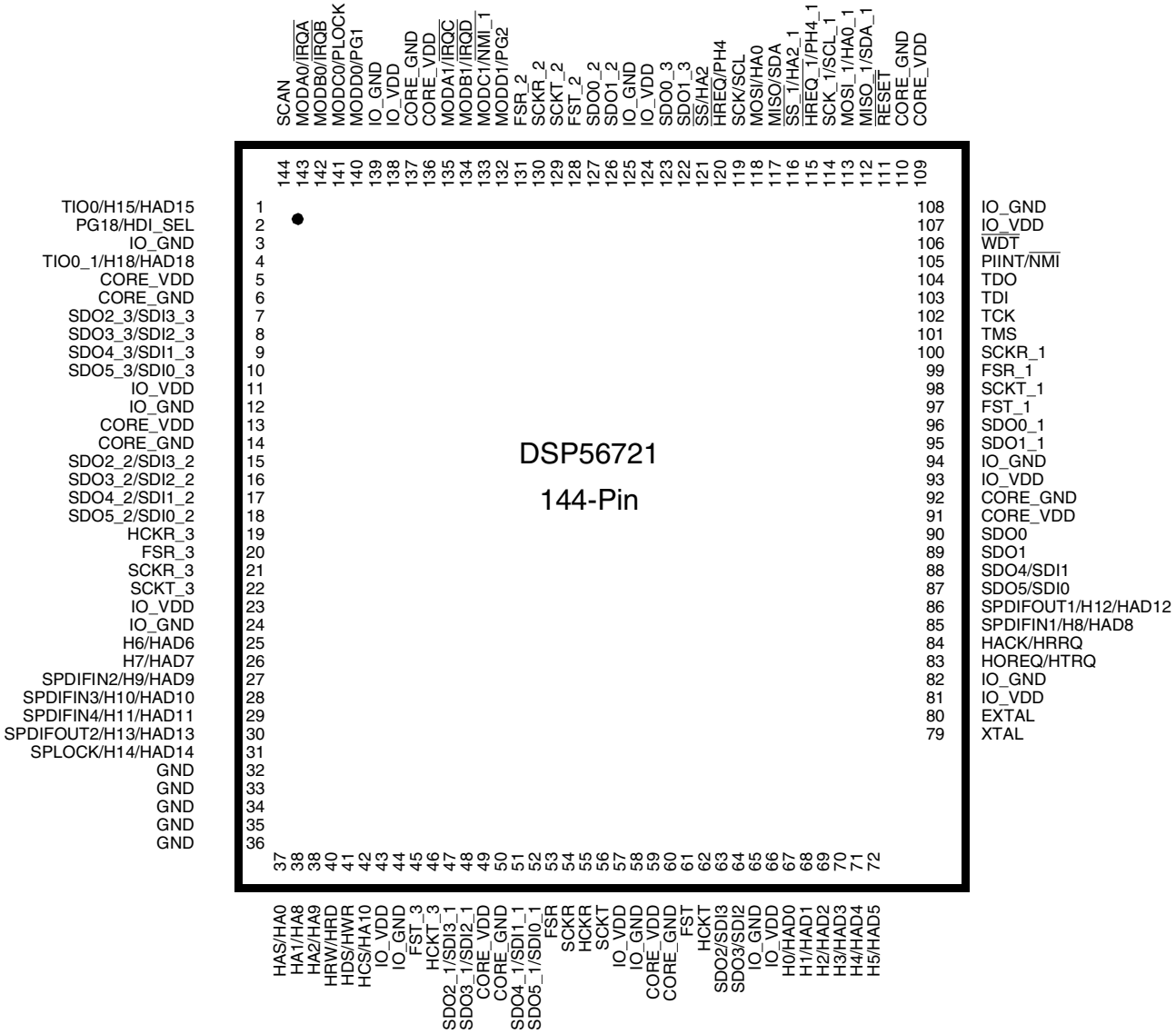

Figure 5. DSP56721 144-Pin Package Pinout

1.4 Pin Multiplexing

Many pins are multiplexed. For more about pin multiplexing, refer to the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manual* (DSP56720RM).

$P_D = 1.1\ V \times 625\ mA$

$= 0.6875\ W$

$T_J = 70 + (0.6875 \times 40)$

$= 97.5°\ C$

2.3 Power Requirements

To prevent high current conditions due to possible improper sequencing of the power supplies, use an external Schottky diode as shown in Figure 6, connected between the DSP56720/DSP56721 IO_VDD and Core_VDD power pins.

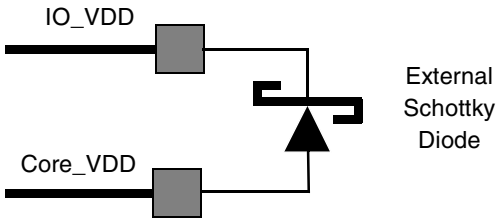

Figure 6. Prevent High Current Conditions by Using External Schottky Diode

If an external Schottky diode is not used (to prevent a high current condition at power-up), then IO_VDD must be applied ahead of Core_VDD, as shown in Figure 7.

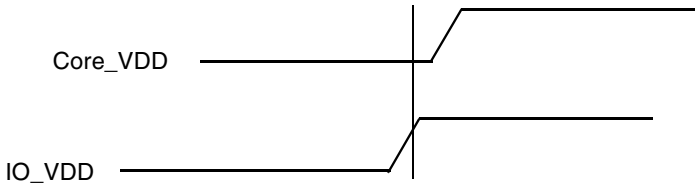

Figure 7. Prevent High Current Conditions by Applying IO_VDD Before Core_VDD

For correct operation of the internal power-on reset logic, the Core_VDD ramp rate (Tr) to full supply must be less than 10 ms, as shown in Figure 8.

There are no power down requirement for the digital 1.0 V (CORE) and 3.3 V (IO). For the analog PLL power, the digital (IO) 3.3 V must be power up before the analog 3.3 V power. Similarly, for power down the digital (IO) 3.3 V must be power down after the analog power 3.3 V. This requirement is for avoiding possible leakage.

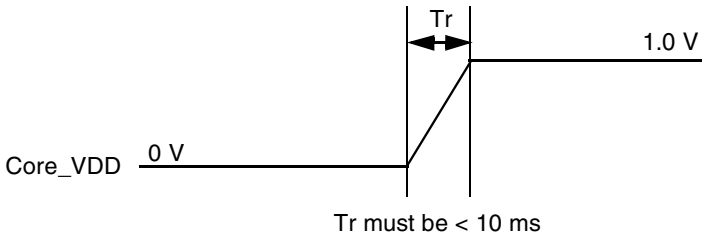

Figure 8. Ensure Correct Operation of Power-On Reset with Fast Ramp of Core_VDD

2.5 DC Electrical Characteristics

Table 4 shows the DC electrical characteristics.

Table 4. DC Electrical Characteristics

	Characteristics	Symbol	Min	Typ	Max	Unit
Commercial	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.9	1	1.1	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Automotive	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.95	1	1.05	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Note: To avoid a high current condition and possible system damage, all 3.3 V supplies must rise before the 1.0 V supplies rise.						
Input low voltage		V_{IL}	–0.3	—	0.8	V
Input leakage current		I_{IN}	—	—	± 84	µA
Clock pin Input Capacitance (EXTAL)		C_{IN}	—	18	—	pF
High impedance (off-state) input current (@ 3.3 V or 0 V)		I_{TSI}	–10	—	10	µA
Output high voltage I_{OH} = -12 mA LSYNC_OUT, LALE, LCLK Pins I_{OH} = -16 mA, TDO Pin I_{OH} = -24 mA		V_{OH}	2.4	—	—	V
Output low voltage I_{OL} = 12 mA LSYNC_OUT, LALE, LCLK Pins I_{OL} = 16 mA, TDO Pins I_{OL} = 24 mA		V_{OL}	—	—	0.4	V
Internal pull-up resistor		R_{PU}	64	92	142	kΩ
Internal pull-down resistor		R_{PD}	57	90	157	kΩ
Commercial	Internal supply current[1] (core only) at internal clock of 200 MHz					
	• In Normal mode	I_{CCI}	—	224	445	mA
	• In Wait mode	I_{CCW}	—	121	353	mA
	• In Stop mode[2]	I_{CCS}	—	90	327	mA

Table 7. Reset, Stop, Mode Select, and Interrupt Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$6 \times T_C$	—	30.0	ns
	• Data write to ESAI, ESAI_1, ESAI_2, ESAI_3, SHI, SHI_1	$7 \times T_C$	—	35.0	ns
	• Timer, Timer_1	$2 \times T_C$	—	10.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$3 \times T_C$	—	15.0	ns

Notes:

1. When using fast interrupts and when $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, if using an external clock (PCTL Bit 13 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.
   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shut down during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 200 µs.
3. Periodically sampled and not 100% tested.
4. $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When V_{DD} is valid, but the other "required $\overline{RESET}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

Figure 11 shows the reset timing diagram.

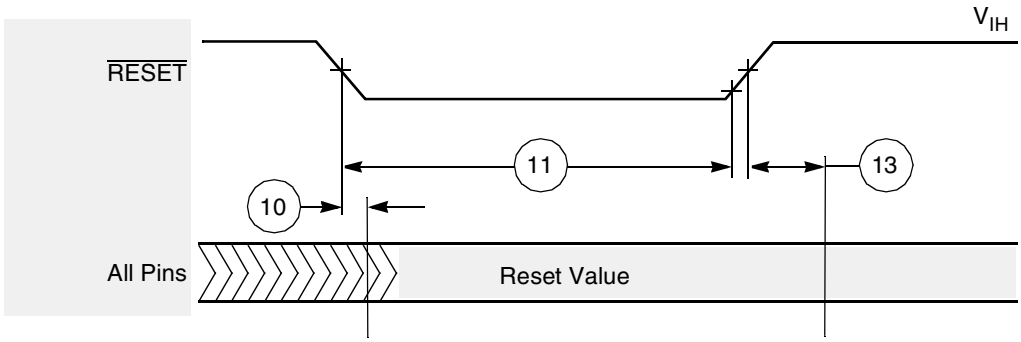

Figure 11. Reset Timing Diagram

Figure 12 shows the external fast interrupt timing diagram.

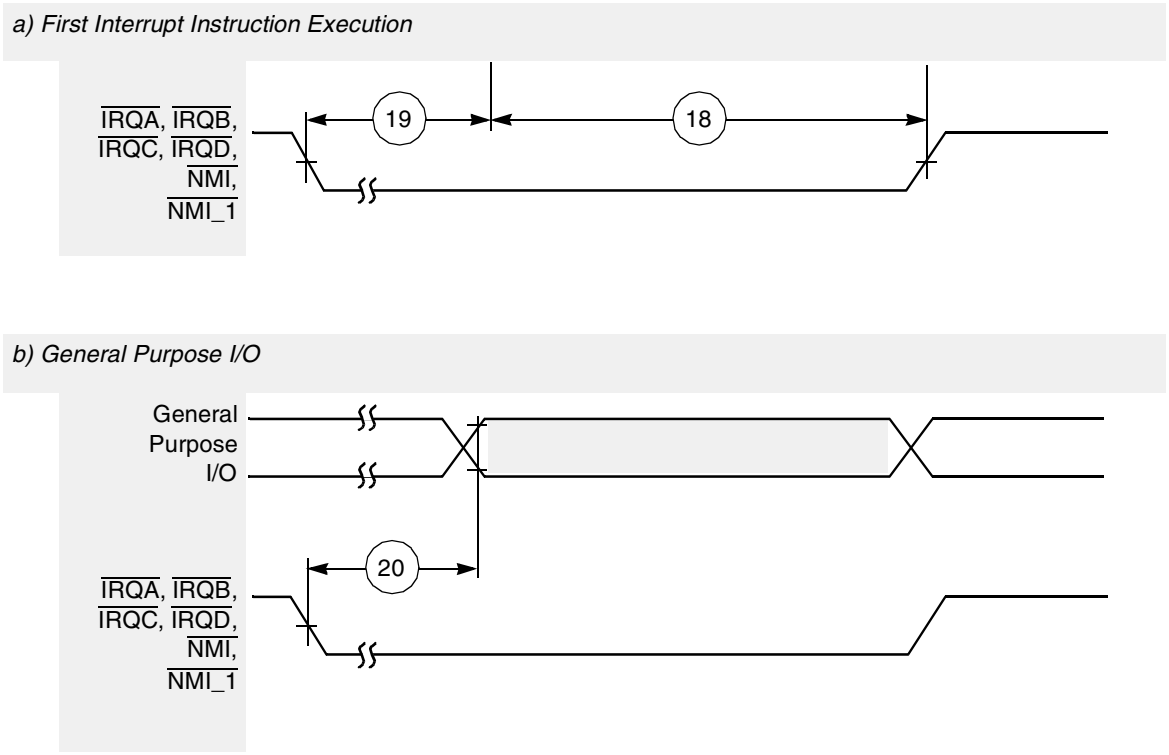

Figure 12. External Fast Interrupt Timing Diagram

Figure 13 shows the negative edge-triggered external interrupt timing diagram.

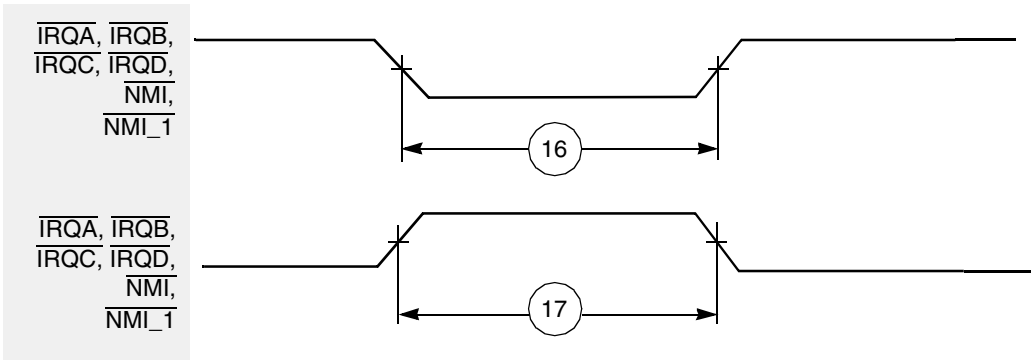

Figure 13. External Interrupt Timing Diagram (Negative Edge-Triggered)

Figure 14 shows the MODE select set up and hold timing diagram.

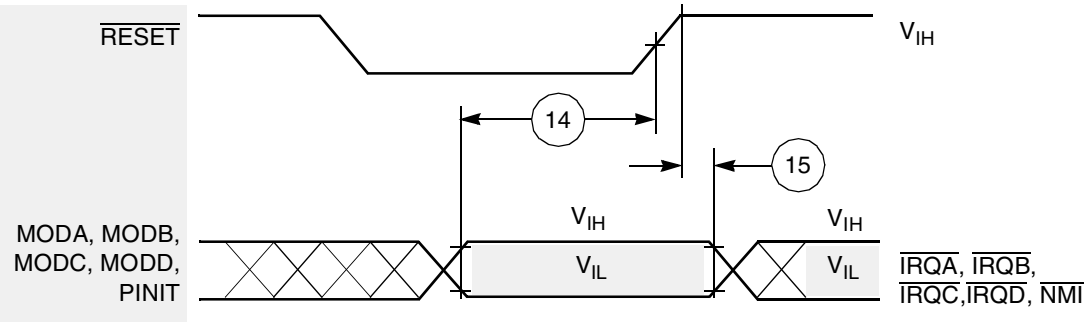

Figure 14. MODE Select Set Up and Hold Timing Diagram

2.10 Serial Host Interface (SHI) SPI Protocol Timing

Table 8 shows the SHI SPI protocol timing parameters and Figure 15 through Figure 18 show the timing diagrams.

Table 8. Serial Host Interface SPI Protocol Timing Parameters

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master	Bypassed	$10 \times T_C + 9$	59.0	—	ns
			Very Narrow	$10 \times T_C + 9$	59.0	—	ns
			Narrow	$10 \times T_C + 133$	183.0	—	ns
			Wide	$10 \times T_C + 333$	373.0	—	ns
		Slave	Bypassed	$2.0 \times T_C + 19.6$	59.2	—	ns
			Very Narrow	$2.0 \times T_C + 19.6$	59.2	—	ns
			Narrow	$2.0 \times T_C + 86.6$	193.2	—	ns
			Wide	$2.0 \times T_C + 186.6$	393.2	—	ns
XX	Tolerable Spike width on data or clock in	—	Bypassed	—	—	0	ns
			Very Narrow	—	—	10	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
24	Serial clock high period	Master	Bypassed	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Very Narrow	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Narrow	$0.5 \times (t_{SPICC})$	91.5	—	ns
			Wide	$0.5 \times (t_{SPICC})$	186.5	—	ns
		Slave	Bypassed	$2.0 \times T_C + 19.6$	29.6	—	ns
			Very Narrow	$2.0 \times T_C + 19.6$	29.6	—	ns
			Narrow	$2.0 \times T_C + 86.6$	96.6	—	ns
			Wide	$2.0 \times T_C + 186.6$	196.6	—	ns

Table 8. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	$3.0 \times T_C + 30$	—	45	ns
			Very Narrow	$3.0 \times T_C + 95$	—	110	ns
			Narrow	$3.0 \times T_C + 120$	—	135	ns
			Wide	$3.0 \times T_C + 210$	—	225	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	$2.0 \times T_C$	10	—	ns
			Very Narrow	$2.0 \times T_C + 5$	15	—	ns
			Narrow	$2.0 \times T_C + 45$	55	—	ns
			Wide	$2.0 \times T_C + 95$	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	14.0	ns
36	First SCK sampling edge to $\overline{HREQ}$ output deassertion	Slave	Bypassed	$3.0 \times T_C + 30$	45	—	ns
			Very Narrow	$3.0 \times T_C + 40$	55	—	ns
			Narrow	$3.0 \times T_C + 80$	95	—	ns
			Wide	$3.0 \times T_C + 130$	145	—	ns
37	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted (CPHA = 1)	Slave	Bypassed	$4.0 \times T_C + 30$	50.0	—	ns
			Very Narrow	$4.0 \times T_C + 40$	60.0	—	ns
			Narrow	$4.0 \times T_C + 80$	100.0	—	ns
			Wide	$4.0 \times T_C + 130$	150.0	—	ns
38	$\overline{SS}$ deassertion to $\overline{HREQ}$ output not deasserted (CPHA = 0)	Slave	—	$3.0 \times T_C + 30$	45.0	—	ns
39	$\overline{SS}$ deassertion pulse width (CPHA = 0)	Slave	—	$2.0 \times T_C$	10.0	—	ns
40	$\overline{HREQ}$ in assertion to first SCK edge	Master	Bypassed	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Very Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	111.5	—	ns
			Wide	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	206.5	—	ns

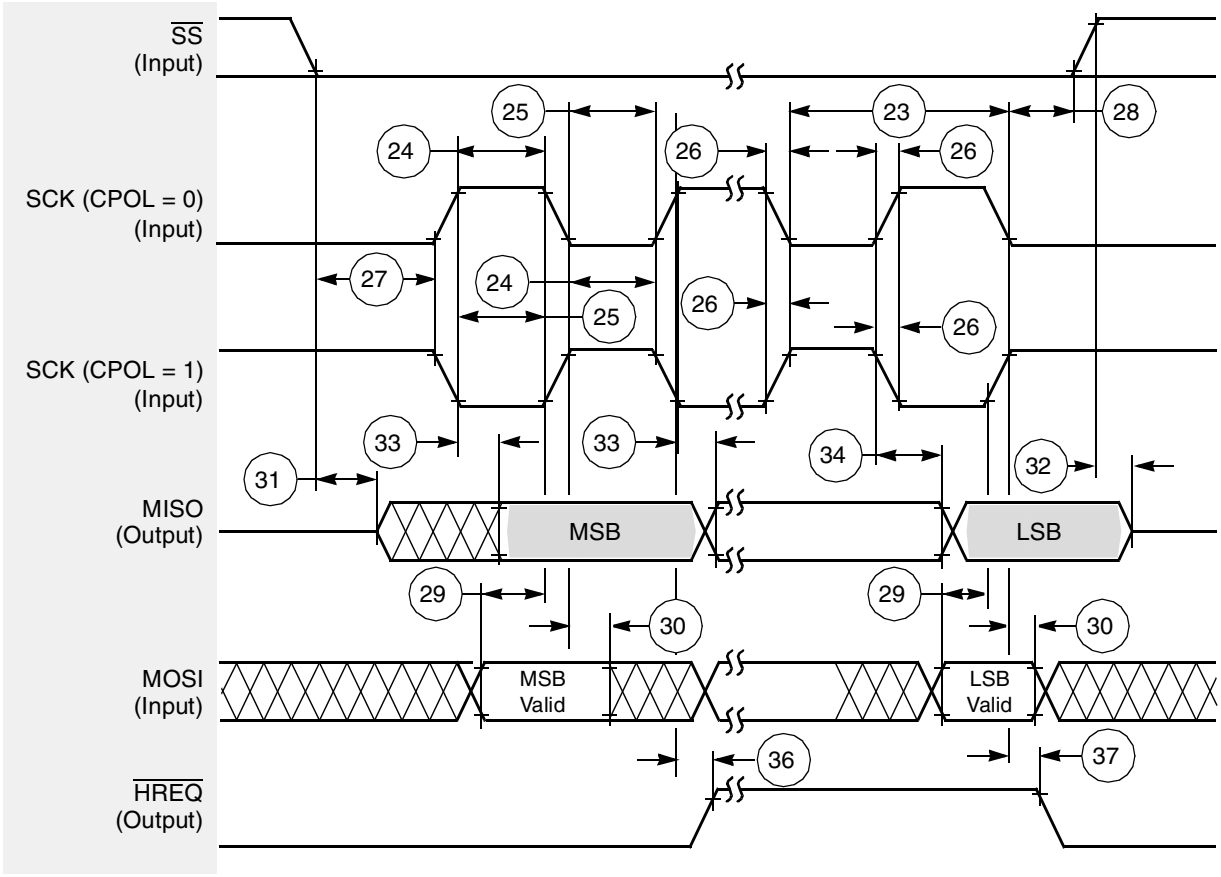

Figure 18. SPI Slave Timing Diagram (CPHA = 1)

2.11 Serial Host Interface (SHI) I²C Protocol Timing

Table 9 lists the SHI I²C protocol timing parameters and Figure 19 shows the timing diagram.

Table 9. SHI I²C Protocol Timing Parameters

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	—	 — — — —	 0 10 50 100	 — — — —	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs

Table 10. Enhanced Serial Audio Interface Timing Parameters (Continued)

No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	5 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge [6]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT rising edge to FST out (bl) high	—	—	— —	14 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[6]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[6]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	14 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	14 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	17.0 11.0	x ck i ck	ns
86	SCKT rising edge to data out valid	—	—	— —	13 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance[7]	—	—	— —	13 16.0	x ck i ck	ns
88	SCKT rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	14.0 9.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[6]	—	—	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	—	—	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	—	—	4.0 5.0	— —	x ck i ck	ns

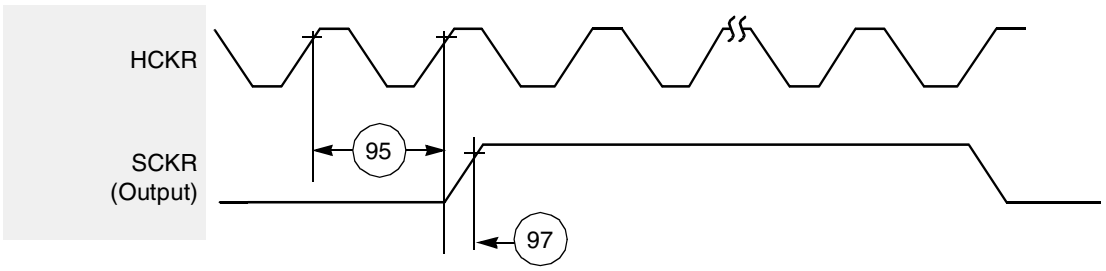

Figure 23. ESAI HCKR Timing

2.14 Timer Timing

Table 11 lists the timer timing parameters and Figure 24 shows the timing diagram.

Table 11. Timer Timing Parameters

No.	Characteristics	Expression			Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	12.0	—	ns
99	TIO High	$2 \times T_C + 2.0$	12.0	—	ns

Notes:
1. V_{CORE_VDD} = 1.00 V ± 0.10 V; T_J = –40°C to 100°C, C_L = 50 pF
2. TIMER_1 specs match those of TIMER

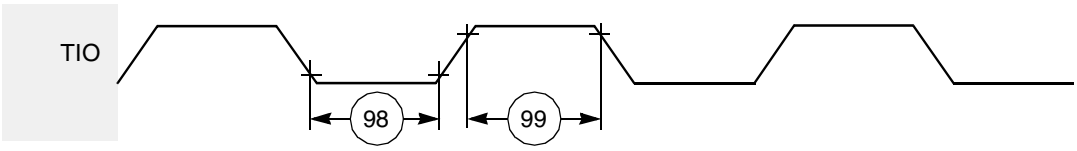

Figure 24. TIO Timer Event Input Restrictions Diagram

2.15 GPIO Timing

Table 12 lists the general purpose input and output (GPIO) timing and Figure 25 shows the timing diagram.

Table 12. GPIO Timing Parameters

No.	Characteristics[1]	Expression	Min	Max	Unit
100	Fsys edge to GPIO out valid (GPIO out delay time)[2]	—	—	7	ns
101	Fsys edge to GPIO out not valid (GPIO out hold time)[2]	—	—	7	ns
102	Fsys In valid to EXTAL edge (GPIO in set-up time)[2]	—	2	—	ns
103	Fsys edge to GPIO in not valid (GPIO in hold time)[2]	—	0	—	ns
104	Minimum GPIO pulse high width	2 × TC	10	—	ns

Table 15. HDI24 Timing Parameters (Continued)

No.	Characteristics[2]	Expression	200 MHz		Unit
			Min	Max	
320	Write data strobe assertion width[7] $\overline{HACK}$ write assertion width	—	13.2	—	ns
321	Write data strobe deassertion width[7] $\overline{HACK}$ write deassertion width • after ICR, CVR and “Last Data Register” writes[4]	$2 \times T_C + 6.6$	16.6	—	ns
	• after IVR writes, or • after TXH:TXM writes (with HBE=0), or • after TXL:TXM writes (with HBE=1)	—	16.5	—	—
322	$\overline{HAS}$ assertion width	—	9.9	—	ns
323	$\overline{HAS}$ deassertion to data strobe assertion[8]	—	0.0	—	ns
324	Host data input setup time before write data strobe deassertion[7] Host data input setup time before $\overline{HACK}$ write deassertion	—	9.9	—	ns
325	Host data input hold time after write data strobe deassertion[7] Host data input hold time after $\overline{HACK}$ write deassertion	—	3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[3] $\overline{HACK}$ read assertion to output data active from high impedance	—	5.9	—	ns
327	Read data strobe assertion to output data valid[3] $\overline{HACK}$ read assertion to output data valid	—	—	29.6	ns
328	Read data strobe deassertion to output data high impedance[3] $\overline{HACK}$ read deassertion to output data high impedance	—	—	9.9	ns
329	Output data hold time after read data strobe deassertion[3] Output data hold time after $\overline{HACK}$ read deassertion	—	3.3	—	ns
330	$\overline{HCS}$ assertion to read data strobe deassertion[3]	$T_C + 9.9$	14.9	—	ns
331	$\overline{HCS}$ assertion to write data strobe deassertion[7]	—	9.9	—	ns
332	$\overline{HCS}$ assertion to output data valid	—	—	19.1	ns
333	$\overline{HCS}$ hold time after data strobe deassertion[8]	—	0.0	—	ns
334	Address (AD7—AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)	—	4.7	—	ns
335	Address (AD7—AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)	—	3.3	—	ns
336	A10—A8 (HMUX=1), A2—A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[8] • Read	—	0	—	ns
	• Write	—	4.7	—	
337	A10—A8 (HMUX=1), A2—A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[8]	—	3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[3, 4, 9]	T_C	5.0	—	ns

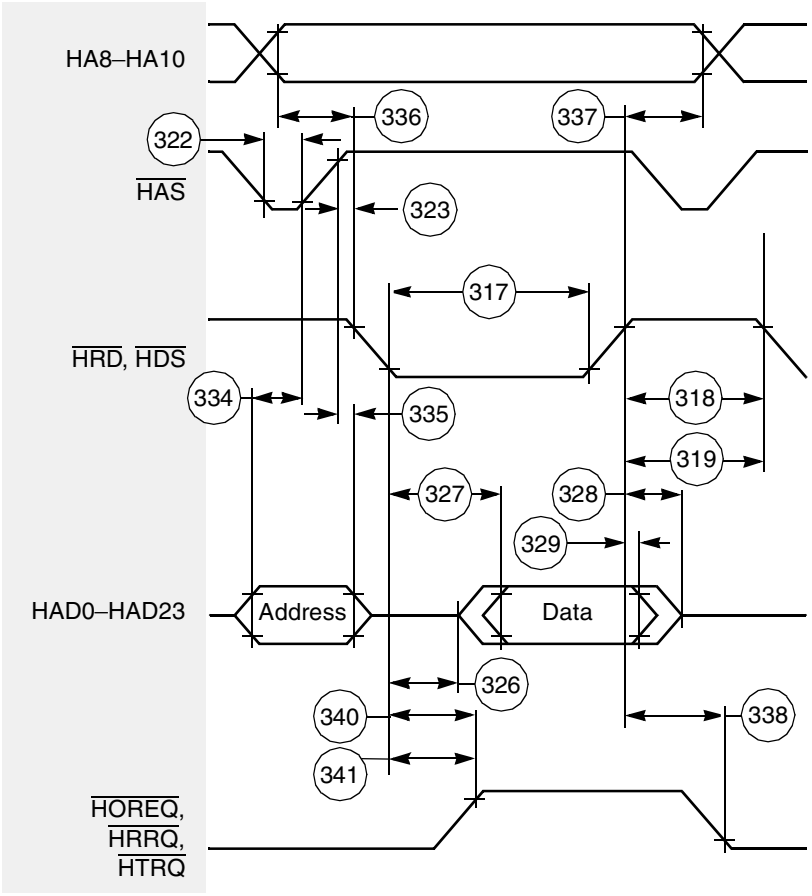

Figure 32. HDI24 Read Timing Diagram, Multiplexed Bus

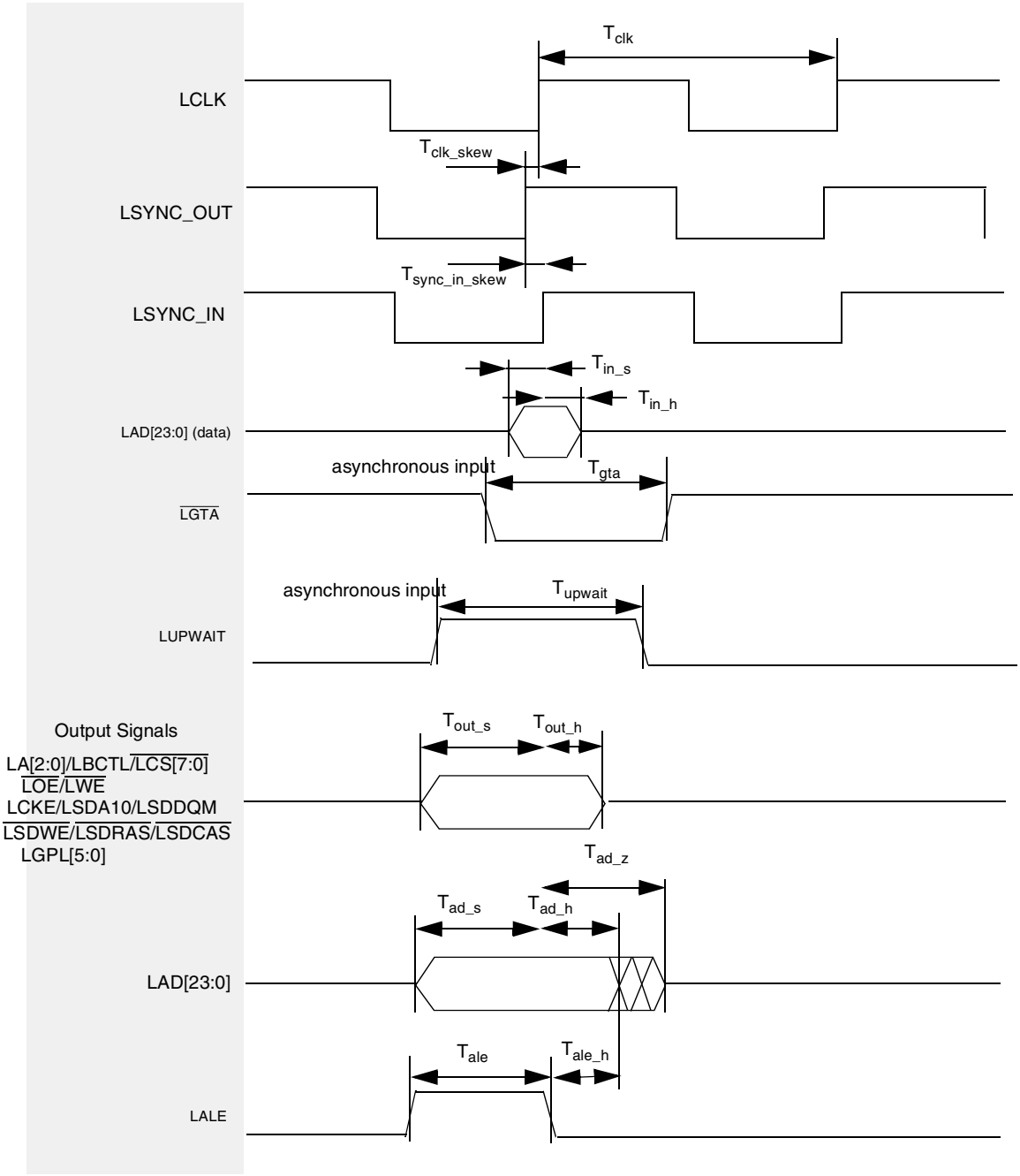

Figure 38. EMC Signals (EMC PLL Enabled; LCRR[CLKDIV] = 2)

Table 18. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 4)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	20	—	ns
Input setup to LCLK (except $\overline{LGTA}$/LUPWAIT)	T_{in_s}	8	—	ns
Input hold from LCLK (except $\overline{LGTA}$/LUPWAIT)[1]	T_{in_h}	-1	—	ns
$\overline{LGTA}$ valid time	T_{gta}	22	—	ns
LUPWAIT valid time	T_{upwait}	22	—	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	4	—	ns
LALE valid time	T_{ale}	14	—	ns
Output setup from LCLK (except LAD[23:0] and LALE)	T_{out_s}	9	—	ns
Output hold from LCLK (except LAD[23:0] and LALE)	T_{out_h}	8	—	ns
LAD[23:0] output setup from LCLK	T_{ad_s}	8	—	ns
LAD[23:0] output hold from LCLK	T_{ad_h}	7	—	ns
LCLK to output high impedance for LAD[23:0]	T_{ad_z}	—	8.1	ns

Notes:
1. A negative hold time means that the signal could be invalid before the LCLK rising edge.

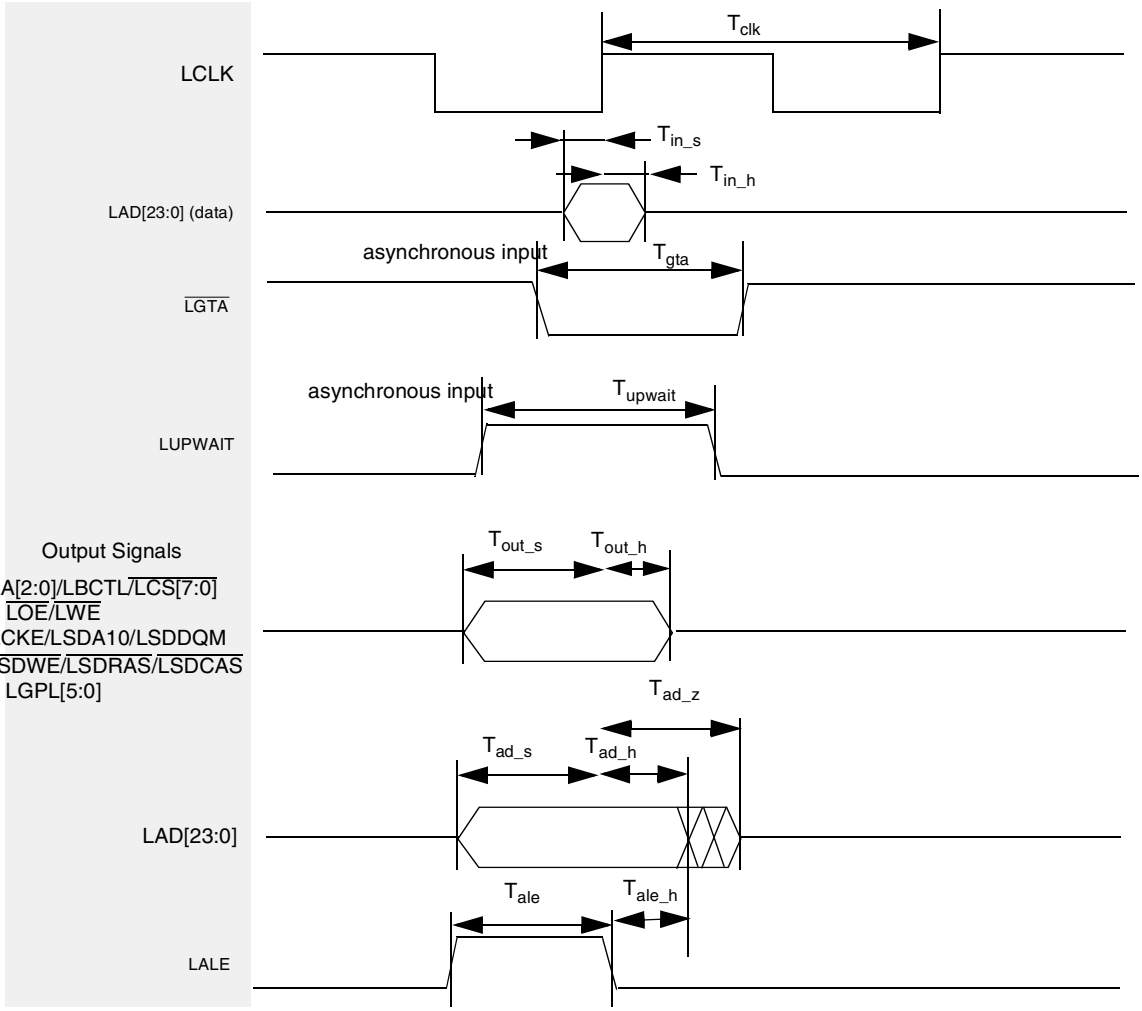

Figure 39. EMC Signals (EMC PLL Bypassed; LRCC[CLKDIV] = 4)

Table 19. EMC Timing Parameters (EMC PLL Bypassed; LRCC[CLKDIV] = 8)

Parameter	Symbol	Min	Max	Unit
LCLK cycle time	T_{clk}	40	—	ns
Input setup to LCLK (except LGTA/LUPWAIT)	T_{in_s}	8	—	ns
Input hold from LCLK (except LGTA/LUPWAIT)[1]	T_{in_h}	–1	—	ns
LGTA valid time	T_{gta}	42	—	ns
LUPWAIT valid time	T_{upwait}	42	—	ns
LALE negedge to LAD (address phase) invalid (address latch hold time)	T_{ale_h}	5	—	ns
LALE valid time	T_{ale}	34	—	ns
Output setup from LCLK (except LAD[23:0] and LALE)	T_{out_s}	19	—	ns
Output hold from LCLK (except LAD[23:0] and LALE)	T_{out_h}	18	—	ns

4 Ordering Information

Table 20 provides ordering information for both the DSP56720 and DSP56721.

Table 20. Ordering Information

Device	Device Marking	Ambient Temp.	LQFP Package
DSP56720 Commercial	DSPA56720AG	0°C–70°C	20 mm × 20 mm
	DSPB56720AG	0°C–70°C	20 mm × 20 mm
	DSPC56720AG	0°C–70°C	20 mm × 20 mm
DSP56720 Automotive	DSPA56720CAG	–40°C–85°C	20 mm × 20 mm
	DSPB56720CAG	–40°C–85°C	20 mm × 20 mm
	DSPC56720CAG	–40°C–85°C	20 mm × 20 mm
DSP56721 Commercial	DSPA56721AG	0°C–70°C	20 mm × 20 mm
	DSPB56721AG	0°C–70°C	20 mm × 20 mm
	DSPC56721AG	0°C–70°C	20 mm × 20 mm
	DSPA56721AF	0°C–70°C	14 mm × 14 mm
	DSPB56721AF	0°C–70°C	14 mm × 14 mm
	DSPC56721AF	0°C–70°C	14 mm × 14 mm
DSP56721 Automotive	DSPA56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPB56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPC56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPA56721CAF	–40°C–85°C	14 mm × 14 mm
	DSPB56721CAF	–40°C–85°C	14 mm × 14 mm
	DSPC56721CAF	–40°C–85°C	14 mm × 14 mm

5 Package Information

For the outline drawings of available device packages, see Table 21 and sections 5.1–5.2.

Table 21. Package Outline Drawings

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52
DSP56721	80-pin plastic LQFP	Figure 43 on page 51 and Figure 42 on page 50
	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52

5.1 80-Pin Package Outline Drawing

Figure 41 and Figure 42 show the 80-pin package outline drawings.

Figure 41. 80-Pin Package Outline Drawing (1 of 2)

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Document Number: DSP56720EC
Rev. 5
02/2009

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