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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Not For New Designs
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	744kB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56721ag

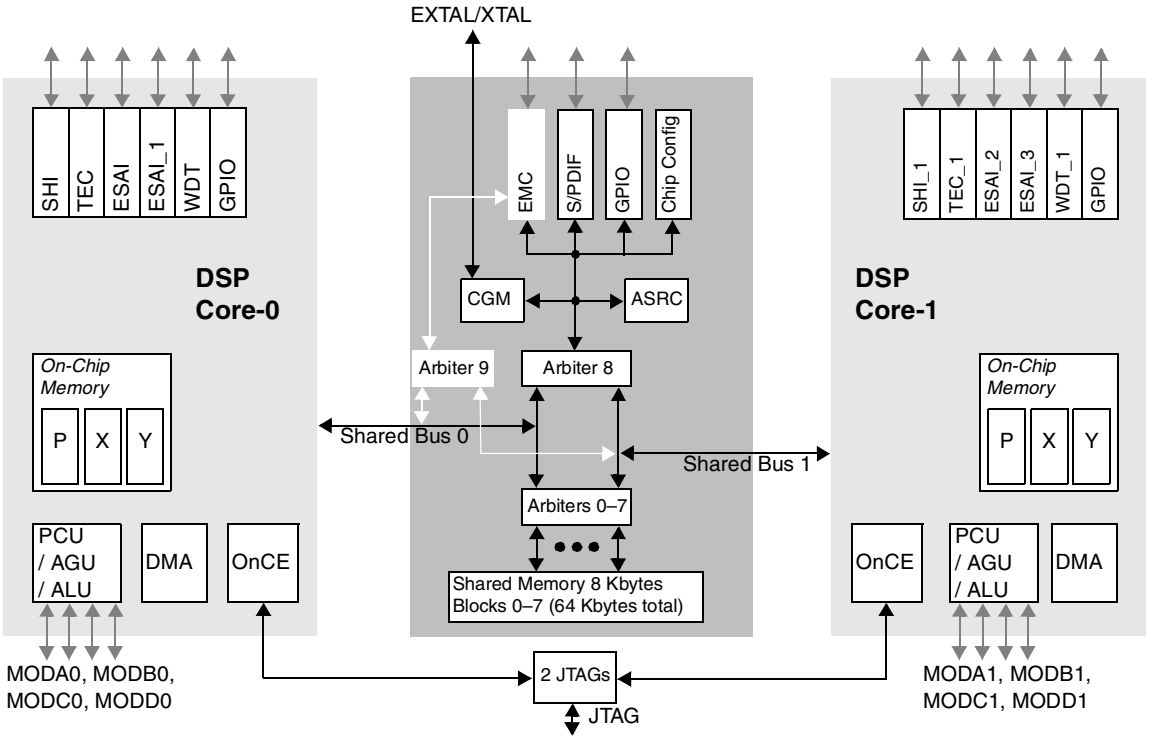


Figure 1. DSP56720 Block Diagram

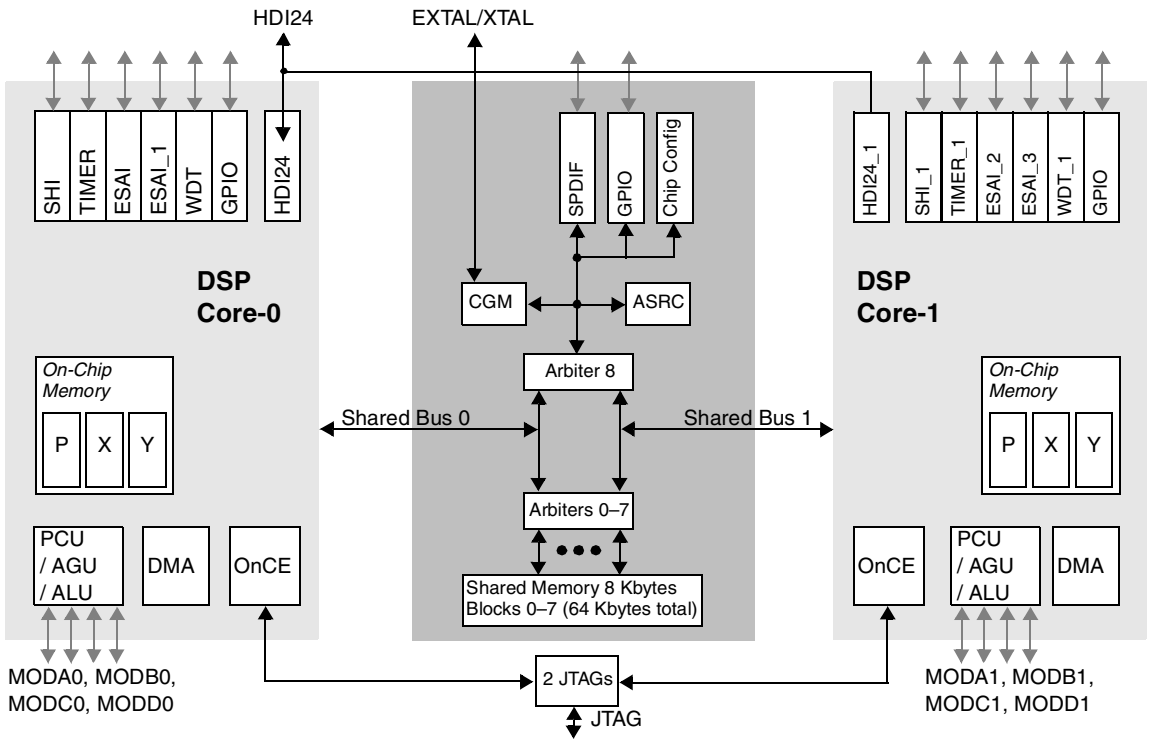


Figure 2. DSP56721 Block Diagram

1 Pin Assignments

DSP56720 devices are available in one package type; DSP56721 devices are available in two package types. For the pin assignments of a specific device in a specific package, refer to Section 1.1, “Pinout for DSP56720 144-Pin Plastic LQFP Package,” through Section 1.3, “Pinout for DSP56721 144-Pin Plastic LQFP Package.”

Table 1. Pin Assignments by Package

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 3 on page 5
DSP56721	80-pin plastic LQFP	Figure 4 on page 6
	144-pin plastic LQFP	Figure 5 on page 7

For more detailed information about signals, refer to the *Symphony™ DSP56720/DSP56721 Multi-Core Audio Processors Reference Manuall* (DSP56720RM).

2.5 DC Electrical Characteristics

Table 4 shows the DC electrical characteristics.

Table 4. DC Electrical Characteristics

	Characteristics	Symbol	Min	Typ	Max	Unit
Commercial	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.9	1	1.1	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Automotive	Supply voltages: • Core (Core_VDD) • PLL (PLLD_VDD, PLLD1_VDD)	V_{DD}	0.95	1	1.05	V
	Supply voltages: • I/O (IO_VDD) • PLL (PLLP_VDD, PLLP1_VDD) • PLL (PLLA_VDD, PLLA1_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Note: To avoid a high current condition and possible system damage, all 3.3 V supplies must rise before the 1.0 V supplies rise.						
Input low voltage		V_{IL}	–0.3	—	0.8	V
Input leakage current		I_{IN}	—	—	± 84	µA
Clock pin Input Capacitance (EXTAL)		C_{IN}	—	18	—	pF
High impedance (off-state) input current (@ 3.3 V or 0 V)		I_{TSI}	–10	—	10	µA
Output high voltage I_{OH} = -12 mA LSYNC_OUT, LALE, LCLK Pins I_{OH} = -16 mA, TDO Pin I_{OH} = -24 mA		V_{OH}	2.4	—	—	V
Output low voltage I_{OL} = 12 mA LSYNC_OUT, LALE, LCLK Pins I_{OL} = 16 mA, TDO Pins I_{OL} = 24 mA		V_{OL}	—	—	0.4	V
Internal pull-up resistor		R_{PU}	64	92	142	kΩ
Internal pull-down resistor		R_{PD}	57	90	157	kΩ
Commercial	Internal supply current[1] (core only) at internal clock of 200 MHz					
	• In Normal mode	I_{CCI}	—	224	445	mA
	• In Wait mode	I_{CCW}	—	121	353	mA
	• In Stop mode[2]	I_{CCS}	—	90	327	mA

Figure 12 shows the external fast interrupt timing diagram.

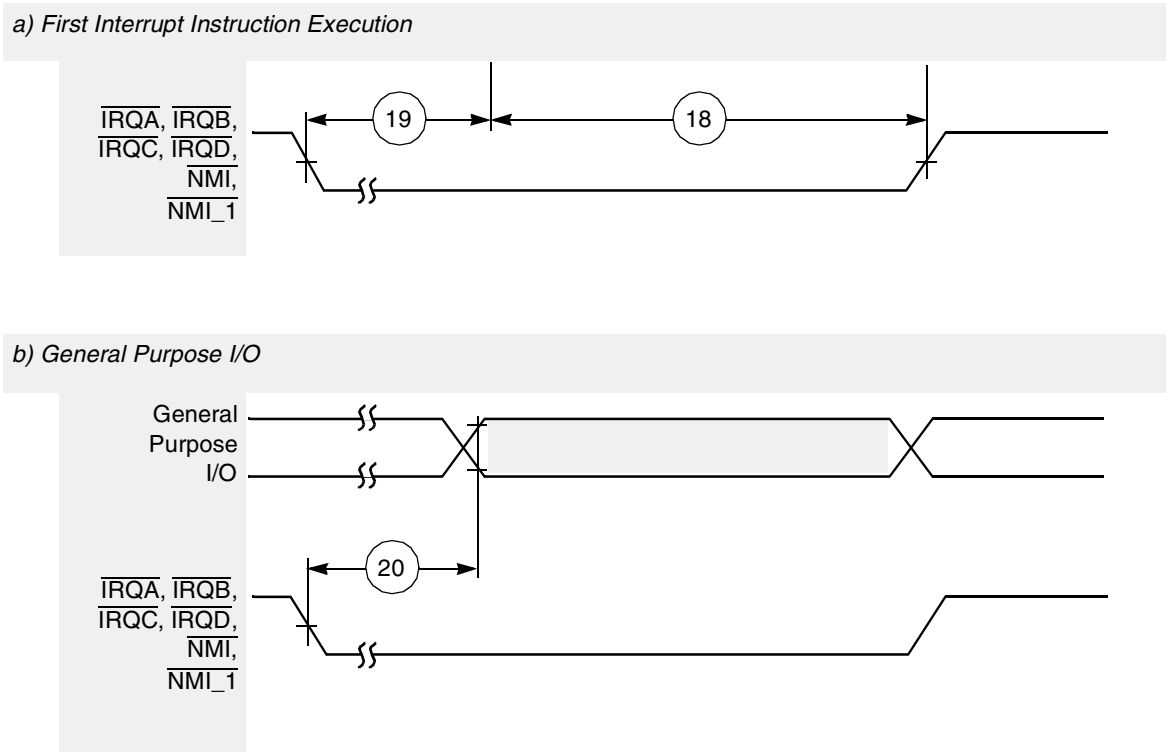


Figure 12. External Fast Interrupt Timing Diagram

Figure 13 shows the negative edge-triggered external interrupt timing diagram.

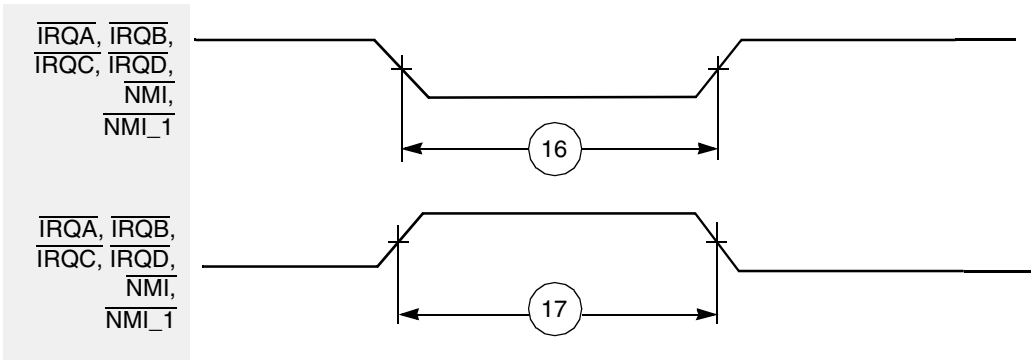


Figure 13. External Interrupt Timing Diagram (Negative Edge-Triggered)

Figure 14 shows the MODE select set up and hold timing diagram.

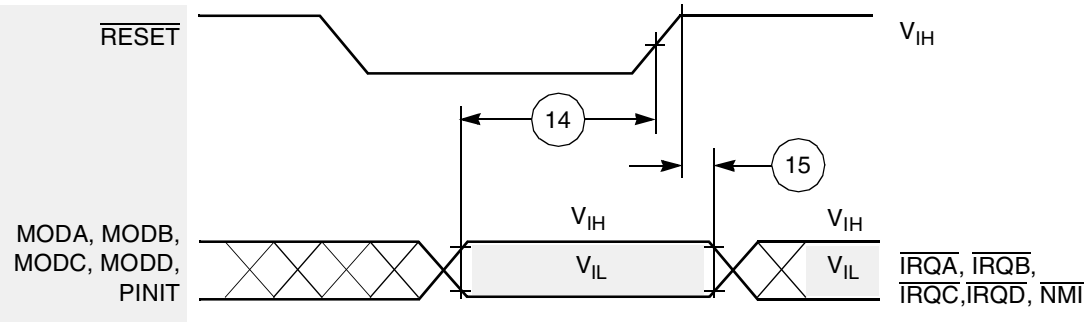


Figure 14. MODE Select Set Up and Hold Timing Diagram

2.10 Serial Host Interface (SHI) SPI Protocol Timing

Table 8 shows the SHI SPI protocol timing parameters and Figure 15 through Figure 18 show the timing diagrams.

Table 8. Serial Host Interface SPI Protocol Timing Parameters

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master	Bypassed	$10 \times T_C + 9$	59.0	—	ns
			Very Narrow	$10 \times T_C + 9$	59.0	—	ns
			Narrow	$10 \times T_C + 133$	183.0	—	ns
			Wide	$10 \times T_C + 333$	373.0	—	ns
		Slave	Bypassed	$2.0 \times T_C + 19.6$	59.2	—	ns
			Very Narrow	$2.0 \times T_C + 19.6$	59.2	—	ns
			Narrow	$2.0 \times T_C + 86.6$	193.2	—	ns
			Wide	$2.0 \times T_C + 186.6$	393.2	—	ns
XX	Tolerable Spike width on data or clock in	—	Bypassed	—	—	0	ns
			Very Narrow	—	—	10	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
24	Serial clock high period	Master	Bypassed	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Very Narrow	$0.5 \times (t_{SPICC})$	29.5	—	ns
			Narrow	$0.5 \times (t_{SPICC})$	91.5	—	ns
			Wide	$0.5 \times (t_{SPICC})$	186.5	—	ns
		Slave	Bypassed	$2.0 \times T_C + 19.6$	29.6	—	ns
			Very Narrow	$2.0 \times T_C + 19.6$	29.6	—	ns
			Narrow	$2.0 \times T_C + 86.6$	96.6	—	ns
			Wide	$2.0 \times T_C + 186.6$	196.6	—	ns

Table 8. Serial Host Interface SPI Protocol Timing Parameters (Continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	$3.0 \times T_C + 30$	—	45	ns
			Very Narrow	$3.0 \times T_C + 95$	—	110	ns
			Narrow	$3.0 \times T_C + 120$	—	135	ns
			Wide	$3.0 \times T_C + 210$	—	225	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	$2.0 \times T_C$	10	—	ns
			Very Narrow	$2.0 \times T_C + 5$	15	—	ns
			Narrow	$2.0 \times T_C + 45$	55	—	ns
			Wide	$2.0 \times T_C + 95$	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	14.0	ns
36	First SCK sampling edge to $\overline{HREQ}$ output deassertion	Slave	Bypassed	$3.0 \times T_C + 30$	45	—	ns
			Very Narrow	$3.0 \times T_C + 40$	55	—	ns
			Narrow	$3.0 \times T_C + 80$	95	—	ns
			Wide	$3.0 \times T_C + 130$	145	—	ns
37	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted (CPHA = 1)	Slave	Bypassed	$4.0 \times T_C + 30$	50.0	—	ns
			Very Narrow	$4.0 \times T_C + 40$	60.0	—	ns
			Narrow	$4.0 \times T_C + 80$	100.0	—	ns
			Wide	$4.0 \times T_C + 130$	150.0	—	ns
38	$\overline{SS}$ deassertion to $\overline{HREQ}$ output not deasserted (CPHA = 0)	Slave	—	$3.0 \times T_C + 30$	45.0	—	ns
39	$\overline{SS}$ deassertion pulse width (CPHA = 0)	Slave	—	$2.0 \times T_C$	10.0	—	ns
40	$\overline{HREQ}$ in assertion to first SCK edge	Master	Bypassed	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Very Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	49.5	—	ns
			Narrow	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	111.5	—	ns
			Wide	$0.5 \times T_{SPICC} + 3.0 \times T_C + 5$	206.5	—	ns

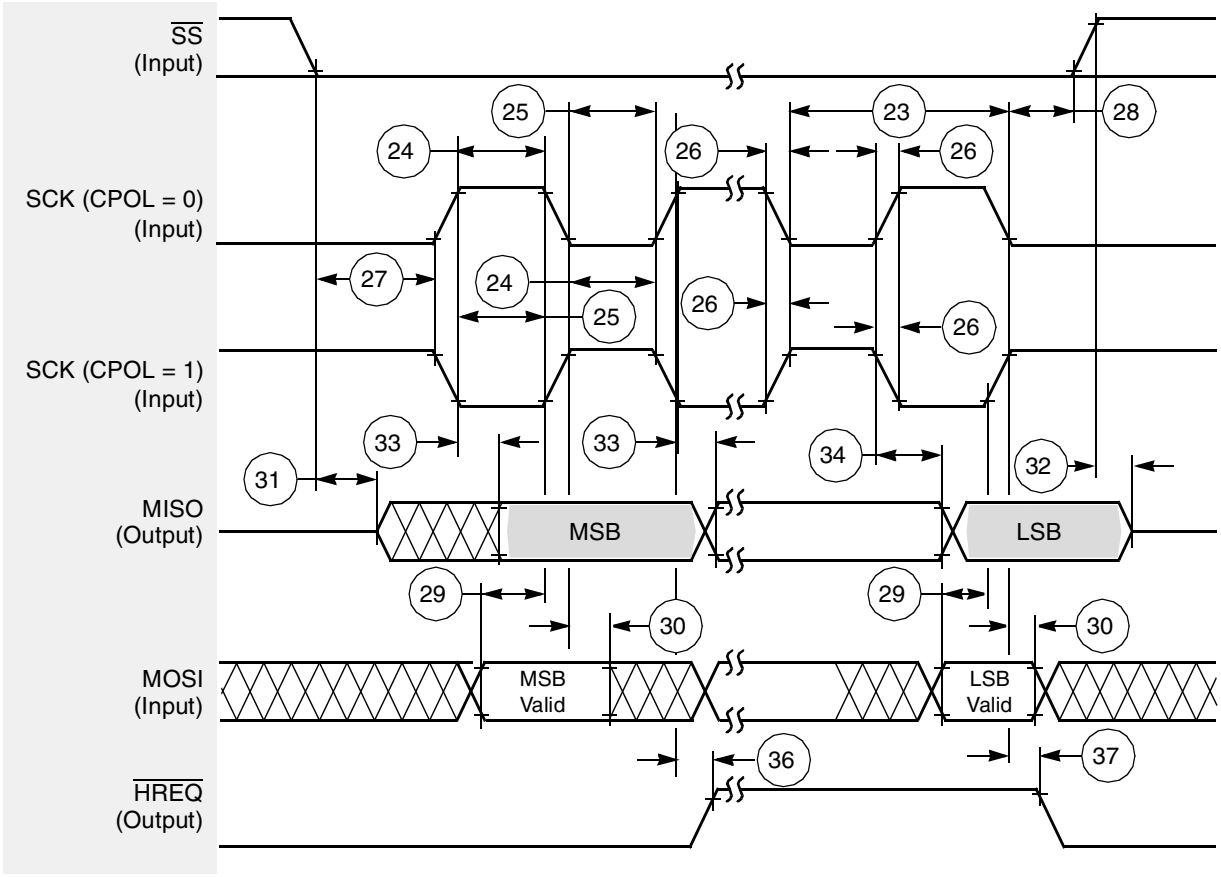


Figure 18. SPI Slave Timing Diagram (CPHA = 1)

2.11 Serial Host Interface (SHI) I²C Protocol Timing

Table 9 lists the SHI I²C protocol timing parameters and Figure 19 shows the timing diagram.

Table 9. SHI I²C Protocol Timing Parameters

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Filters enabled.	—	 — — — —	 0 10 50 100	 — — — —	 0 10 50 100	 ns ns ns ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs

Table 9. SHI I²C Protocol Timing Parameters (Continued)

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
48	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
50	SCL and SDA rise time[7]	T_R	—	1000	—	300	ns
51	SCL and SDA fall time[7]	T_F	—	5.0	—	5.0	ns
52	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
53	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
54	DSP clock frequency • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	F_{OSC}	 10.6 10.6 11.8 13.1	 — — — —	 28.5 28.5 39.7 61.0	 — — — —	 MHz MHz MHz MHz
55	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
56	Stop condition setup time	$T_{SU;STO}$	4.0	—	0.6	—	µs
57	$\overline{HREQ}$ in deassertion to last SCL edge ($\overline{HREQ}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
58	First SCL sampling edge to $\overline{HREQ}$ output deassertion[2] • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	$T_{NG;RQO}$ $4 \times T_C + 30$ $4 \times T_C + 50$ $4 \times T_C + 130$ $4 \times T_C + 230$	 — — — —	 50.0 70.0 250.0 150.0	 — — — —	 50.0 70.0 150.0 250.0	 ns ns ns ns
59	Last SCL edge to $\overline{HREQ}$ output not deasserted[2] • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled	$T_{AS;RQO}$ $2 \times T_C + 30$ $2 \times T_C + 40$ $2 \times T_C + 80$ $2 \times T_C + 130$	 40 50 90 140	 — — — —	 40 50 90 140	 — — — —	 ns ns ns ns

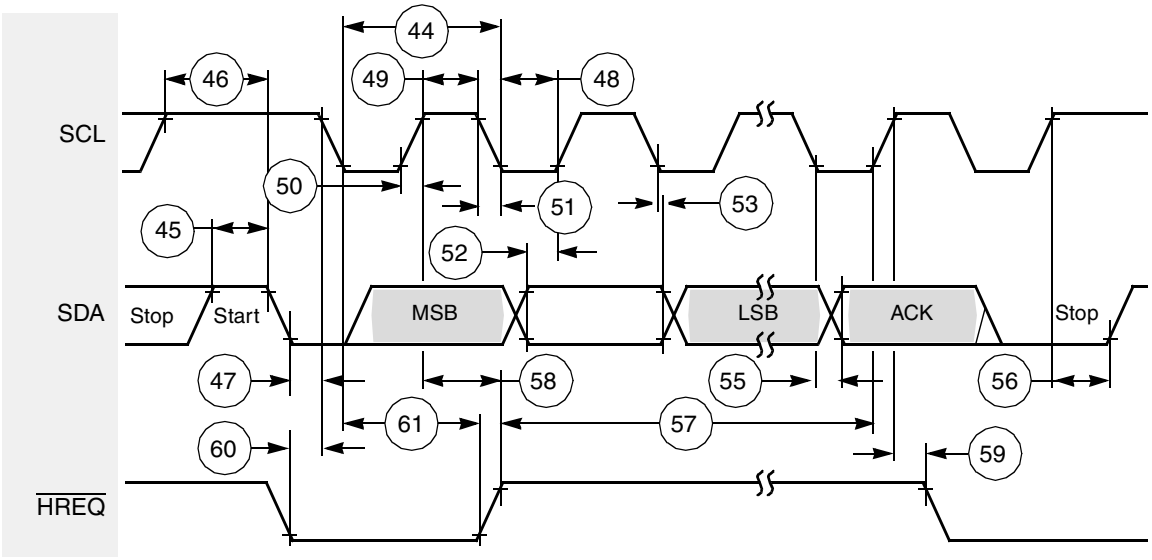


Figure 19. I²C Timing Diagram

2.13 Enhanced Serial Audio Interface (ESAI) Timing

Table 10 lists the ESAI timing parameters and Figure 20 through Figure 23 show the timing diagrams.

Table 10. Enhanced Serial Audio Interface Timing Parameters

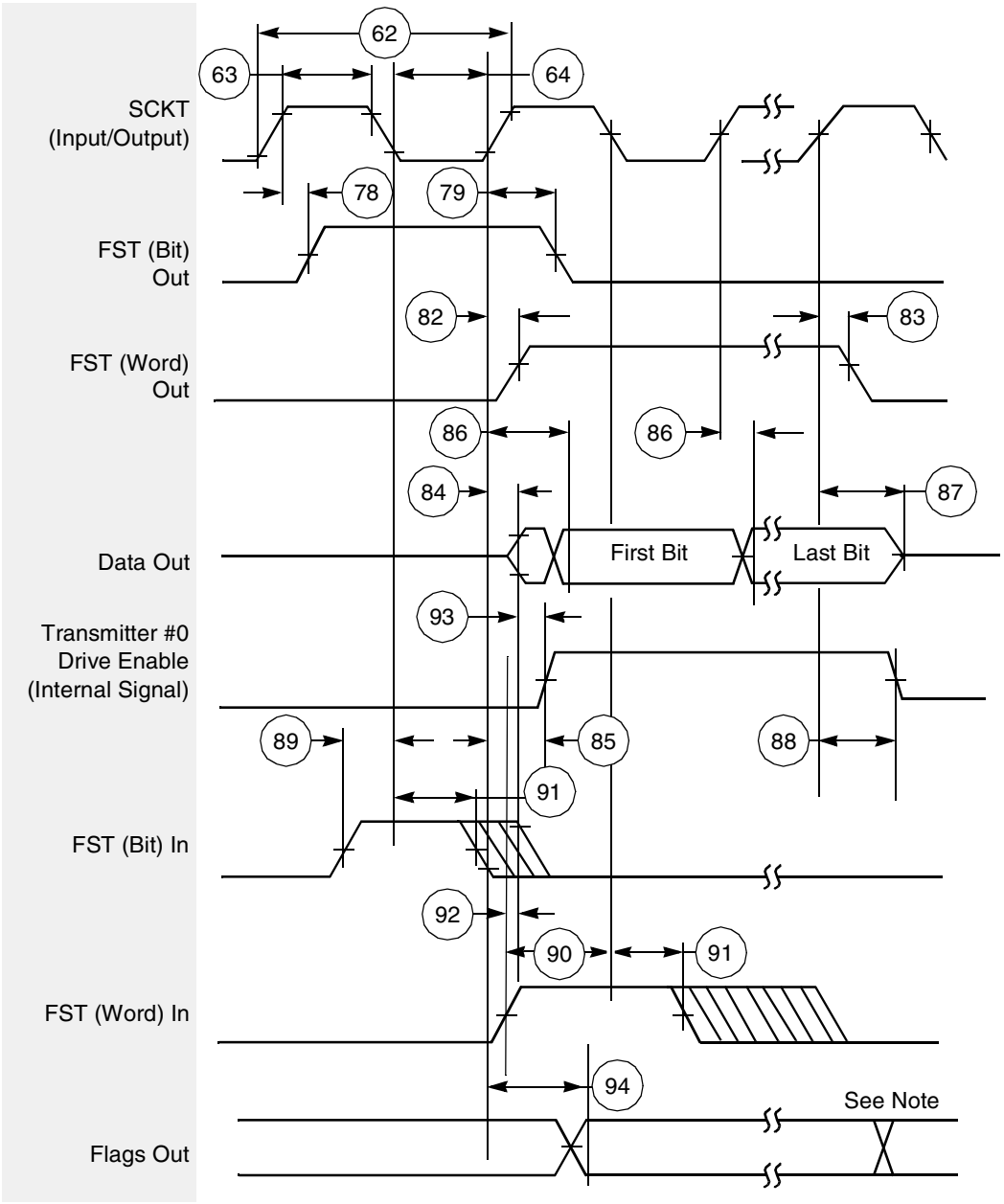
No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	20.0 20.0	— —	i ck i ck	ns
63	Clock high period • For internal clock • For external clock	— —	$2 \times T_C$ $2 \times T_C$	10 10	— —	— —	ns
64	Clock low period • For internal clock • For external clock	— —	$2 \times T_C$ $2 \times T_C$	10 10	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	—	—	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[6]	—	—	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[6]	—	—	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	—	—	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	—	—	— —	17.0 7.0	x ck i ck a	ns

Table 10. Enhanced Serial Audio Interface Timing Parameters (Continued)

No.	Characteristics[1, 3, 4]	Symbol	Expression[5]	Min	Max	Condition[2]	Unit
92	FST input (wl) to data out enable from high impedance	—	—	—	21.0	—	ns
93	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	14.0	—	ns
94	Flag output valid after SCKT rising edge	—	—	— —	14.0 9.0	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	$2 \times T_C$	10	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

Notes:

1. V_{CORE_VDD} = 1.00 ± 0.10 V; T_J = –40°C to 100°C; C_L = 50 pF.
2. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, asynchronous mode
   (Asynchronous implies that SCKT and SCKR are two different clocks.)
   i ck s = internal clock, synchronous mode
   (Synchronous implies that SCKT and SCKR are the same clock.)
3. bl = bit length
   wl = word length
   wr = word length relative
4. SCKT(SCKT pin) = transmit clock
   SCKR(SCKR pin) = receive clock
   FST(FST pin) = transmit frame sync
   FSR(FSR pin) = receive frame sync
   HCKT(HCKT pin) = transmit high frequency clock
   HCKR(HCKR pin) = receive high frequency clock
5. For the internal clock, the external clock cycle is defined by Tc and the ESAI control register.
6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
7. Periodically sampled and not 100% tested.
8. ESAI_1, ESAI_2, ESAI_3 specs match those of ESAI.



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 20. ESAI Transmitter Timing Diagram

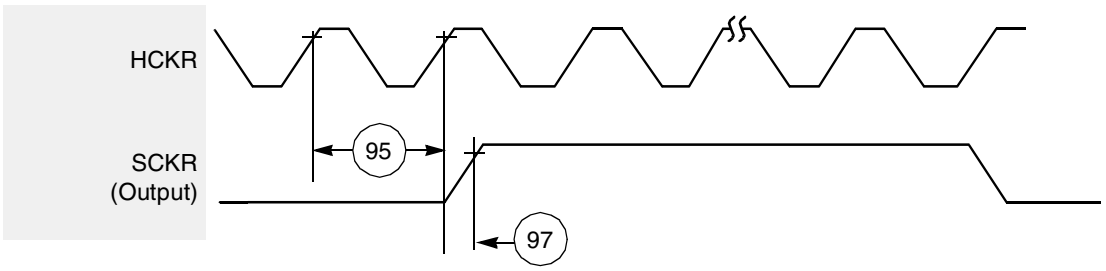


Figure 23. ESAI HCKR Timing

2.14 Timer Timing

Table 11 lists the timer timing parameters and Figure 24 shows the timing diagram.

Table 11. Timer Timing Parameters

No.	Characteristics	Expression			Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	12.0	—	ns
99	TIO High	$2 \times T_C + 2.0$	12.0	—	ns

Notes:
1. V_{CORE_VDD} = 1.00 V ± 0.10 V; T_J = –40°C to 100°C, C_L = 50 pF
2. TIMER_1 specs match those of TIMER

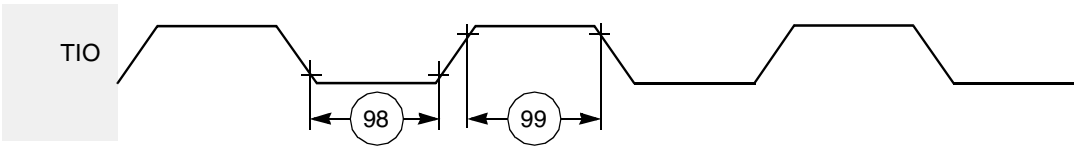


Figure 24. TIO Timer Event Input Restrictions Diagram

2.15 GPIO Timing

Table 12 lists the general purpose input and output (GPIO) timing and Figure 25 shows the timing diagram.

Table 12. GPIO Timing Parameters

No.	Characteristics[1]	Expression	Min	Max	Unit
100	Fsys edge to GPIO out valid (GPIO out delay time)[2]	—	—	7	ns
101	Fsys edge to GPIO out not valid (GPIO out hold time)[2]	—	—	7	ns
102	Fsys In valid to EXTAL edge (GPIO in set-up time)[2]	—	2	—	ns
103	Fsys edge to GPIO in not valid (GPIO in hold time)[2]	—	0	—	ns
104	Minimum GPIO pulse high width	2 × TC	10	—	ns

Table 12. GPIO Timing (Continued)Parameters (Continued)

No.	Characteristics[1]	Expression	Min	Max	Unit
105	Minimum GPIO pulse low width	2 × TC	10	—	ns
106	GPIO out rise time	—	—	13.0	ns
107	GPIO out fall time	—	—	13.0	ns

Notes:
V_{CORE_VDD} = 1.0 V ± 0.10 V; T_J = –40°C to 100°C; C_L = 50 pF

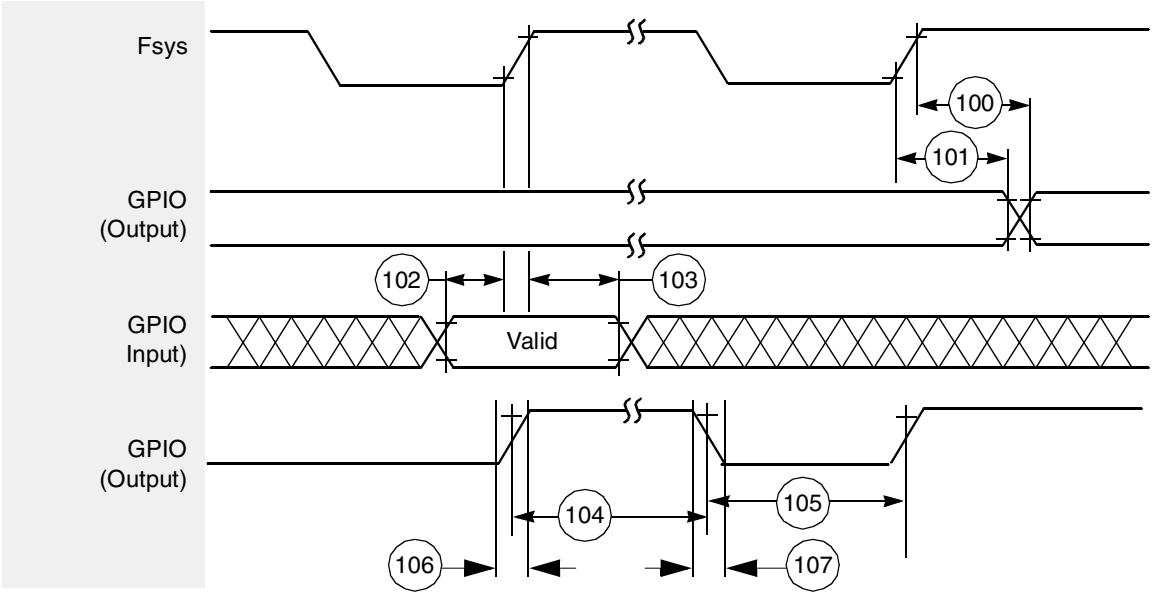


Figure 25. GPIO Timing Diagram

2.16 JTAG Timing

Table 13 lists the joint test action group (JTAG) timing parameters, and Figure 26 through Figure 28 show the timing diagrams.

Table 13. JTAG Timing Parameters

No.	Characteristics	All Frequencies		Unit
		Min	Max	
108	TCK frequency of operation (1/(T_C × 3); maximum 10 MHz)	—	10.0	MHz
109	TCK cycle time in Crystal mode	100.0	—	ns
110	TCK clock pulse width measured at 1.65 V	50.0	—	ns
111	TCK rise and fall times	—	3.0	ns
112	Boundary scan input data setup time	15.0	—	ns
113	Boundary scan input data hold time	24.0	—	ns
114	TCK low to output data valid	—	40.0	ns
115	TCK low to output high impedance	—	40.0	ns

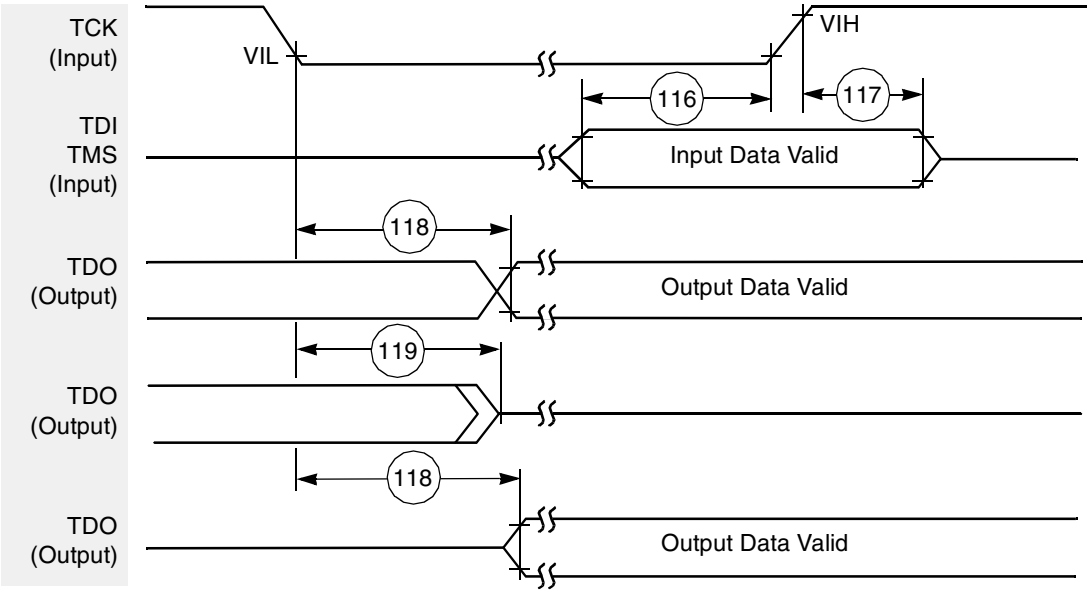


Figure 28. Test Access Port Timing Diagram

2.17 Watchdog Timer Timing

Table 14 lists the watchdog timer timing.

Table 14. Watchdog Timer Timing Parameters

No.	Characteristics	Expression	Min	Max	Unit
120	Delay from time-out to fall of $\overline{WDT}$, $\overline{WDT\_1}$	$2 \times T_C$	10.0	—	ns
121	Delay from timer clear to rise of $\overline{WDT}$, $\overline{WDT\_1}$	$2 \times Tc$	10.0	—	ns

2.18 Host Data Interface (HDI24) Timing

The HDI24 module is only on the DSP56721 device; the DSP56720 device does not have a HDI24 module. Also, only 16 bits of the HDI24 interface are pinned out on the DSP56721 device. Table 15 lists HDI24 timing and Figure 29 through Figure 35 show the timing diagrams.

Table 15. HDI24 Timing Parameters

No.	Characteristics[2]	Expression	200 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[3] $\overline{HACK}$ read assertion width	$T_C + 9.9$	14.9	—	ns
318	Read data strobe deassertion width[3] $\overline{HACK}$ read deassertion width	—	9.9	—	ns
319	Read data strobe deassertion width[3] after “Last Data Register” reads[4,5], or between two consecutive CVR, ICR, or ISR reads[6] $\overline{HACK}$ deassertion width after “Last Data Register” reads[4,5]	$2 \times T_C + 6.6$	16.6	—	ns

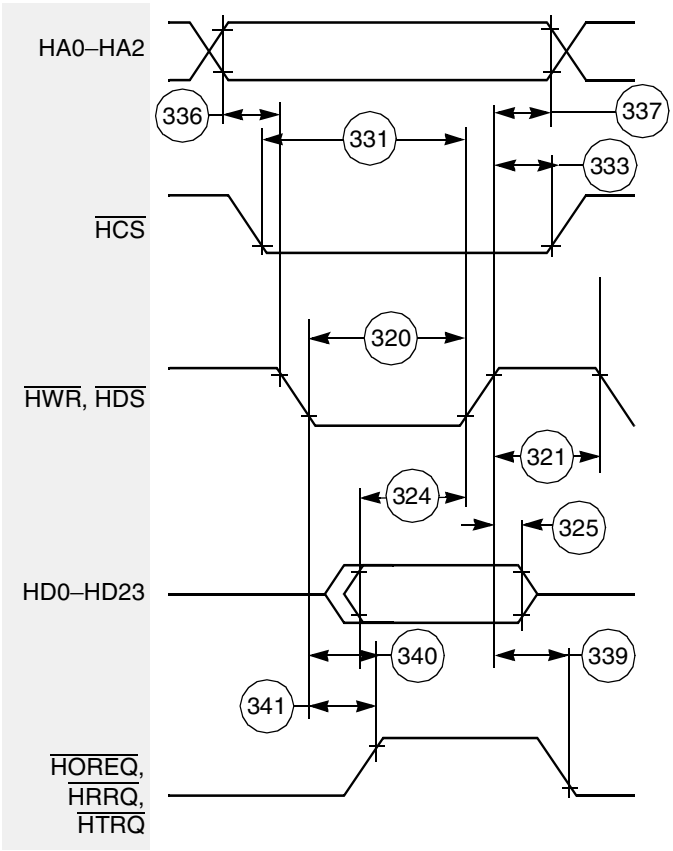


Figure 31. HDI24 Write Timing Diagram, Non-Multiplexed Bus

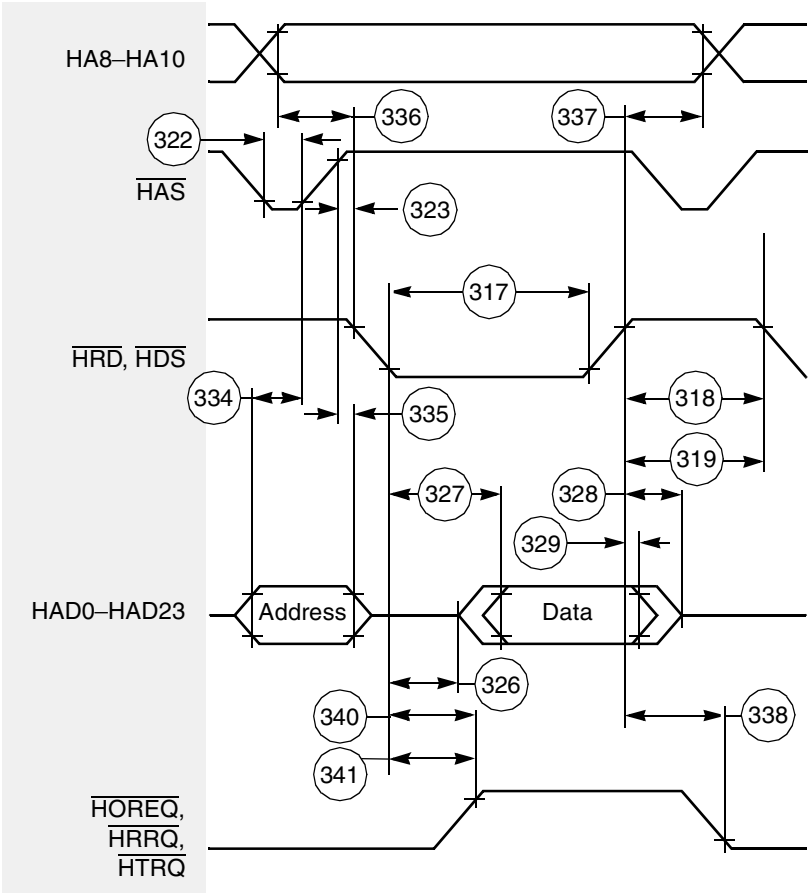


Figure 32. HDI24 Read Timing Diagram, Multiplexed Bus

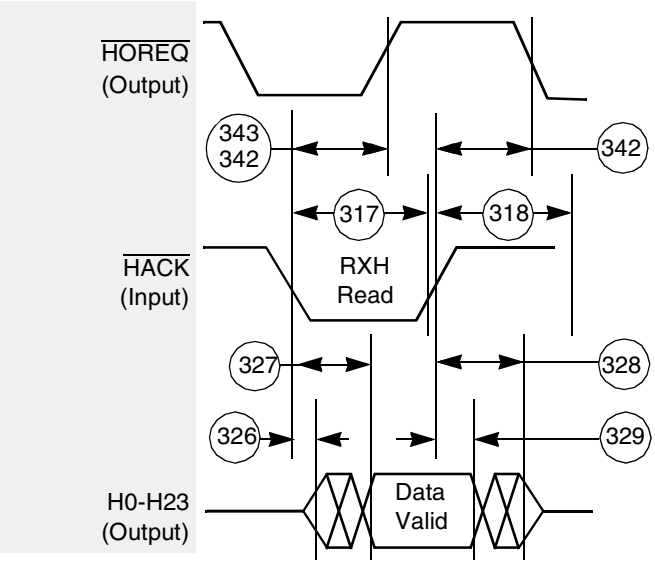


Figure 35. HDI24 Host DMA Read Timing Diagram

2.19 S/PDIF Timing

Table 16 lists the Sony/Philips Digital Interconnect Format (S/PDIF) timing parameters and Figure 36 and Figure 37 show the timing diagrams.

Table 16. S/PDIF Timing Parameters

Characteristics	Symbol	All Frequency		Unit
		Min	Max	
SPDIFIN1, SPDIFIN2, SPDIFIN3, SPDIFIN4 Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT1,SPDIFOUT2 output (Load = 50 pf) • Skew • Transition Risng • Transition Falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1, SPDIFOUT2 output (Load = 30 pf) • Skew • Transition Risng • Transition Falling	 — — —	 — — —	 1.5 13.6 18.0	ns
SRCK period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
STCLK period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

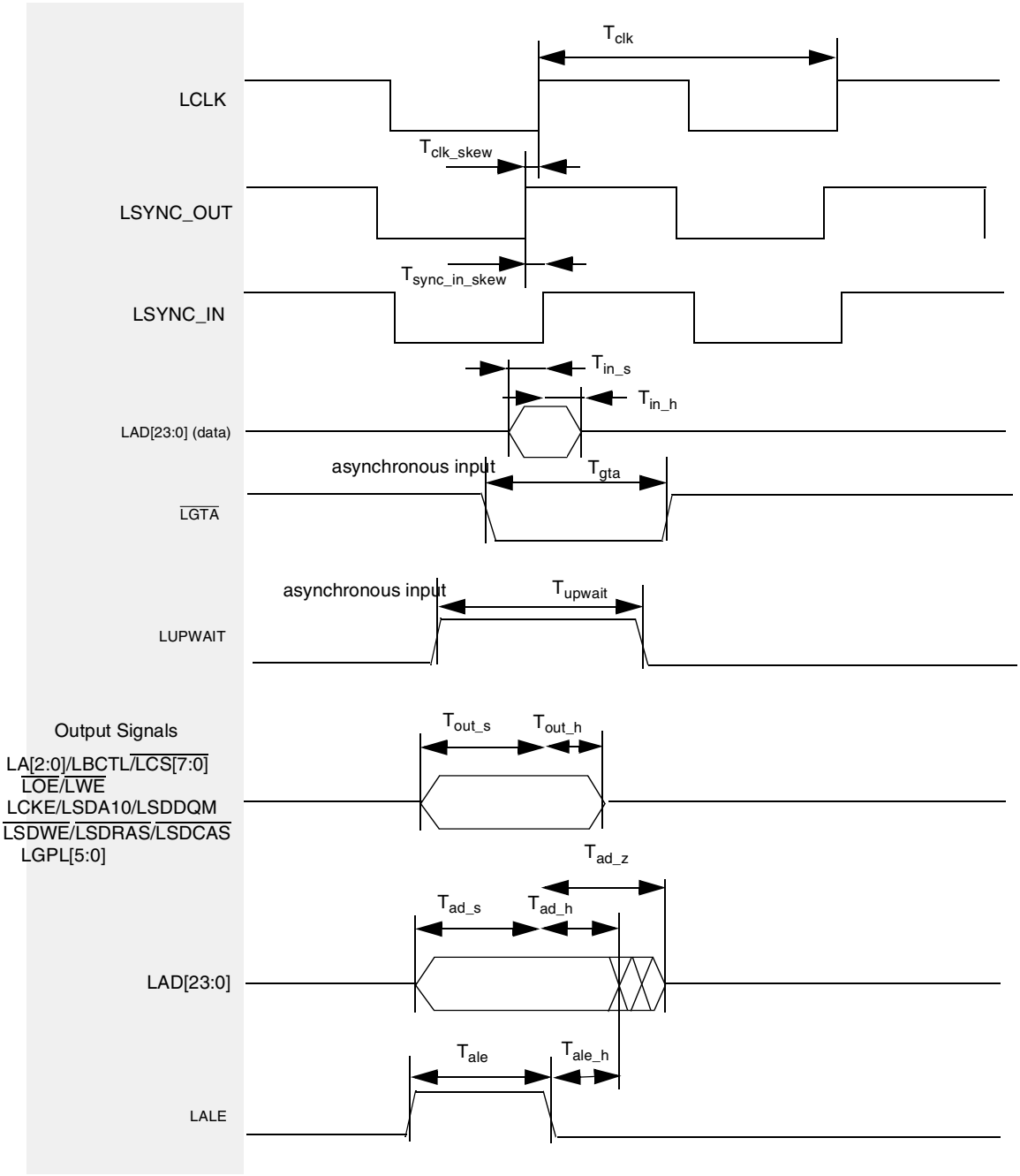


Figure 38. EMC Signals (EMC PLL Enabled; LCRR[CLKDIV] = 2)

4 Ordering Information

Table 20 provides ordering information for both the DSP56720 and DSP56721.

Table 20. Ordering Information

Device	Device Marking	Ambient Temp.	LQFP Package
DSP56720 Commercial	DSPA56720AG	0°C–70°C	20 mm × 20 mm
	DSPB56720AG	0°C–70°C	20 mm × 20 mm
	DSPC56720AG	0°C–70°C	20 mm × 20 mm
DSP56720 Automotive	DSPA56720CAG	–40°C–85°C	20 mm × 20 mm
	DSPB56720CAG	–40°C–85°C	20 mm × 20 mm
	DSPC56720CAG	–40°C–85°C	20 mm × 20 mm
DSP56721 Commercial	DSPA56721AG	0°C–70°C	20 mm × 20 mm
	DSPB56721AG	0°C–70°C	20 mm × 20 mm
	DSPC56721AG	0°C–70°C	20 mm × 20 mm
	DSPA56721AF	0°C–70°C	14 mm × 14 mm
	DSPB56721AF	0°C–70°C	14 mm × 14 mm
	DSPC56721AF	0°C–70°C	14 mm × 14 mm
DSP56721 Automotive	DSPA56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPB56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPC56721CAG	–40°C–85°C	20 mm × 20 mm
	DSPA56721CAF	–40°C–85°C	14 mm × 14 mm
	DSPB56721CAF	–40°C–85°C	14 mm × 14 mm
	DSPC56721CAF	–40°C–85°C	14 mm × 14 mm

5 Package Information

For the outline drawings of available device packages, see Table 21 and sections 5.1–5.2.

Table 21. Package Outline Drawings

Device	Package	See
DSP56720	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52
DSP56721	80-pin plastic LQFP	Figure 43 on page 51 and Figure 42 on page 50
	144-pin plastic LQFP	Figure 43 on page 51 and Figure 44 on page 52

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Document Number: DSP56720EC
Rev. 5
02/2009

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