

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Ξ·ΧΕΙ

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck128mp206t-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

dsPIC33CK256MP508 FAMILY

FIGURE 2-6: OFF-LINE UPS



REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2	 SFA: Stack Frame Active Status bit 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG 0 = Stack frame is not active; W14 and W15 address the base Data Space
bit 1	RND: Rounding Mode Select bit
	1 = Biased (conventional) rounding is enabled0 = Unbiased (convergent) rounding is enabled
bit 0	IF: Integer or Fractional Multiplier Mode Select bit
	1 = Integer mode is enabled for DSP multiply0 = Fractional mode is enabled for DSP multiply
Note 1:	This bit is always read as '0'.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	_	—	CCTXI2	CCTXI1	CCTXI0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	_	MCTXI2	MCTXI1	MCTXI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11	Unimplemented: Read as '0'
bit 10-8	CCTXI<2:0>: Current (W Register) Context Identifier bits
	111 = Reserved
	•
	•
	•
	 100 = Alternate Working Register Set 4 is currently in use 011 = Alternate Working Register Set 3 is currently in use 010 = Alternate Working Register Set 2 is currently in use 001 = Alternate Working Register Set 1 is currently in use 000 = Default register set is currently in use
bit 7-3	Unimplemented: Read as '0'
bit 2-0	MCTXI<2:0>: Manual (W Register) Context Identifier bits
	111 = Reserved
	•
	•
	•
	100 = Alternate Working Register Set 4 was most recently manually selected 011 = Alternate Working Register Set 3 was most recently manually selected 010 = Alternate Working Register Set 2 was most recently manually selected 001 = Alternate Working Register Set 1 was most recently manually selected 000 = Default register set was most recently manually selected

			-	1				
Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I/O Ports			CNEN0B	E2C	000000000000000000000000000000000000000	CNPUD	E5E	000000000000000000
ANSELA	E00	11111	CNSTATB	E2E	000000000000000000000000000000000000000	CNPDD	E60	000000000000000000
TRISA	E02	11111	CNEN1B	E30	000000000000000000000000000000000000000	CNCOND	E62	0
PORTA	E04	xxxxx	CNFB	E32	000000000000000000000000000000000000000	CNEN0D	E64	000000000000000000
LATA	E06	xxxxx	ANSELC	E38	111111	CNSTATD	E66	000000000000000000
ODCA	E08	00000	TRISC	E3A	11111111111111111	CNEN1D	E68	000000000000000000
CNPUA	E0A	00000	PORTC	E3C	*****	CNFD	E6A	000000000000000000
CNPDA	E0C	00000	LATC	E3E	*****	ANSELE	E70	1111
CNCONA	E0E	0	ODCC	E40	000000000000000000000000000000000000000	TRISE	E72	11111111111111111
CNEN0A	E10	00000	CNPUC	E42	000000000000000000000000000000000000000	PORTE	E74	*****
CNSTATA	E12	00000	CNPDC	E44	00000000000000000000	LATE	E76	*****
CNEN1A	E14	00000	CNCONC	E46	0	ODCE	E78	000000000000000000
CNFA	E16	00000	CNEN0C	E48	000000000000000000000000000000000000000	CNPUE	E7A	000000000000000000
ANSELB	E1C	11111111	CNSTATC	E4A	000000000000000000000000000000000000000	CNPDE	E7C	000000000000000000
TRISB	E1E	11111111111111111	CNEN1C	E4C	000000000000000000000000000000000000000	CNCONE	E7E	0
PORTB	E20	*****	CNFC	E4E	000000000000000000000000000000000000000	CNEN0E	E80	000000000000000000
LATB	E22	*****	ANSELD	E54	1-11	CNSTATE	E82	0000000000000000000
ODCB	E24	0000000000000000000	TRISD	E56	11111111111111111	CNEN1E	E84	0000000000000000000
CNPUB	E26	000000000000000000	PORTD	E58	*****	CNFE	E86	000000000000000000
CNPDB	E28	000000000000000000	LATD	E5A	*****	Memory BIST		
CNCONB	E2A	0	ODCD	E5C	000000000000000000000000000000000000000	MBISTCON	EFC	1

TABLE 4-15: SFR BLOCK E00h

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address values are in hexadecimal. Reset values are in binary.

5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Dual Partition Flash Program Memory" (DS70005156) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - **2:** Some registers and associated bits described in this section may not be available on all devices.

The dsPIC33CK256MP508 family devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming[™] (ICSP[™]) programming capability
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33CK256MP508 family device to be serially programmed while in the end application circuit. This is done with a Programming Clock and Programming Data (PGCx/PGDx) line, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

Enhanced In-Circuit Serial Programming uses an on-board bootloader, known as the Program Executive, to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data with a single program memory word and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1. The TBLRDL and TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes. The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



TABLE 8-10: PORTC REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSELC	—	—	—		—		—	—	ANSEL	.C<7:6>	—	—		ANSEL	C<3:0>	
TRISC								TRISC<1	15:0>							
PORTC	RC<15:0>															
LATC								LATC<1	5:0>							
ODCC								ODCC<1	5:0>							
CNPUC								CNPUC<	15:0>							
CNPDC								CNPDC<	15:0>							
CNCONC	ON	_	—	_	CNSTYLE		_	—	_	_	_	—	—	_	_	_
CNEN0C								CNEN0C<	<15:0>							
CNSTATC	CNSTATC<15:0>															
CNEN1C	CNEN1C<15:0>															
CNFC								CNFC<1	5:0>							

TABLE 8-11: PORTD REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSELD	_	_	ANSELD<13>	_	ANSELD	<11:10>	_	_	—	_	_	_			_	_
TRISD	TRISD<15:0>															
PORTD	RD<15:0>															
LATD							LATI	D<15:0>								
ODCD							ODC	D<15:0>								
CNPUD							CNPL	JD<15:0>								
CNPDD							CNPE	DD<15:0>								
CNCOND	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	_	—	—	—	—
CNEN0D							CNEN	10D<15:0>								
CNSTATD							CNSTA	\TD<15:0>	>							
CNEN1D	CNEN1D<15:0>															
CNFD							CNF	D<15:0>								

dsPIC33CK256MP508 FAMILY

FIGURE 10-1: DMA FUNCTIONAL BLOCK DIAGRAM



NOTES:

12.2 Architecture Overview

The PWM module consists of a common set of controls and features, and multiple instantiations of PWM Generators (PGs). Each PWM Generator can be independently configured or multiple PWM Generators can be used to achieve complex multiphase systems. PWM Generators can also be used to implement sophisticated triggering, protection and logic functions. A high-level block diagram is shown in Figure 12-1.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLMOD	SWAP	OVRENH	OVRENL	OVRDAT1	OVRDAT0	OSYNC1	OSYNC0
bit 15				I		1	bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	FFDAT1	FFDAT0	DBDAT1	DBDAT0
bit 7					•	·	bit 0
Legend:							
R = Readal	ble bit	W = Writable	bit	U = Unimplen	nented bit, read a	is '0'	
-n = Value a	at POR	'1' = Bit is set	:	'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15	CLMOD: Cu	rrent-Limit Mo	de Select bit				
	1 = If PCI cu	urrent limit is a	ctive, then the	PWMxH and P	WMxL output sig	nals are inverte	ed (bit flipping),
	and the $0 = f PC c$	CLDAI <1:0> I	oits are not use	ed CLDAT<1:0> bi	ts define the P\//	M output levels	
hit 14	SWAP: Swa	n PWM Signal	s to PWMxH a	nd PWMxL Dev	ice Pins hit		
	1 = The PW	MxH signal is co	onnected to the	PWMxI pin and	the PWMxL signa	l is connected to	the PWMxH pin
	0 = PWMxH	I/L signals are	mapped to the	ir respective pin	IS		
bit 13	OVRENH: U	ser Override E	nable for PWN	/IxH Pin bit			
	1 = OVRDA	T1 provides da	ata for output o	n the PWMxH p	vin		
	0 = PWM G	enerator provid	des data for the	e PWMxH pin			
bit 12	OVRENL: U	ser Override E	nable for PWM	1xL Pin bit			
	1 = OVRDA	T0 provides da enerator provid	ita for output o	n the PWMxL p	in		
hit 11-10		0> Data for P		Pins if Overrid	e is Enabled hits		
	If OVERENE	I = 1, then OV	RDAT1 provide	s data for PWM			
	If OVERENL	= 1, then OVF	RDAT0 provide	s data for PWM	xL.		
bit 9-8	OSYNC<1:0	>: User Outpu	t Override Syn	chronization Co	ntrol bits		
	11 = Reserv	ed					
		utput override	s via the OVR	ENH/L and O	/RDAT<1:0> bits	occur when sp	pecified by the
	01 = User of	utput overrides	via the OVRE	ENH/L and OVF	RDAT<1:0> bits c	occur immediate	ly (as soon as
	possibl	e)					5
	00 = User ou	utput overrides	via the OVREN	NH/L and OVRD	AT<1:0> bits are	synchronized to	the local PWM
hit 7 C		ise (next Start-		Dipa if Coult Cu	ant in Antivo hito		
DIL 7-0	If Fault is act	J>: Data for PV		PINS IF FAULT EV			
	If Fault is act	tive, then FLTE	AT1 provides	data for PWMxI			
bit 5-4	CLDAT<1:0	>: Data for PW	MxH/PWMxL I	Pins if Current-L	imit Event is Acti	ve bits	
	If current lim	it is active, the	n CLDAT1 prov	vides data for P	WMxH.		
	If current lim	it is active, the	n CLDAT0 prov	vides data for P	WMxL.		
bit 3-2	FFDAT<1:0>	Data for PW	MxH/PWMxL F	Pins if Feed-For	ward Event is Act	tive bits	
	If feed-forwa	rd is active, the	en FFDAT1 pro	ovides data for F	PWMxH.		
hit 1 0					·vviviXL. Iodo is Activo hita		
		Data 101 PM	d device balter		provides data fo	r PWMxH	
	If Debug mo	de is active an	d device halted	I, then DBDAT0	provides data fo	r PWMxL.	

REGISTER 12-15: PGxIOCONL: PWM GENERATOR x I/O CONTROL REGISTER LOW

13.0 HIGH-SPEED, 12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- Note 1: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "12-Bit High-Speed, Multiple SARs A/D Converter (ADC)" (DS70005213) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33CK256MP508 devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and oversampling capabilities to improve performance in AC/DC, DC/DC power converters. The devices implement the ADC with three SAR cores, two dedicated and one shared.

13.1 ADC Features Overview

The High-Speed, 12-Bit Multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- Three ADC Cores: Two Dedicated Cores and One Shared (common) Core
- User-Configurable Resolution of up to 12 Bits for each Core
- Up to 3.5 Msps Conversion Rate per Channel at 12-Bit Resolution
- Low-Latency Conversion
- Up to 24 Analog Input Channels, with a Separate 16-Bit Conversion Result Register for each Input
- Conversion Result can be Formatted as Unsigned or Signed Data, on a per Channel Basis, for All Channels

- Simultaneous Sampling of up to 3 Analog Inputs
- Channel Scan Capability
- Multiple Conversion Trigger Options for each Core, including:
 - PWM triggers from CPU cores
 - MCCP/SCCP modules triggers
 - CLC modules triggers
 - External pin trigger event (ADTRG31)
 - Software trigger
- Four Integrated Digital Comparators with Dedicated Interrupts:
 - Multiple comparison options
 - Assignable to specific analog inputs
- Four Oversampling Filters with Dedicated Interrupts:
 - Provide increased resolution
 - Assignable to a specific analog input

The module consists of three independent SAR ADC cores. Simplified block diagrams of the Multiple SARs 12-Bit ADC are shown in Figure 13-1 and Figure 13-2.

The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S&H) circuit of each ADC core. The core uses the channel information (the output format, the Measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input, and passed to the digital filter and digital comparator if they were configured to use data from this particular channel.

The ADC module can sample up to three inputs at a time (two inputs from the dedicated SAR cores and one from the shared SAR core). If multiple ADC inputs request conversion on the shared core, the module will convert them in a sequential manner, starting with the lowest order input.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

REGISTER 15-11: INTxTMRL: INTERVAL x TIMER REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			INTTN	/IR<15:8>						
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			INTTI	MR<7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'						
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown			

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INTxTMR) bits

REGISTER 15-12: INTxTMRH: INTERVAL x TIMER REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			INTTM	IR<31:24>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			INTTM	IR<23:16>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			oit	U = Unimplemented bit, read as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	red	x = Bit is unknown		

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INTxTMR) bits

REGISTER 16-11: UxP3: UARTx TIMING PARAMETER 3 REGISTE
--

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			P3<	15:8>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			P3•	<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unkn			nown		
bit 15-0	P3<15:0>: Pa	arameter 3 bits						
	<u>DMX RX:</u> The last byte number to receive – 1, not including Start code (bits<8:0>).							
	LIN Slave RX: Number of bytes to receive (bits<7:0>).							
Asynchronous RX: Used to mask the UxP2 address bits; 1 = P2 address bit is used, 0 = P2 address bit is masked off (bits<7:0>).								
	Smart Card N Waiting Time	<u>/lode:</u> Counter bits (bits	s<15:0>).					
	Other Modes Not used.	<u>.</u>						

REGISTER 16-12: UxP3H: UARTx TIMING PARAMETER 3 REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—	—	—	-	—	—		
bit 15							bit 8		
r									
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			P3<2	23:16>					
bit 7 bi									
Legend:									
R = Readab	le bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown		
bit 15-8	Unimplemented: Read as '0'								
bit 7-0	P3<23:16>: F	Parameter 3 Hig	h bits						
	Smart Card N	<u>/lode:</u>							
	Waiting Time	Counter bits (bi	its<23:16>).						
	Other Modes	<u>.</u>							
	Not used.								

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	
—	— — FRMERREN			BUSYEN	—	—	SPITUREN	
bit 15								
R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	
SRMTEN	SPIROVEN	SPIRBEN		SPITBEN		SPITBFEN	SPIRBFEN	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	1 as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown	
bit 15-13	Unimplemen	ted: Read as '	כי					
bit 12	FRMERREN:	Enable Interru	pt Events via F	RMERR bit				
	1 = Frame err 0 = Frame err	or generates a or does not ge	n interrupt ever nerate an interr	nt rupt event				
bit 11	BUSYEN: En	able Interrupt E	Events via SPIB	USY bit				
	1 = SPIBUSY generates an interrupt event							
bit 10-9	Unimplemented: Read as '0'							
bit 8	SPITUREN: Enable Interrupt Events via SPITUR bit							
	1 = Transmit Underrun (TUR) generates an interrupt event 0 = Transmit Underrun does not generate an interrupt event							
bit 7	SRMTEN: En	able Interrupt E	Events via SRM	IT bit				
	1 = Shift Register Empty (SRMT) generates interrupt events 0 = Shift Register Empty does not generate interrupt events							
bit 6	SPIROVEN:	Enable Interrup	t Events via SF	PIROV bit				
	1 = SPIx Rece	eive Overflow (ROV) generate	s an interrupt e	event			
	0 = SPIx Rec	eive Overflow o	loes not genera	ate an interrupt	event			
bit 5	SPIRBEN: Enable Interrupt Events via SPIRBE bit							
	 1 = SPIx RX buffer empty generates an interrupt event 0 = SPIx RX buffer empty does not generate an interrupt event 							
bit 4	Unimplemented: Read as '0'							
bit 3	SPITBEN: Enable Interrupt Events via SPITBE bit							
	 1 = SPIx transmit buffer empty generates an interrupt event 0 = SPIx transmit buffer empty does not generate an interrupt event 							
bit 2	Unimplemented: Read as '0'							
bit 1	SPITBFEN: Enable Interrupt Events via SPITBF bit							
	 1 = SPIx transmit buffer full generates an interrupt event 0 = SPIx transmit buffer full does not generate an interrupt event 							
bit 0	SPIRBFEN: Enable Interrupt Events via SPIRBF bit							
	1 = SPIx rece	ive buffer full g	enerates an int	errupt event				
	0 = SPIx rece	ive buffer full d	oes not genera	te an interrupt	event			

REGISTER 17-6: SPIxIMSKL: SPIx INTERRUPT MASK REGISTER LOW

dsPIC33CK256MP508 FAMILY

FIGURE 20-1: SENTX MODULE BLOCK DIAGRAM

FIGURE 20-2: SENTX PROTOCOL DATA FRAMES

Sync F	Period Status	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	CRC	Pause (optional)	\downarrow
56	6 12-27	12-27	12-27	12-27	12-27	12-27	12-27	12-27	12-768	I

OETRIG OSCNT2 OSCNT1 OSCNT0 — OUTM2 ⁽¹⁾ DUTM2 ⁽¹⁾ </th <th>R/W-0</th> <th>R/W-0</th> <th>R/W-0</th> <th>R/W-0</th> <th>U-0</th> <th>R/W-0</th> <th>R/W-0</th> <th>R/W-0</th>	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 - - POLACE POLBDF ⁽¹⁾ PSSACE1 PSSACE0 PSSBDF1 ⁽¹⁾ PSSBDF0 ⁽¹⁾ bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'	OFTRIG	OSCNT2	OSCNT1	OSCNTO		OUTM2 ⁽¹⁾	OUTM1 ⁽¹⁾	
U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 - - POLACE POLBDF ⁽¹⁾ PSSACE1 PSSACE0 PSSBDF1 ⁽¹⁾ PSSBDF0 ⁽¹⁾ bit 7 - - POLACE POLBDF ⁽¹⁾ PSSACE1 PSSACE0 PSSBDF1 ⁽¹⁾ PSSBDF0 ⁽¹⁾ bit 7 - - - - - bit 0 Legend: - - - - - - - - - bit 0 Legend: - - - - - - - - - bit 0 Legend: - - - - - - - - - bit 0 Legend: - - - - - - - - - bit 0 Legend: -	bit 15	0001112	000111	0001110		0011112	001111	bit 8
U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 POLACE POLBDF ⁽¹⁾ PSSACE1 PSSACE0 PSSBDF1 ⁽¹⁾ PSSBDF0 ⁽¹⁾ bit 7 POLACE POLBDF ⁽¹⁾ PSSACE1 PSSACE0 PSSBDF1 ⁽¹⁾ PSSBDF0 ⁽¹⁾ bit 7 bit 0 Legend: bit 0								
- POLACE POLBDF ⁽¹⁾ PSSACE1 PSSACE0 PSSBDF1 ⁽¹⁾ PSSBDF0 ⁽¹⁾ bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 OETRIG: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 10 = Extends one-shot event by 7 time base periods (8 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 3 time base periods (6 time base periods total) 101 = Extends one-shot event by 3 time base periods (1 time base periods total) 101 = Extends one-shot event by 2 time base periods (2 time base periods total) 101 = Extends one-shot event by 1 time base periods (2 time base periods total) 001 = Extends one-shot event by 2 time base periods (2 time base periods total) 101 = Extends one-shot event by 1 time base periods (2 time base periods total) 010 = Extends one-shot event by 1 time base periods (2 time base periods total) 101 = Extends one-shot event by 1 time base periods (2 time base periods total)	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 OETRIG: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCNT<2:0: One-Shot Event Count bits		—	POLACE	POLBDF ⁽¹⁾	PSSACE1	PSSACE0	PSSBDF1 ⁽¹⁾	PSSBDF0 ⁽¹⁾
Legend: W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 OETRIG: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCNT<2:0>: One-Shot Event Count bits 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 100 = Extends one-shot event by 6 time base periods (6 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 100 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 2 time base periods (3 time base periods total) 000 = Extends one-shot event by 2 time base periods (2 time base periods total) 001 = Extends one-shot event by 2 time base periods (3 time base periods total) 001 = Extends one-shot event by 2 time base periods (2 time base periods total) 001 = Extends one-shot event by 1 time base period (2 time base periods total) 001 = Extends one-shot event by 1 time base periods (3 time base periods total) 001 = Extends one-shot event by 1 time base periods (2 time base periods total) 001 = Extends one-shot event by 1 time base periods (2 time base periods total) 010 = Does not extend one-shot Trigger event 111 = Reserved 111 111 = Reserved 1	bit 7		•			•	•	bit 0
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 OETRIG: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCNT<2:0>: One-Shot Event Count bits 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 100 = Extends one-shot event by 6 time base periods (7 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 102 = Extends one-shot event by 5 time base periods (6 time base periods total) 103 = Extends one-shot event by 3 time base periods (6 time base periods total) 104 = Extends one-shot event by 3 time base periods (6 time base periods total) 105 = Extends one-shot event by 3 time base periods (6 time base periods total) 106 = Extends one-shot event by 2 time base periods (6 time base periods total) 107 = Extends one-shot event by 2 time base periods (7 time base periods total) 108 = Extends one-shot event by 2 time base periods (7 time base periods total) 109 = Does not extend one-shot Trigger event bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits ⁽¹⁾ 111 = Reserved 110 = Output Scan mode 111 = Reserved 110 = Brush DC Output mode, forward 110 = Brush DC Output mode, forward 110 = Brush DC Output mode 110 = Push-Pull Output mode 111 = Reserved 112 = Reserved 113 = Reserved 114 = Reserved 115 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-low 1 = Output pin polarity is active-low								
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 OETRIG: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCNT<2:0>: One-Shot Event Count bits 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 100 = Extends one-shot event by 5 time base periods (5 time base periods total) 101 = Extends one-shot event by 4 time base periods (6 time base periods total) 001 = Extends one-shot event by 2 time base periods (5 time base periods total) 010 = Extends one-shot event by 2 time base periods (2 time base periods total) 001 = Extends one-shot event by 2 time base periods (2 time base periods total) 010 = Extends one-shot event by 1 time base period (2 time base periods total) 001 = Extends one-shot event by 1 time base period (2 time base periods total) 010 = Extends one-shot event by 5 time base period (2 time base periods total) 001 = Extends one-shot event by 5 time base period (2 time base periods total) 010 = Bush DC Output Mode 011 = Reserved 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode	Legend:							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 OETRIG: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCNT<2:0>: One-Shot Event Count bits 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 100 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 5 time base periods (3 time base periods total) 101 = Extends one-shot event by 5 time base periods (3 time base periods total) 001 = Extends one-shot event by 2 time base periods (3 time base periods total) 010 = Extends one-shot event by 1 time base periods (3 time base periods total) 001 = Extends one-shot event by 1 time base periods (3 time base periods total) 001 = Extends one-shot event by 1 time base periods (3 time base periods total) 001 = Extends one-shot event by 1 time base periods (5 time base periods total) 001 = Extends one-shot event by 2 time base 0'' = Bit is zerved 110 = Output Scan mode 111 = Reserved 111 = Reserved 111 = Reserved 102 = Brush DC Output mode, forward 100 = Brush DC Output mode 001 = Haif-Bridge Output mode 001 = Haif-Bridge Output mode	R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
bit 15 OETRIG: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCNT-2:0:: One-Shot Event Count bits 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 110 = Extends one-shot event by 6 time base periods (7 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 4 time base periods (5 time base periods total) 011 = Extends one-shot event by 4 time base periods (6 time base periods total) 011 = Extends one-shot event by 2 time base periods (3 time base periods total) 010 = Extends one-shot event by 1 time base periods (3 time base periods total) 010 = Does not extend one-shot Trigger event bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits ⁽¹⁾ 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, forward 100 = Brush DC Output mode 011 = Reserved 012 = Half-Bridge Output mode 013 = Half-Bridge Output mode 014 = Reserved 115 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit ⁽¹⁾ 1 = Output pin polarity is active-low	-n = Value at I	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15 OETRIC: CCPx Dead-Time Select bit 1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCMT<2:0>: One-Shot Event Count bits 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 4 time base periods (5 time base periods total) 101 = Extends one-shot event by 4 time base periods (5 time base periods total) 010 = Extends one-shot event by 2 time base periods (3 time base periods total) 011 = Extends one-shot event by 2 time base periods (3 time base periods total) 010 = Extends one-shot event by 1 time base period (2 time base periods total) 010 = Extends one-shot event by 1 time base period (2 time base periods total) 010 = Extends one-shot event by 1 time base period (2 time base periods total) 010 = Extends one-shot event by 1 time base period (2 time base periods total) 010 = Does not extend one-shot Trigger event bit 10 Unimplemented: Read as '0' bit 10 = 0 utput Scan mode 101 = Brush DC Output mode, reverse 011 = Reserved 010 = Brush DC Output mode 010 = Brush DC Output mode 011 = Reserved								
 is Pot Inggered mode (IRRGEN = 1): Module does not drive enabled output pins until triggered 0 = Normal output pin operation bit 14-12 OSCNT<2:0>: One-Shot Event Count bits = Extends one-shot event by 7 time base periods (8 time base periods total) 10 = Extends one-shot event by 5 time base periods (7 time base periods total) 10 = Extends one-shot event by 5 time base periods (6 time base periods total) 10 = Extends one-shot event by 5 time base periods (6 time base periods total) 001 = Extends one-shot event by 2 time base periods (4 time base periods total) 001 = Extends one-shot event by 2 time base periods (4 time base periods total) 001 = Extends one-shot event by 1 time base periods (3 time base periods total) 001 = Extends one-shot event by 1 time base periods (4 time base periods total) 001 = Extends one-shot event by 1 time base periods (4 time base periods total) 001 = Extends one-shot event by 1 time base periods (4 time base periods total) 001 = Extends one-shot event by 1 time base periods (4 time base periods total) 001 = Extends one-shot event by 1 time base periods (4 time base periods total) 001 = Extends one-shot event by 1 time base periods (4 time base periods total) 000 = Does not extend one-shot Trigger event Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits⁽¹⁾ 11 = Reserved 10 = Output mode, forward 10 = Output mode 01 = Brush DC Output mode 01 = Brush DC Output mode 01 = Haif-Bridge Output mode 01 = Push-Pull Output mode 01 = Push-Pull Output mode 01 = Push-Pull Output pins, OCMxA, OCMxC and OCMxE, Polarity Control bit	bit 15	OETRIG: CCI	Px Dead-Time	Select bit		المعاملة والمعالم		l fui a a a d
bit 14-12 OSCNT<2:0>: One-Shot Event Count bits 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 100 = Extends one-shot event by 5 time base periods (7 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 100 = Extends one-shot event by 4 time base periods (5 time base periods total) 100 = Extends one-shot event by 4 time base periods (4 time base periods total) 100 = Extends one-shot event by 2 time base periods (3 time base periods total) 100 = Extends one-shot event by 1 time base periods (3 time base periods total) 100 = Extends one-shot event by 1 time base periods (2 time base periods total) 100 = Does not extend one-shot Trigger event bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits ⁽¹⁾ 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output mode 11 = Output pin polarity is active-low 01 = Output pin polarity is active-low 01 = Output pin polarity is active-low		1 = For Triggeneration = Normal o	erea moae (1 k utput pin opera	(GEN = 1): NO	aule does not	drive enabled (output pins until	i triggered
 111 = Extends one-shot event by 7 time base periods (8 time base periods total) 110 = Extends one-shot event by 5 time base periods (6 time base periods total) 101 = Extends one-shot event by 4 time base periods (6 time base periods total) 100 = Extends one-shot event by 4 time base periods (5 time base periods total) 111 = Extends one-shot event by 2 time base periods (3 time base periods total) 112 = Extends one-shot event by 2 time base periods (3 time base periods total) 113 = Extends one-shot event by 1 time base periods (3 time base periods total) 114 = Extends one-shot event by 1 time base periods (2 time base periods total) 115 = Extends one-shot event by 1 time base periods (3 time base periods total) 116 = Extends one-shot event by 1 time base periods (2 time base periods total) 111 = Extends one-shot event by 1 time base periods (2 time base periods total) 112 = Extends one-shot event by 1 time base periods (3 time base periods total) 113 = Extends one-shot event by 1 time base periods (3 time base periods total) 114 = Extends one-shot event by 1 time base periods (2 time base periods total) 115 = Output Scan mode 111 = Reserved 111 = Reserved 112 = Reserved 113 = Reserved 114 = Reserved 115 = Push-Pull Output mode 115 = PoLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 11 = Output pin polarity is active-low 0 = Output pin polarity is active-low 	bit 14-12	OSCNT<2:0>	: One-Shot Ev	ent Count bits				
 110 = Extends one-shot event by 6 time base periods (7 time base periods total) 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 100 = Extends one-shot event by 4 time base periods (5 time base periods total) 011 = Extends one-shot event by 2 time base periods (4 time base periods total) 010 = Extends one-shot event by 2 time base periods (2 time base periods total) 001 = Extends one-shot event by 1 time base periods (2 time base periods total) 000 = Does not extend one-shot Trigger event bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits⁽¹⁾ 111 = Reserved 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-low 1 = Output pin polarity is active-low 		111 = Extend	s one-shot eve	nt by 7 time ba	se periods (8 t	ime base perio	ds total)	
 101 = Extends one-shot event by 5 time base periods (6 time base periods total) 100 = Extends one-shot event by 3 time base periods (4 time base periods total) 011 = Extends one-shot event by 2 time base periods (3 time base periods total) 010 = Extends one-shot event by 1 time base periods (2 time base periods total) 001 = Extends one-shot event by 1 time base period (2 time base periods total) 000 = Does not extend one-shot Trigger event bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits⁽¹⁾ 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode 111 = Output pin polarity is active-low 011 = Output pin polarity is active-low 		110 = Extend	s one-shot eve	nt by 6 time ba	se periods (7 t	ime base perio	ds total)	
 bit 10 = Extends one-shot event by 3 time base periods (4 time base periods total) 010 = Extends one-shot event by 2 time base periods (3 time base periods total) 010 = Extends one-shot event by 1 time base periods (2 time base periods total) 001 = Extends one-shot event by 1 time base periods (2 time base periods total) 000 = Does not extend one-shot Trigger event bit 11 Unimplemented: Read as '0' bit 10-8 OUTM DUTM 2:0>: PWMx Output Mode Control bits⁽¹⁾ 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-low 0 = Output pin polarity is active-low 		101 = Extend	s one-shot eve	nt by 5 time ba	se periods (6 ti se periods (5 ti	ime base perio ime base perio	ds total) ds total)	
010 = Extends one-shot event by 2 time base periods (3 time base periods total) 001 = Extends one-shot event by 1 time base period (2 time base periods total) 000 = Does not extend one-shot Trigger event bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits ⁽¹⁾ 111 = Reserved 100 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output mode 000 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-low		011 = Extend	s one-shot eve	nt by 3 time ba	se periods (3 t	ime base perio	ds total)	
 bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits⁽¹⁾ 111 = Reserved 101 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-low 1 = Output pin polarity is active-low 		010 = Extend	s one-shot eve	nt by 2 time ba	se periods (3 t	ime base perio	ds total)	
 bit 11 Unimplemented: Read as '0' bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits⁽¹⁾ 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-low bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit⁽¹⁾ 1 = Output pin polarity is active-low 		001 = Extend	s one-shot eve	nt by 1 time ba	se period (2 tir	ne base period	ls total)	
bit 10-8 OUTM<2:0>: PWMx Output Mode Control bits ⁽¹⁾ 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit ⁽¹⁾ 1 = Output pin polarity is active-low	bit 11		ted: Read as '	n'	Chi			
 111 = Reserved 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit⁽¹⁾ 1 = Output pin polarity is active-low 	bit 10-8	OUTM<2:0>:	PWMx Output	Mode Control I	oits ⁽¹⁾			
 110 = Output Scan mode 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit⁽¹⁾ 1 = Output pin polarity is active-low 		111 = Reserv	red					
 101 = Brush DC Output mode, forward 100 = Brush DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit⁽¹⁾ 1 = Output pin polarity is active-low 		110 = Output	Scan mode					
 bit 300 = bitsin DC Output mode, reverse 011 = Reserved 010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit⁽¹⁾ 1 = Output pin polarity is active-low 		101 = Brush [DC Output mod	le, forward				
010 = Half-Bridge Output mode 001 = Push-Pull Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit ⁽¹⁾ 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high		011 = Reserv	ed					
001 = Push-Pull Output mode 000 = Steerable Single Output mode bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit ⁽¹⁾ 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high		010 = Half-Br	idge Output mo	ode				
bit 7-6 Unimplemented: Read as '0' bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit ⁽¹⁾ 1 = Output pin polarity is active-low		001 = Push-P	Pull Output mod	le ut mode				
bit 5 POLACE: CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit 1 = Output pin polarity is active-low 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit ⁽¹⁾ 1 = Output pin polarity is active-low	bit 7.6		ted: Bood as '	a'				
 bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit⁽¹⁾ 1 = Output pin polarity is active-low 	bit 5		Px Output Pin		MxC and OCM	xE Polarity Co	ntrol hit	
 0 = Output pin polarity is active-high bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit⁽¹⁾ 1 = Output pin polarity is active-low 	bit o	1 = Output pi	n polarity is act	tive-low		xe, i olanty oc		
bit 4 POLBDF: CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit ⁽¹⁾ 1 = Output pin polarity is active-low		0 = Output pi	n polarity is act	tive-high				
1 = Output pin polarity is active-low	bit 4	POLBDF: CC	Px Output Pine	s, OCMxB, OCI	MxD and OCM	xF, Polarity Co	ntrol bit ⁽¹⁾	
		1 = Output pi	n polarity is ac	tive-low				
0 = Output pin polarity is active-high			n polarity is act	tive-high				
bit 3-2 PSSACE<1:0>: PWMx Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits	bit 3-2	PSSACE<1:0	>: PWMx Outp	out Pins, OCMx	A, OCMXC and	d OCMxE, Shu	tdown State Co	ontrol bits
11 = Pins are driven active when a shutdown event occurs $10 = Pins are driven inactive when a shutdown event occurs$		11 = Pins are 10 = Pins are	driven active v	when a shutdow	own event occurs	s Irs		
0x = Pins are tri-stated when a shutdown event occurs		0x = Pins are	tri-stated wher	n a shutdown e	vent occurs			
bit 1-0 PSSBDF<1:0>: PWMx Output Pins, OCMxB, OCMxD, and OCMxF, Shutdown State Control bits ⁽¹⁾	bit 1-0	PSSBDF<1:0	>: PWMx Outp	out Pins, OCMx	B, OCMxD, an	d OCMxF, Shu	tdown State Co	ontrol bits ⁽¹⁾
11 = Pins are driven active when a shutdown event occurs		11 = Pins are	driven active v	when a shutdow	n event occurs	5		
10 = Pins are driven inactive when a shutdown event occurs 0x = Pins are in a high-impedance state when a shutdown event occurs		10 = Pins are	driven inactive	when a shutdo	own event occu	Jrs Nevent occurs		

REGISTER 22-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

Note 1: These bits are implemented in the MCCP9 module only.

TABLE 33-36: ADC MODULE SPECIFICATIONS	
--	--

Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C < TA \le +125^{\circ}C$ for Extended								
Param No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions	
			Analog	j Input				
AD12 VINH-VINL Full-Scale Input Span AVss — AVDD V								
AD14	Vin	Absolute Input Voltage	AVss – 0.3	_	AVDD + 0.3	V		
AD17	Rin	Recommended Impedance of Analog Voltage Source	_	100	_	Ω	For minimum sampling time (Note 1)	
AD66	Vbg	Internal Voltage Reference Source	_	1.2		\vee		
			ADC Ac	curacy				
AD20c	Nr	Resolution	1	2 data bits		bits		
AD21c	INL	Integral Nonlinearity	> -11.3	—	< 11.3	LSb	AVss = 0V, AVDD = 3.3V	
AD22c	DNL	Differential Nonlinearity	> -1.5	_	< 11.5	LSb	AVss = 0V, AVDD = 3.3V	
AD23c	Gerr	Gain Error	> -12		< 12	LSb	AVss = 0V, AVDD = 3.3V	
AD24c	EOFF	Offset Error	> -7.5		< 7.5	LSb	AVss = 0V, AVDD = 3.3V	
Dynamic Performance								
AD31b	SINAD	Signal-to-Noise and Distortion	56	_	70	dB	(Notes 2, 3)	
AD34b	ENOB	Effective Number of Bits	9.0	_	11.4	bits	(Notes 2, 3)	
AD50	TAD	ADC Clock Period	14.3	_	—	ns		
AD51	Ftp	Throughput Rate	_		3.5	Msps	Dedicated Cores 0 and 1	
			_	—	3.5	Msps	Shared core	

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

34.0 PACKAGING INFORMATION

34.1 Package Marking Information

28-Lead SSOP (5.30 mm)

28-Lead UQFN (6x6 mm)

36-Lead UQFN (5x5 mm)

48-Lead TQFP (7x7 mm)

Example

Example

Example

Example

CK256MP 5051710 017

Legend	d: XXX Y YY WW NNN	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code				
Note:	te: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.					

34.1 Package Marking Information (Continued)

48-Lead UQFN (6x6 mm)

Example

PIC33CK 256MP505 1710017

64-Lead TQFP (10x10x1 mm)

64-Lead QFN (9x9x0.9 mm)

80-Lead TQFP (12x12x1 mm)

Example

Example

Example

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Ν	IILLIMETER	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

Resets	91
Brown-out Reset (BOR)	91
Configuration Mismatch Reset (CM)	91
Illegal Condition Reset (IOPUWR)	91
Illegal Opcode	91
Security	91
Uninitialized W Register	91
Master Clear (MCLR) Pin Reset	91
Power-on Reset (POR)	91
RESET Instruction (SWR)	91
Resources	92
Trap Conflict Reset (TRAPR)	91
Watchdog Timer Time-out Reset (WDTO)	91
Revision History	605

S

-	
SENTx Protocol Data Frames	416
Serial Peripheral Interface (SPI)	373
Serial Peripheral Interface. See SPI.	
SFR Blocks	
000h	50
100h	51
200h	52
300h	53
400h	54
500h	55
600h	56
800h	57
900h	58
A00h	59
B00h	60
C00h	61
D00h	62
E00h	63
F00h	64
Single-Edge Nibble Transmission (SENT)	415
Control Registers	419
Receive Mode	418
Configuration	418
Transmit Mode	417
Configuration	417
Single-Edge Nibble Transmission for	
Automotive Applications	415
Single-Edge Nibble Transmission. See SENT.	
Software Simulator	
MPLAB X SIM	543
Special Features of the CPU	505
SPI	
Control Registers	378

Т

Thermal Operating Conditions 54 Thermal Packaging Characteristics 54 Third-Party Development Tools 54 Timer1 42	16 16 14 25
Control Register	26
Timing Diagrams	
BOR and Master Clear Reset Characteristics 56	31
Clock/Instruction Cycle 18	35
External Clock55	58
High-Speed PWMx Fault Characteristics 56	33
High-Speed PWMx Module Characteristics 56	33
I/O Characteristics	31
I2Cx Bus Data (Master Mode) 57	/2
I2Cx Bus Data (Slave Mode) 57	74
I2Cx Bus Start/Stop Bits (Master Mode) 57	72
I2Cx Bus Start/Stop Bits (Slave Mode)57	74
QEI Interface Signals	31
SPIx Master Mode (Full-Duplex, CKE = 0,	
CKP = x, SMP = 1)	37
SPIx Master Mode (Full-Duplex, CKE = 1,	
CKP = x, SMP = 1)	36
SPIx Master Mode (Half-Duplex,	
Transmit Only, CKE = 0)56	34
SPIx Master Mode (Half-Duplex,	
Transmit Only, CKE = 1)	35
SPIx Slave Mode (Full-Duplex, CKE = 0,	
CKP = x, SMP = 0)	38
SPIx Slave Mode (Full-Duplex, CKE = 1,	
CKP = x, SMP = 0)	70
UARTx I/O Characteristics	76

U

UART	
Architectural Overview	352
Character Frame	353
Control Registers	354
Data Buffers	353
Protocol Extensions	353
Unique Device Identifier (UDID)	43
Unique Device Identifier. See UDID.	
Universal Asynchronous Receiver	
Transmitter (UART)	351
Universal Asynchronous Receiver Transmitter	r. See UART.
User OTP Memory	524
V	

olto

Voltage Regulator (On-Chip)	524
W	
Watchdog Timer (WDT)	505
WWW Address	615

WWW, On-Line Support 15