Microchip Technology - DSPIC33CK256MP202T-I/2N Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

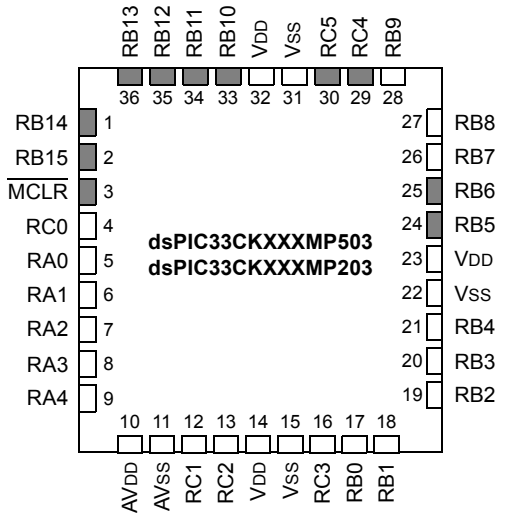
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck256mp202t-i-2n

Pin Diagrams (Continued)

36-Pin UQFN



Note: Shaded pins are up to 5 VDC tolerant.

TABLE 5: 36-PIN UQFN

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/RB14	19	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	**RP47**/PWM1L/RB15	20	PGD2/OA2IN-/AN8/**RP35**/RB3
3	MCLR	21	PGC2/OA2IN+/**RP36**/RB4
4	AN12/ANN0/**RP48**/RC0	22	VSS
5	OA1OUT/AN0/CMP1A/IBIAS0/RA0	23	VDD
6	OA1IN-/ANA1/RA1	24	PGD3/**RP37**/PWM6L/SDA2/RB5
7	OA1IN+/AN9/RA2	25	PGC3/**RP38**/PWM6H/SCL2/RB6
8	DACOUT1/AN3/CMP1C/RA3	26	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
9	OA3OUT/AN4/CMP3B/IBIAS3/RA4	27	PGD1/AN10/**RP40**/SCL1/RB8
10	AVDD	28	PGC1/AN11/**RP41**/SDA1/RB9
11	AVSS	29	**RP52**/PWM5H/ASDA2/RC4
12	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	30	**RP53**/PWM5L/ASCL2/RC5
13	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/RC2	31	VSS
14	VDD	32	VDD
15	VSS	33	TMS/**RP42**/PWM3H/RB10
16	AN15/CMP2A/IBIAS2/**RP51**/RC3	34	TCK/**RP43**/PWM3L/RB11
17	OSCI/CLKI/AN5/**RP32**/RB0	35	TDI/**RP44**/PWM2H/RB12
18	OSCO/CLKO/AN6/**RP33**/RB1	36	**RP45**/PWM2L/RB13

Note: **RPn** represents remappable peripheral functions.

TABLE 8: 80-PIN TQFP

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/PMD5/RB14	41	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	AN20/RE0	42	RE8
3	**RP47**/PWM1L/PMD6/RB15	43	PGD2/OA2IN-/AN8/**RP35**/RB3
4	AN21/RE1	44	RE9
5	**RP60**/PWM8H/PMD7/RC12	45	PGC2/OA2IN+/**RP36**/RB4
6	**RP61**/PWM8L/PMA5/RC13	46	**RP56**/ASDA1/SCK2/RC8
7	**RP62**/PWM6H/PMA4/RC14	47	**RP57**/ASCL1/SDI2/RC9
8	**RP63**/PWM6L/PMA3/RC15	48	**RP73**/PCI20/RD9
9	$\overline{\text{MCLR}}$	49	**RP72**/SDO2/PCI19/RD8
10	**RP79**/PCI22/PMA2/RD15	50	VSS
11	VSS	51	VDD
12	VDD	52	**RP71**/PMD15/RD7
13	**RP78**/PCI21/RD14	53	**RP70**/PMD14/RD6
14	ANN2/**RP77**/RD13	54	**RP69**/PMA15/PMCS2/RD5
15	AN12/ANN0/**RP48**/RC0	55	PGD3/**RP37**/SDA2/PMA14/PMCS1/PSCS/RB5
16	OA1OUT/AN0/CMP1A/IBIAS0/RA0	56	PGC3/**RP38**/SCL2/RB6
17	AN22/RE2	57	RE10
18	OA1IN-/ANA1/RA1	58	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
19	AN23/RE3	59	RE11
20	OA1IN+/AN9/PMA6/RA2	60	PGD1/AN10/**RP40**/SCL1/RB8
21	DACOUT1/AN3/CMP1C/RA3	61	PGC1/AN11/**RP41**/SDA1/RB9
22	RE4	62	RE12
23	OA3OUT/AN4/CMP3B/IBIAS3/RA4	63	**RP52**/PWM5H/ASDA2/RC4
24	RE5	64	RE13
25	AVDD	65	**RP53**/PWM5L/ASCL2/PMWR/PMENB/PSWR/RC5
26	AVss	66	**RP58**/PWM7H/PMRD/$\overline{\text{PMWR}}$/PSRD/RC10
27	**RP76**/RD12	67	**RP59**/PWM7L/RC11
28	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/PMA7/RC1	68	**RP68**/ASDA3/RD4
29	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/PMD13/PMA13/RC2	69	**RP67**/ASCL3/RD3
30	AN17/ANN1/IBIAS1/**RP54**/PMD12/PMA12/RC6	70	VSS
31	VDD	71	VDD
32	VSS	72	**RP66**/RD2
33	AN15/CMP2A/IBIAS2/**RP51**/PMD11/PMA11/RC3	73	**RP65**/PWM4H/RD1
34	OSCI/CLKI/AN5/**RP32**/PMD10/PMA10/RB0	74	**RP64**/PWM4L/PMD0/RD0
35	OSCO/CLKO/AN6/**RP33**/PMA1/PMALH/PSA1/RB1	75	TMS/**RP42**/PWM3H/PMD1/RB10
36	AN19/CMP2C/**RP75**/PMA0/PMALL/PSA0/RD11	76	TCK/**RP43**/PWM3L/PMD2/RB11
37	RE6	77	RE14
38	AN18/CMP3C/ISRC3/**RP74**/PMD9/PMA9/RD10	78	TDI/**RP44**/PWM2H/PMD3/RB12
39	RE7	79	RE15
40	AN16/ISRC2/**RP55**/PMD8/PMA8/RC7	80	**RP45**/PWM2L/PMD4/RB13

Note: **RPn** represents remappable peripheral functions.

Table of Contents

2.4 ICSP Pins

The PGCx and PGDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGCx and PGDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGCx/PGDx pins) programmed into the device matches the physical connections for the ICSP to PICkit™ 3, MPLAB® ICD 3 or MPLAB REAL ICE™ emulator.

For more information on MPLAB ICD 2, MPLAB ICD 3 and REAL ICE emulator connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3 In-Circuit Debugger"* (poster) (DS51765)
- *"Development Tools Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.5 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator (POSC) and a low-frequency Secondary Oscillator (SOSC). For details, see **Section 9.2 "Primary Oscillator (POSC)"**.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

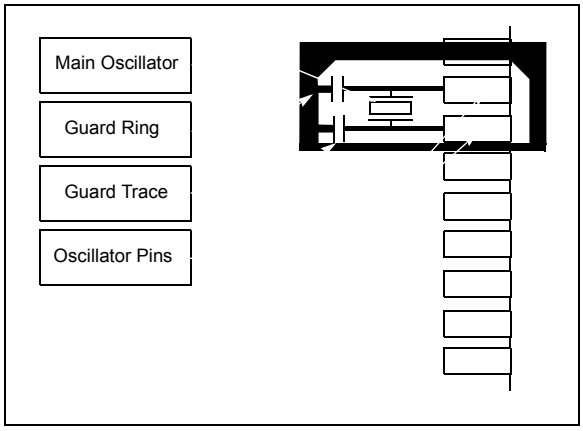


TABLE 4-6: SFR BLOCK 400h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
High-Speed PWM (Continued)			PG6FPCIH	448	0000-00000000000	PG7DC	492	0000000000000000
PG4CAP	400	0000000000000000	PG6CLPCIL	44A	0000000000000000	PG7DCA	494	--------00000000
PG5CONL	402	-----0000--00000	PG6CLPCIH	44C	0000-00000000000	PG7PER	496	0000000000000000
PG5CONH	404	000-000000--0000	PG6FFPCIL	44E	0000000000000000	PG7TRIGA	498	0000000000000000
PG5STAT	406	0000000000000000	PG6FFPCIH	450	0000-00000000000	PG7TRIGB	49A	0000000000000000
PG5IOCONL	408	0000000000000000	PG6SPCIL	452	0000000000000000	PG7TRIGC	49C	0000000000000000
PG5IOCONH	40A	0000---0--000000	PG6SPCIH	454	0000-00000000000	PG7DTL	49E	--00000000000000
PG5EVTL	40C	00000000---00000	PG6LEBL	456	0000000000000000	PG7DTH	4A0	--00000000000000
PG5EVTH	40E	0000--0000000000	PG6LEBH	458	-----000----0000	PG7CAP	4A2	0000000000000000
PG5FPCIL	410	0000000000000000	PG6PHASE	45A	0000000000000000	PG8CONL	4A4	-----0000--00000
PG5FPCIH	412	0000-00000000000	PG6DC	45C	0000000000000000	PG8CONH	4A6	000-000000--0000
PG5CLPCIL	414	0000000000000000	PG6DCA	45E	--------00000000	PG8STAT	4A8	0000000000000000
PG5CLPCIH	416	0000-00000000000	PG6PER	460	0000000000000000	PG8IOCONL	4AA	0000000000000000
PG5FFPCIL	418	0000000000000000	PG6TRIGA	462	0000000000000000	PG8IOCONH	4AC	0000---0--000000
PG5FFPCIH	41A	0000-00000000000	PG6TRIGB	464	0000000000000000	PG8EVTL	4AE	00000000---00000
PG5SPCIL	41C	0000000000000000	PG6TRIGC	466	0000000000000000	PG8EVTH	4B0	0000--0000000000
PG5SPCIH	41E	0000-00000000000	PG6DTL	468	--00000000000000	PG8FPCIL	4B2	0000000000000000
PG5LEBL	420	0000000000000000	PG6DTH	46A	--00000000000000	PG8FPCIH	4B4	0000-00000000000
PG5LEBH	422	-----000----0000	PG6CAP	46C	0000000000000000	PG8CLPCIL	4B6	0000000000000000
PG5PHASE	424	0000000000000000	PG7CONL	46E	-----0000--00000	PG8CLPCIH	4B8	0000-00000000000
PG5DC	426	0000000000000000	PG7CONH	470	000-000000--0000	PG8FFPCIL	4BA	0000000000000000
PG5DCA	428	--------00000000	PG7STAT	472	0000000000000000	PG8FFPCIH	4BC	0000-00000000000
PG5PER	42A	0000000000000000	PG7IOCONL	474	0000000000000000	PG8SPCIL	4BE	0000000000000000
PG5TRIGA	42C	0000000000000000	PG7IOCONH	476	0000---0--000000	PG8SPCIH	4C0	0000-00000000000
PG5TRIGB	42E	0000000000000000	PG7EVTL	478	00000000---00000	PG8LEBL	4C2	0000000000000000
PG5TRIGC	430	0000000000000000	PG7EVTH	47A	0000--0000000000	PG8LEBH	4C4	-----000----0000
PG5DTL	432	--00000000000000	PG7FPCIL	47C	0000000000000000	PG8PHASE	4C6	0000000000000000
PG5DTH	434	--00000000000000	PG7FPCIH	47E	0000-00000000000	PG8DC	4C8	0000000000000000
PG5CAP	436	0000000000000000	PG7CLPCIL	480	0000000000000000	PG8DCA	4CA	--------00000000
PG6CONL	438	-----0000--00000	PG7CLPCIH	482	0000-00000000000	PG8PER	4CC	0000000000000000
PG6CONH	43A	000-000000--0000	PG7FFPCIL	484	0000000000000000	PG8TRIGA	4CE	0000000000000000
PG6STAT	43C	0000000000000000	PG7FFPCIH	486	0000-00000000000	PG8TRIGB	4D0	0000000000000000
PG6IOCONL	43E	0000000000000000	PG7SPCIL	488	0000000000000000	PG8TRIGC	4D2	0000000000000000
PG6IOCONH	440	0000---0--000000	PG7SPCIH	48A	0000-00000000000	PG8DTL	4D4	--00000000000000
PG6EVTL	442	00000000---00000	PG7LEBL	48C	0000000000000000	PG8DTH	4D6	--00000000000000
PG6EVTH	444	0000--0000000000	PG7LEBH	48E	-----000----0000	PG8CAP	4D8	0000000000000000
PG6FPCIL	446	0000000000000000	PG7PHASE	490	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address values are in hexadecimal. Reset values are in binary.

TABLE 4-7: SFR BLOCK 500h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
CAN			C1TSCONL	5D4	------0000000000	C1RXOVIFH	5EA	0000000000000000
C1CONL	5C0	--00011101100000	C1TSCONH	5D6	------------000	C1TXATIFL	5EC	0000000000000000
C1CONH	5C2	0000010010011000	C1VECL	5D8	---00000-1000000	C1TXATIFH	5EE	0000000000000000
C1NBTCFGL	5C4	00001111-0001111	C1VECH	5DA	11000000-1000000	C1TXREQL	5F0	0000000000000000
C1NBTCFGH	5C6	0000000000111110	C1INTL	5DC	000000-----00000	C1TXREQH	5F2	0000000000000000
C1DBTCFGL	5C8	----0011----0011	C1INTH	5DE	000000-----00000	C1TRECL	5F4	0000000000000000
C1DBTCFGH	5CA	00000000---01110	C1RXIFL	5E0	0000000000000000	C1TRECH	5F6	----------100000
C1TDCL	5CC	00010000--000000	C1RXIFH	5E2	0000000000000000	C1BDIAG0L	5F8	0000000000000000
C1TDCH	5CE	------00------10	C1TXIFL	5E4	000000000000000-	C1BDIAG0H	5FA	0000000000000000
C1TBCL	5D0	0000000000000000	C1TXIFH	5E6	0000000000000000	C1BDIAG1L	5FC	0000000000000000
C1TBCH	5D2	0000000000000000	C1RXOVIFL	5E8	000000000000000-	C1BDIAG1H	5FE	00000-000-000000

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address values are in hexadecimal. Reset values are in binary.

TABLE 8-5: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name(1)	Function Name	Register	Register Bits
External Interrupt 1	INT1	RPINR0	INT1R<7:0>
External Interrupt 2	INT2	RPINR1	INT2R<7:0>
External Interrupt 3	INT3	RPINR1	INT3R<7:0>
Timer1 External Clock	T1CK	RPINR2	T1CK<7:0>
SCCP Timer1	TCKI1	RPINR3	TCKI1R<7:0>
SCCP Capture 1	ICM1	RPINR3	ICM1R<7:0>
SCCP Timer2	TCKI2	RPINR4	TCKI2R<7:0>
SCCP Capture 2	ICM2	RPINR4	ICM2R<7:0>
SCCP Timer3	TCKI3	RPINR5	TCKI3R<7:0>
SCCP Capture 3	ICM3	RPINR5	ICM3R<7:0>
SCCP Timer4	TCKI4	RPINR6	TCKI4R<7:0>
SCCP Capture 4	ICM4	RPINR6	ICM4R<7:0>
SCCP Timer5	TCKI5	RPINR7	TCKI5R<7:0>
SCCP Capture 5	ICM5	RPINR7	ICM5R<7:0>
SCCP Timer6	TCKI6	RPINR8	TCKI6R<7:0>
SCCP Capture 6	ICM6	RPINR8	ICM6R<7:0>
SCCP Timer7	TCKI7	RPINR9	TCKI7R<7:0>
SCCP Capture 7	ICM7	RPINR9	ICM7R<7:0>
SCCP Timer8	TCKI8	RPINR10	TCKI8R<7:0>
SCCP Capture 8	ICM8	RPINR10	ICM8R<7:0>
xCCP Fault A	OCFA	RPINR11	OCFAR<7:0>
xCCP Fault B	OCFB	RPINR11	OCFBR<7:0>
PWM PCI 8	PCI8	RPINR12	PCI8R<7:0>
PWM PCI 9	PCI9	RPINR12	PCI9R<7:0>
PWM PCI 10	PCI10	RPINR13	PCI10R<7:0>
PWM PCI 11	PCI11	RPINR13	PCI11R<7:0>
QEI1 Input A	QEIA1	RPINR14	QEIA1R<7:0>
QEI1 Input B	QEIB1	RPINR14	QEIB1R<7:0>
QEI1 Index 1 Input	QEINDX1	RPINR15	QEINDX1R<7:0>
QEI1 Home 1 Input	QEIHOM1	RPINR15	QEIHOM1R<7:0>
QEI2 Input A	QEIA2	RPINR16	QEIA2R<7:0>
QEI2 Input B	QEIB2	RPINR16	QEIB2R<7:0>
QEI2 Index 1 Input	QEINDX2	RPINR17	QEINDX2R<7:0>
QEI2 Home 1 Input	QEIHOM2	RPINR17	QEIHOM2R<7:0>
UART1 Receive	U1RX	RPINR18	U1RXR<7:0>
UART1 Data-Set-Ready	$\overline{\text{U1DSR}}$	RPINR18	U1DSRR<7:0>
UART2 Receive	U2RX	RPINR19	U2RXR<7:0>
UART2 Data-Set-Ready	$\overline{\text{U2DSR}}$	RPINR19	U2DSRR<7:0>
SPI1 Data Input	SDI1	RPINR20	SDI1R<7:0>
SPI1 Clock Input	SCK1IN	RPINR20	SCK1R<7:0>
SPI1 Slave Select	$\overline{\text{SS1}}$	RPINR21	SS1R<7:0>
Reference Clock Input	REFOI	RPINR21	REFOIR<7:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<7:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

TABLE 8-10: PORTC REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSELC	—	—	—	—	—	—	—	—	ANSELC<7:6>		—	—	ANSELC<3:0>			
TRISC	TRISC<15:0>															
PORTC	RC<15:0>															
LATC	LATC<15:0>															
ODCC	ODCC<15:0>															
CNPUC	CNPUC<15:0>															
CNPDC	CNPDC<15:0>															
CNCONC	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—
CNEN0C	CNEN0C<15:0>															
CNSTATC	CNSTATC<15:0>															
CNEN1C	CNEN1C<15:0>															
CNFC	CNFC<15:0>															

TABLE 8-11: PORTD REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSELD	—	—	ANSELD<13>	—	ANSELD<11:10>		—	—	—	—	—	—	—	—	—	—
TRISD	TRISD<15:0>															
PORTD	RD<15:0>															
LATD	LATD<15:0>															
ODCD	ODCD<15:0>															
CNPUD	CNPUD<15:0>															
CNPDD	CNPDD<15:0>															
CNCOND	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—
CNEN0D	CNEN0D<15:0>															
CNSTATD	CNSTATD<15:0>															
CNEN1D	CNEN1D<15:0>															
CNFD	CNFD<15:0>															

REGISTER 8-23: RPINR9: PERIPHERAL PIN SELECT INPUT REGISTER 9

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM7R7	ICM7R6	ICM7R5	ICM7R4	ICM7R3	ICM7R2	ICM7R1	ICM7R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI7R7	TCKI7R6	TCKI7R5	TCKI7R4	TCKI7R3	TCKI7R2	TCKI7R1	TCKI7R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM7R<7:0>:** Assign SCCP Capture 7 (ICM7) Input to the Corresponding RPn Pin bits
See Table 8-4.

bit 7-0 **TCKI7R<7:0>:** Assign SCCP Timer7 (TCKI7) Input to the Corresponding RPn Pin bits
See Table 8-4.

REGISTER 8-24: RPINR10: PERIPHERAL PIN SELECT INPUT REGISTER 10

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICM8R7	ICM8R6	ICM8R5	ICM8R4	ICM8R3	ICM8R2	ICM8R1	ICM8R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TCKI8R7	TCKI8R6	TCKI8R5	TCKI8R4	TCKI8R3	TCKI8R2	TCKI8R1	TCKI8R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ICM8R<7:0>:** Assign SCCP Capture 8 (ICM8) Input to the Corresponding RPn Pin bits
See Table 8-4.

bit 7-0 **TCKI8R<7:0>:** Assign SCCP Timer8 (TCKI8) Input to the Corresponding RPn Pin bits
See Table 8-4.

REGISTER 11-3: C1NBTCFGH: CAN NOMINAL BIT TIME CONFIGURATION REGISTER HIGH(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BRP<7:0>							
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
TSEG1<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **BRP<7:0>:** Baud Rate Prescaler bits
1111 1111 = TQ = 256/FSYS
...
0000 0000 = TQ = 1/FSYS

bit 7-0 **TSEG1<7:0>:** Time Segment 1 bits (Propagation Segment + Phase Segment 1)
1111 1111 = Length is 256 x TQ
...
0000 0000 = Length is 1 x TQ

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 11-4: C1NBTCFGL: CAN NOMINAL BIT TIME CONFIGURATION REGISTER LOW(1)

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	TSEG2<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	SJW<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **TSEG2<6:0>:** Time Segment 2 bits (Phase Segment 2)
111 1111 = Length is 128 x TQ
...
000 0000 = Length is 1 x TQ

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SJW<6:0>:** Synchronization Jump Width bits
111 1111 = Length is 128 x TQ
...
000 0000 = Length is 1 x TQ

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 12-13: PGxCONH: PWM GENERATOR x CONTROL REGISTER HIGH (CONTINUED)

bit 6 **TRGMOD:** PWM Generator Trigger Mode Selection bit
1 = PWM Generator operates in Retriggerable mode
0 = PWM Generator operates in Single Trigger mode

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **SOCS<3:0>:** Start-of-Cycle Selection bits(1,2,3)
1111 = TRIG bit or PCI Sync function only (no hardware trigger source is selected)
1110-0101 = Reserved
0100 = Trigger output selected by PG4 or PG8 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0011 = Trigger output selected by PG3 or PG7 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0010 = Trigger output selected by PG2 or PG6 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0001 = Trigger output selected by PG1 or PG5 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0000 = Local EOC – PWM Generator is self-triggered

Note 1: The PCI selected Sync signal is always available to be OR'd with the selected SOC signal per the SOCS<3:0> bits if the PCI Sync function is enabled.

2: The source selected by the SOCS<3:0> bits MUST operate from the same clock source as the local PWM Generator. If not, the source must be routed through the PCI Sync logic so the trigger signal may be synchronized to the PWM Generator clock domain.

3: PWM Generators are grouped into groups of four: PG1-PG4 and PG5-PG8, if available. Any generator within a group of four may be used to trigger another generator within the same group.

REGISTER 14-6: DACxDATH: DACx DATA HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACDAT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACDAT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 15-0 **DACDAT<15:0>:** DACx Data bits
This register specifies the high DACx data value. Valid values are from 0x0205 to 0x3890.

REGISTER 14-7: DACxDATL: DACx DATA LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACLOW<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACLOW<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 15-0 **DACLOW<15:0>:** DACx Low Data bits
In Hysteretic mode, Slope Generator mode and Triangle mode, this register specifies the low data value and/or limit for the DACx module. Valid values are from 0x0205 to 0x3890.

REGISTER 15-15: INDXxCNTL: INDEX x COUNTER REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INDXCNT<15:0>:** Low Word Used to Form 32-Bit Index x Counter Register (INDXxCNT) bits

REGISTER 15-16: INDXxCNTH: INDEX x COUNTER REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXCNT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INDXCNT<31:16>:** High Word Used to Form 32-Bit Index x Counter Register (INDXxCNT) bits

REGISTER 18-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 8 **SMEN:** SMBus Input Levels Enable bit
1 = Enables input logic so thresholds are compliant with the SMBus specification
0 = Disables SMBus-specific inputs

bit 7 **GCEN:** General Call Enable bit (I^2C Slave mode only)
1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
0 = General call address is disabled.

bit 6 **STREN:** SCLx Clock Stretch Enable bit
In I^2C Slave mode only; used in conjunction with the SCLREL bit.
1 = Enables clock stretching
0 = Disables clock stretching

bit 5 **ACKDT:** Acknowledge Data bit
In I^2C Master mode during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Slave mode when AHEN = 1 or DHEN = 1. The value that the Slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
1 = NACK is sent
0 = ACK is sent

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
In I^2C Master mode only; applicable during Master Receive mode.
1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
0 = Acknowledge sequence is Idle

bit 3 **RCEN:** Receive Enable bit (I^2C Master mode only)
1 = Enables Receive mode for I^2C; automatically cleared by hardware at end of 8-bit receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (I^2C Master mode only)
1 = Initiates Stop condition on SDAx and SCLx pins
0 = Stop condition is Idle

bit 1 **RSEN:** Restart Condition Enable bit (I^2C Master mode only)
1 = Initiates Restart condition on SDAx and SCLx pins
0 = Restart condition is Idle

bit 0 **SEN:** Start Condition Enable bit (I^2C Master mode only)
1 = Initiates Start condition on SDAx and SCLx pins
0 = Start condition is Idle

Note 1: Automatically cleared to '0' at the beginning of Slave transmission; automatically cleared to '0' at the end of Slave reception.
2: Automatically cleared to '0' at the beginning of Slave transmission.

REGISTER 22-2: CCPxCON1H: CCPx CONTROL 1 HIGH REGISTERS

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
OPSSRC(1)	RTRGEN(2)	—	—	OPS3(3)	OPS2(3)	OPS1(3)	OPS0(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGEN	ONESHOT	ALTSYNC	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OPSSRC:** Output Postscaler Source Select bit(1)
1 = Output postscaler scales module trigger output events
0 = Output postscaler scales time base interrupt events

bit 14 **RTRGEN:** Retrigger Enable bit(2)
1 = Time base can be retriggered when TRIGEN bit = 1
0 = Time base may not be retriggered when TRIGEN bit = 1

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **OPS3<3:0>:** CCPx Interrupt Output Postscale Select bits(3)
1111 = Interrupt every 16th time base period match
1110 = Interrupt every 15th time base period match
...
0100 = Interrupt every 5th time base period match
0011 = Interrupt every 4th time base period match or 4th input capture event
0010 = Interrupt every 3rd time base period match or 3rd input capture event
0001 = Interrupt every 2nd time base period match or 2nd input capture event
0000 = Interrupt after each time base period match or input capture event

bit 7 **TRIGEN:** CCPx Trigger Enable bit
1 = Trigger operation of time base is enabled
0 = Trigger operation of time base is disabled

bit 6 **ONESHOT:** One-Shot Trigger Mode Enable bit
1 = One-Shot Trigger mode is enabled; trigger duration is set by OSCNT<2:0>
0 = One-Shot Trigger mode is disabled

bit 5 **ALTSYNC:** CCPx Clock Select bits
1 = An alternate signal is used as the module synchronization output signal
0 = The module synchronization output signal is the Time Base Reset/rollover event

bit 4-0 **SYNC<4:0>:** CCPx Synchronization Source Select bits
See Table 22-5 for the definition of inputs.

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Output postscale settings, from 1:5 to 1:16 (0100-1111), will result in a FIFO buffer overflow for Input Capture modes.

REGISTER 22-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2(1)	OUTM1(1)	OUTM0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	POLBDF(1)	PSSACE1	PSSACE0	PSSBDF1(1)	PSSBDF0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** CCPx Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT<2:0>:** One-Shot Event Count bits
111 = Extends one-shot event by 7 time base periods (8 time base periods total)
110 = Extends one-shot event by 6 time base periods (7 time base periods total)
101 = Extends one-shot event by 5 time base periods (6 time base periods total)
100 = Extends one-shot event by 4 time base periods (5 time base periods total)
011 = Extends one-shot event by 3 time base periods (4 time base periods total)
010 = Extends one-shot event by 2 time base periods (3 time base periods total)
001 = Extends one-shot event by 1 time base period (2 time base periods total)
000 = Does not extend one-shot Trigger event

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OUTM<2:0>:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **POLACE:** CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 4 **POLBDF:** CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit(1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 3-2 **PSSACE<1:0>:** PWMx Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are tri-stated when a shutdown event occurs

bit 1-0 **PSSBDF<1:0>:** PWMx Output Pins, OCMxB, OCMxD, and OCMxF, Shutdown State Control bits(1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in the MCCP9 module only.

REGISTER 24-2: PTGCON: PTG CONTROL/STATUS HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **PTGCLK<2:0>:** PTG Module Clock Source Selection bits
111 = CLC1
110 = PLL VCO DIV 4 output
101 = PTG module clock source will be SCCP7
100 = PTG module clock source will be SCCP8
011 = Input from Timer1 Clock pin, T1CK
010 = PTG module clock source will be ADC clock
001 = PTG module clock source will be FOSC
000 = PTG module clock source will be FOSC/2 (FP)

bit 12-8 **PTGDIV<4:0>:** PTG Module Clock Prescaler (Divider) bits
11111 = Divide-by-32
11110 = Divide-by-31
...
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width (in PTG clock cycles) bits
1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
...
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PTGWDT<2:0>:** PTG Watchdog Timer Time-out Selection bits
111 = Watchdog Timer will time out after 512 PTG clocks
110 = Watchdog Timer will time out after 256 PTG clocks
101 = Watchdog Timer will time out after 128 PTG clocks
100 = Watchdog Timer will time out after 64 PTG clocks
011 = Watchdog Timer will time out after 32 PTG clocks
010 = Watchdog Timer will time out after 16 PTG clocks
001 = Watchdog Timer will time out after 8 PTG clocks
000 = Watchdog Timer is disabled

TABLE 33-11: APLL DELTA CURRENT

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended						
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions(1)**		
DC110	5.93	6.6	mA	-40°C	3.3V	AFPLLO = 500 MHz (AVCO = 1000 MHz, PLLFBD = 125, APLLDIV1 = 2)
	5.95	7	mA	+25°C		
	6.15	7.6	mA	+85°C		
	7.15	9	mA	+125°C		
DC111	2.72	3.3	mA	-40°C	3.3V	AFPLLO = 400 MHz (AVCO = 400 MHz, PLLFBD = 50, APLLDIV1 = 1)
	2.74	3.7	mA	+25°C		
	2.92	4.3	mA	+85°C		
	3.87	5.6	mA	+125°C		
DC112	1.39	2.7	mA	-40°C	3.3V	AFPLLO = 200 MHz (AVCO = 400 MHz, PLLFBD = 50, APLLDIV1 = 2)
	1.49	2.7	mA	+25°C		
	1.65	3	mA	+85°C		
	2.6	4.4	mA	+125°C		
DC113	0.79	1.1	mA	-40°C	3.3V	AFPLLO = 100 MHz (AVCO = 400 MHz, PLLFBD = 50, APLLDIV1 = 4)
	0.84	1.4	mA	+25°C		
	0.96	2.3	mA	+85°C		
	1.93	3.6	mA	+125°C		

Note 1: The APLL current will be the same if more than 1 PWM or DAC is run to the APLL clock. All parameters are characterized but not tested during manufacturing.

TABLE 33-12: ADC DELTA CURRENT(1)

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended						
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**		
DC120	3.61	4	mA	-40°C	3.3V	TAD = 14.3 ns (3.5 Msps conversion rate)
	3.68	4.1	mA	+25°C		
	3.69	4.2	mA	+85°C		
	3.89	4.6	mA	+125°C		

Note 1: Shared core continuous conversion. TAD = 14.3 nS (3.5 Msps conversion rate). Listed delta currents are for only one ADC core. All parameters are characterized but not tested during manufacturing.

TABLE 33-32: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 0) TIMING REQUIREMENTS

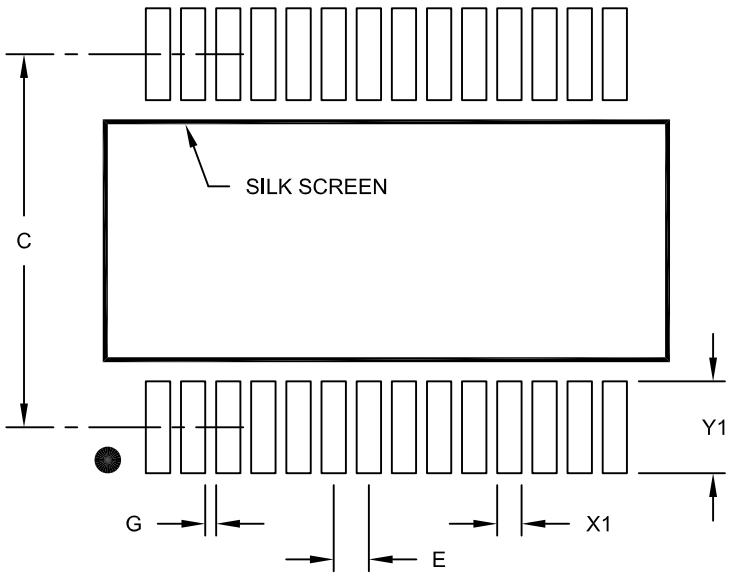
Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCKx Input Frequency	—	—	15	MHz	Using PPS pins
			—	—	40	MHz	SPIx dedicated pins
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	Using PPS pins
			20	—	—	ns	SPIx dedicated pins
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			10	—	—	ns	SPIx dedicated pins
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			15	—	—	ns	SPIx dedicated pins
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	8	—	50	ns	
SP52	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge	1.5 TCY + 40	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid After $\overline{SSx}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

