Microchip Technology - DSPIC33CK256MP505T-I/PT Datasheet

What is "Embedded - Microcontrollers"?

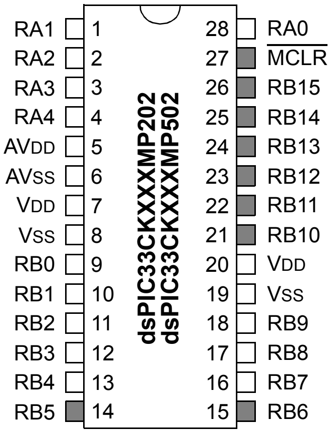
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	39
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck256mp505t-i-pt

Pin Diagrams

28-Pin SSOP



Note: Shaded pins are up to 5 VDC tolerant.

TABLE 3: 28-PIN SSOP

Pin #	Function	Pin #	Function
1	OA1IN-/ANA1/RA1	15	PGC3/**RP38**/SCL2/RB6
2	OA1IN+/AN9/RA2	16	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
3	DACOUT1/AN3/CMP1C/RA3	17	PGD1/AN10/**RP40**/SCL1/RB8
4	AN4/CMP3B/IBIAS3/RA4	18	PGC1/AN11/**RP41**/SDA1/RB9
5	AVDD	19	VSS
6	AVSS	20	VDD
7	VDD	21	TMS/**RP42**/PWM3H/RB10
8	VSS	22	TCK/**RP43**/PWM3L/RB11
9	OSCI/CLKI/AN5/**RP32**/RB0	23	TDI/**RP44**/PWM2H/RB12
10	OSCO/CLKO/AN6/**RP33**/RB1	24	**RP45**/PWM2L/RB13
11	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2	25	**RP46**/PWM1H/RB14
12	PGD2/OA2IN-/AN8/**RP35**/RB3	26	**RP47**/PWM1L/RB15
13	PGC2/OA2IN+/**RP36**/RB4	27	$\overline{\text{MCLR}}$
14	PGD3/**RP37**/SDA2/RB5	28	OA1OUT/AN0/CMP1A/IBIAS0/RA0

Note: **RPn** represents remappable peripheral functions.

TABLE 8: 80-PIN TQFP

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/PMD5/RB14	41	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	AN20/RE0	42	RE8
3	**RP47**/PWM1L/PMD6/RB15	43	PGD2/OA2IN-/AN8/**RP35**/RB3
4	AN21/RE1	44	RE9
5	**RP60**/PWM8H/PMD7/RC12	45	PGC2/OA2IN+/**RP36**/RB4
6	**RP61**/PWM8L/PMA5/RC13	46	**RP56**/ASDA1/SCK2/RC8
7	**RP62**/PWM6H/PMA4/RC14	47	**RP57**/ASCL1/SDI2/RC9
8	**RP63**/PWM6L/PMA3/RC15	48	**RP73**/PCI20/RD9
9	$\overline{\text{MCLR}}$	49	**RP72**/SDO2/PCI19/RD8
10	**RP79**/PCI22/PMA2/RD15	50	VSS
11	VSS	51	VDD
12	VDD	52	**RP71**/PMD15/RD7
13	**RP78**/PCI21/RD14	53	**RP70**/PMD14/RD6
14	ANN2/**RP77**/RD13	54	**RP69**/PMA15/PMCS2/RD5
15	AN12/ANN0/**RP48**/RC0	55	PGD3/**RP37**/SDA2/PMA14/PMCS1/PSCS/RB5
16	OA1OUT/AN0/CMP1A/IBIAS0/RA0	56	PGC3/**RP38**/SCL2/RB6
17	AN22/RE2	57	RE10
18	OA1IN-/ANA1/RA1	58	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
19	AN23/RE3	59	RE11
20	OA1IN+/AN9/PMA6/RA2	60	PGD1/AN10/**RP40**/SCL1/RB8
21	DACOUT1/AN3/CMP1C/RA3	61	PGC1/AN11/**RP41**/SDA1/RB9
22	RE4	62	RE12
23	OA3OUT/AN4/CMP3B/IBIAS3/RA4	63	**RP52**/PWM5H/ASDA2/RC4
24	RE5	64	RE13
25	AVDD	65	**RP53**/PWM5L/ASCL2/PMWR/PMENB/PSWR/RC5
26	AVss	66	**RP58**/PWM7H/PMRD/$\overline{\text{PMWR}}$/PSRD/RC10
27	**RP76**/RD12	67	**RP59**/PWM7L/RC11
28	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/PMA7/RC1	68	**RP68**/ASDA3/RD4
29	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/PMD13/PMA13/RC2	69	**RP67**/ASCL3/RD3
30	AN17/ANN1/IBIAS1/**RP54**/PMD12/PMA12/RC6	70	VSS
31	VDD	71	VDD
32	VSS	72	**RP66**/RD2
33	AN15/CMP2A/IBIAS2/**RP51**/PMD11/PMA11/RC3	73	**RP65**/PWM4H/RD1
34	OSCI/CLKI/AN5/**RP32**/PMD10/PMA10/RB0	74	**RP64**/PWM4L/PMD0/RD0
35	OSCO/CLKO/AN6/**RP33**/PMA1/PMALH/PSA1/RB1	75	TMS/**RP42**/PWM3H/PMD1/RB10
36	AN19/CMP2C/**RP75**/PMA0/PMALL/PSA0/RD11	76	TCK/**RP43**/PWM3L/PMD2/RB11
37	RE6	77	RE14
38	AN18/CMP3C/ISRC3/**RP74**/PMD9/PMA9/RD10	78	TDI/**RP44**/PWM2H/PMD3/RB12
39	RE7	79	RE15
40	AN16/ISRC2/**RP55**/PMD8/PMA8/RC7	80	**RP45**/PWM2L/PMD4/RB13

Note: **RPn** represents remappable peripheral functions.

2.4 ICSP Pins

The PGCx and PGDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGCx and PGDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGCx/PGDx pins) programmed into the device matches the physical connections for the ICSP to PICkit™ 3, MPLAB® ICD 3 or MPLAB REAL ICE™ emulator.

For more information on MPLAB ICD 2, MPLAB ICD 3 and REAL ICE emulator connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3 In-Circuit Debugger"* (poster) (DS51765)
- *"Development Tools Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.5 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator (POSC) and a low-frequency Secondary Oscillator (SOSC). For details, see **Section 9.2 "Primary Oscillator (POSC)"**.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

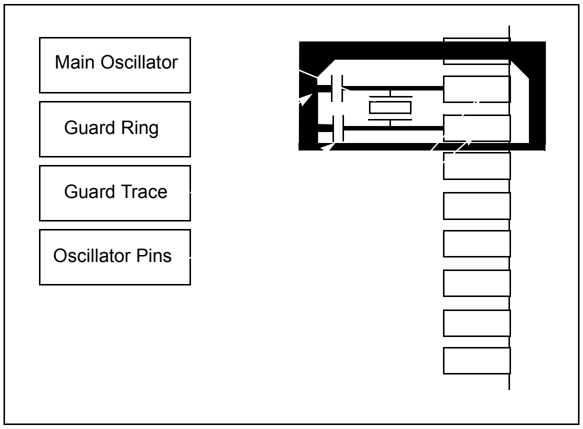
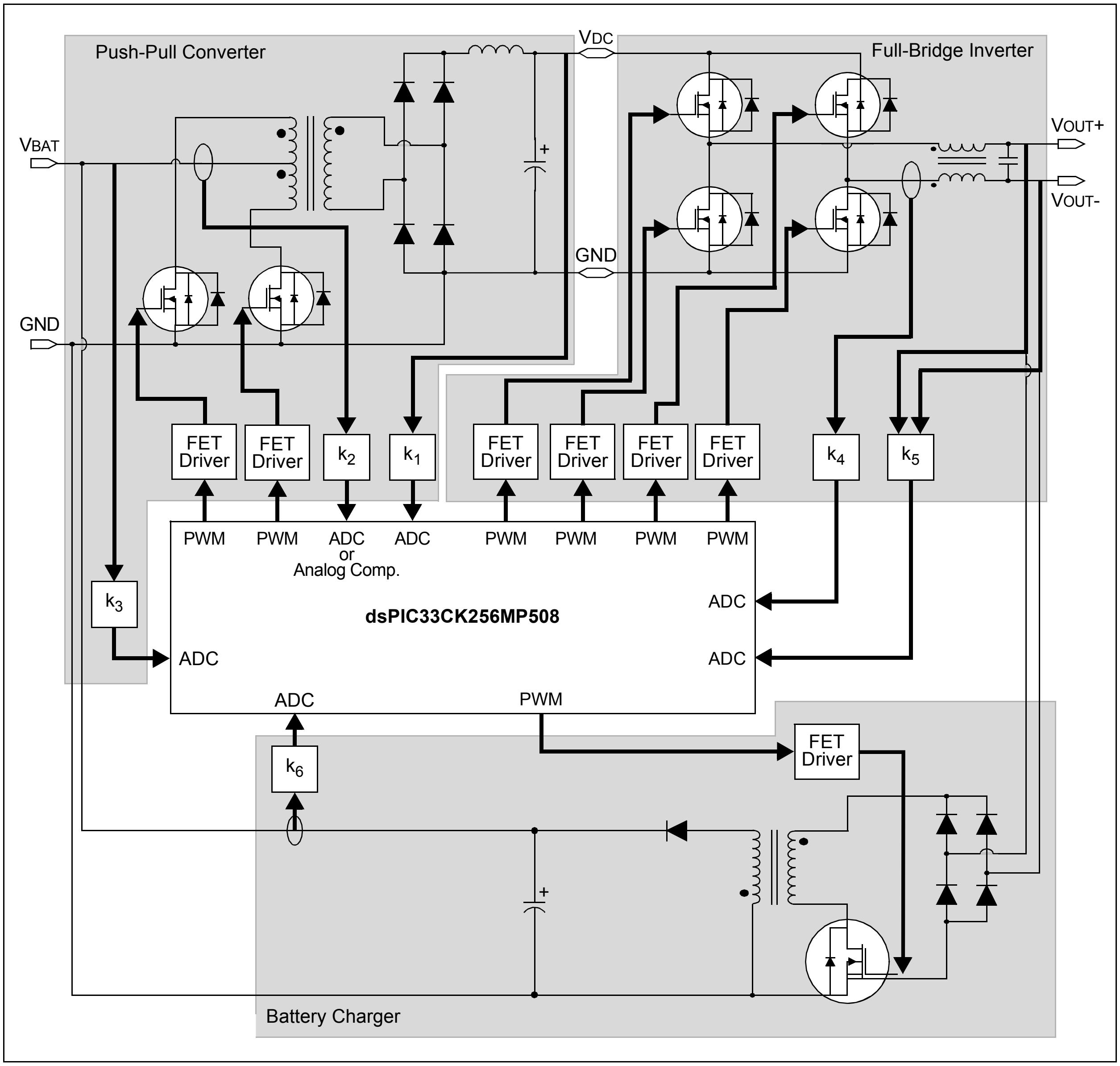


FIGURE 2-6: OFF-LINE UPS



4.4.3.3 Modulo Addressing Applicability

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than, or greater than, the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note:	The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.4.4 BIT-REVERSED ADDRESSING

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.4.4.1 Bit-Reversed Addressing Implementation

Bit-Reversed Addressing mode is enabled in any of these situations:

- BWMx bits (W register selection) in the MODCON register are any value other than ‘1111’ (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is M = 2^N bytes, the last ‘N’ bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Addressing modifier, or ‘pivot point’, which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

TABLE 8-12: PORTE REGISTER SUMMARY

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANSLE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
TRISE	TRISE<15:0>															
PORTE	RE<15:0>															
LATE	LATE<15:0>															
ODCE	ODCE<15:0>															
CNPUE	CNPUE<15:0>															
CNPDE	CNPDE<15:0>															
CNCONE	ON	—	—	—	CNSTYLE	—	—	—	—	—	—	—	—	—	—	—
CNEN0E	CNEN0E<15:0>															
CNSTATE	CNSTATE<15:0>															
CNEN1E	CNEN1E<15:0>															
CNFE	CNFE<15:0>															

REGISTER 8-76: RPOR22: PERIPHERAL PIN SELECT OUTPUT REGISTER 22

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP77R5	RP77R4	RP77R3	RP77R2	RP77R1	RP77R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP76R5	RP76R4	RP76R3	RP76R2	RP76R1	RP76R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP77R<5:0>:** Peripheral Output Function is Assigned to RP77 Output Pin bits
(see Table 8-7 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP76R<5:0>:** Peripheral Output Function is Assigned to RP76 Output Pin bits
(see Table 8-7 for peripheral function numbers)

REGISTER 8-77: RPOR23: PERIPHERAL PIN SELECT OUTPUT REGISTER 23

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP79R5	RP79R4	RP79R3	RP79R2	RP79R1	RP79R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP78R5	RP78R4	RP78R3	RP78R2	RP78R1	RP78R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP79R<5:0>:** Peripheral Output Function is Assigned to RP79 Output Pin bits
(see Table 8-7 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP78R<5:0>:** Peripheral Output Function is Assigned to RP78 Output Pin bits
(see Table 8-7 for peripheral function numbers)

REGISTER 11-54: C1MASKxH: CAN MASK REGISTER x HIGH (x = 0 TO 15)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MIDE	MSID11	MEID17	MEID16	MEID15	MEID14	MEID13
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MEID12	MEID11	MEID10	MEID9	MEID8	MEID7	MEID6	MEID5
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **MIDE:** Identifier Receive Mode bit

1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter

0 = Matches either standard or extended address message if filters match
(i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))

bit 13 **MSID11:** Standard Identifier Mask bit

bit 12-0 **MEID<17:5>:** Extended Identifier Mask bits

In DeviceNet™ mode, these are the mask bits for the first 2 data bytes.

REGISTER 11-55: C1MASKxL: CAN MASK REGISTER x LOW (x = 0 TO 15)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MEID4	MEID3	MEID2	MEID1	MEID0	MSID10	MSID9	MSID8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MSID7	MSID6	MSID5	MSID4	MSID3	MSID2	MSID1	MSID0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-11 **MEID<4:0>:** Extended Identifier Mask bits

In DeviceNet™ mode, these are the mask bits for the first 2 data bytes.

bit 10-0 **MSID<10:0>:** Standard Identifier Mask bits

REGISTER 12-13: PGxCONH: PWM GENERATOR x CONTROL REGISTER HIGH

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
MDCSEL	MPERSEL	MPHSEL	—	MSTEN	UPMOD2	UPMOD1	UPMOD0
bit 15							bit 8

r-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TRGMOD	—	—	SOCS3(1,2,3)	SOCS2(1,2,3)	SOCS1(1,2,3)	SOCS0(1,2,3)
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **MDCSEL:** Master Duty Cycle Register Select bit

1 = PWM Generator uses MDC register
0 = PWM Generator uses PGxDC register

bit 14 **MPERSEL:** Master Period Register Select bit

1 = PWM Generator uses MPER register
0 = PWM Generator uses PGxPER register

bit 13 **MPHSEL:** Master Phase Register Select bit

1 = PWM Generator uses MPHASE register
0 = PWM Generator uses PGxPHASE register

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **MSTEN:** Master Update Enable bit

1 = PWM Generator broadcasts software set/clear of the UPDREQ status bit and EOC signal to other PWM Generators
0 = PWM Generator does not broadcast the UPDREQ status bit state or EOC signal

bit 10-8 **UPMOD<2:0>:** PWM Buffer Update Mode Selection bits

011 = Slaved immediate update
Data registers immediately, or as soon as possible, when a Master update request is received. A Master update request will be transmitted if MSTEN = 1 and UPDATE = 1 for the requesting PWM Generator.
010 = Slaved SOC update
Data registers at start of next cycle if a Master update request is received. A master update request will be transmitted if MSTEN = 1 and UPDATE = 1 for the requesting PWM Generator.
001 = Immediate update
Data registers immediately, or as soon as possible, if UPDATE = 1. The UPDATE status bit will be cleared automatically after the update occurs (UPDATE = 1). The UPDATE status bit will be cleared automatically after the update occurs.
000 = SOC update
Data registers at start of next PWM cycle if UPDATE = 1. The UPDATE status bit will be cleared automatically after the update occurs.(1)

bit 7 **Reserved:** Maintain as ‘0’

Note 1: The PCI selected Sync signal is always available to be OR’d with the selected SOC signal per the SOCS<3:0> bits if the PCI Sync function is enabled.

2: The source selected by the SOCS<3:0> bits MUST operate from the same clock source as the local PWM Generator. If not, the source must be routed through the PCI Sync logic so the trigger signal may be synchronized to the PWM Generator clock domain.

3: PWM Generators are grouped into groups of four: PG1-PG4 and PG5-PG8, if available. Any generator within a group of four may be used to trigger another generator within the same group.

REGISTER 12-19: PGxyPCIL: PWM GENERATOR xy PCI REGISTER LOW (x = PWM GENERATOR #; y = F, CL, FF OR S) (CONTINUED)

bit 4-0 **PSS<4:0>:** PCI Source Selection bits

11111 = CLC1
11110 = Reserved
11101 = Comparator 3 output
11100 = Comparator 2 output
11011 = Comparator 1 output
11010 = PWM Event D
11001 = PWM Event C
11000 = PWM Event B
10111 = PWM Event A
10110 = Device pin, PCI<22>
10101 = Device pin, PCI<21>
10100 = Device pin, PCI<20>
10011 = Device pin, PCI<19>
10010 = RPn input, PCI18R
10001 = RPn input, PCI17R
10000 = RPn input, PCI16R
01111 = RPn input, PCI15R
01110 = RPn input, PCI14R
01101 = RPn input, PCI13R
01100 = RPn input, PCI12R
01011 = RPn input, PCI11R
01010 = RPn input, PCI10R
01001 = RPn input, PCI9R
01000 = RPn input, PCI8R
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = Reserved
00011 = Internally connected to Combo Trigger B
00010 = Internally connected to Combo Trigger A
00001 = Internally connected to the output of PWMPCI<2:0> MUX
00000 = Tied to ‘0’

REGISTER 13-15: ADEIEL: ADC EARLY INTERRUPT ENABLE REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **EIEN<15:0>:** Early Interrupt Enable for Corresponding Analog Inputs bits

1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

REGISTER 13-16: ADEIEH: ADC EARLY INTERRUPT ENABLE REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	EIEN<25:24>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9-0 **EIEN<25:16>:** Early Interrupt Enable for Corresponding Analog Inputs bits

1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

REGISTER 16-2: UxMODEH: UARTx CONFIGURATION REGISTER HIGH (CONTINUED)

bit 2 **UTXINV:** UART Transmit Polarity bit

1 = Inverts TX polarity; TX is low in Idle state
0 = Output data is not inverted; TX output is high in Idle state

bit 1-0 **FLO<1:0>:** Flow Control Enable bits (only valid when MOD<3:0> = 0xxx)

11 = Reserved
10 = $\overline{\text{RTS}}$-$\overline{\text{DSR}}$ (for TX side)/$\overline{\text{CTS}}$-DTR (for RX side) hardware flow control
01 = XON/XOFF software flow control
00 = Flow control off

REGISTER 17-2: SPIxCON1H: SPIx CONTROL REGISTER 1 HIGH (CONTINUED)

bit 6 **FRMSYNC:** Frame Sync Pulse Direction Control bit

1 = Frame Sync pulse input (Slave)
0 = Frame Sync pulse output (Master)

bit 5 **FRMPOL:** Frame Sync/Slave Select Polarity bit

1 = Frame Sync pulse/Slave select is active-high
0 = Frame Sync pulse/Slave select is active-low

bit 4 **MSSEN:** Master Mode Slave Select Enable bit

1 = SPIx Slave select support is enabled with polarity determined by FRMPOL ($\overline{\text{SSx}}$ pin is automatically driven during transmission in Master mode)
0 = Slave select SPIx support is disabled ($\overline{\text{SSx}}$ pin will be controlled by port I/O)

bit 3 **FRMSYPW:** Frame Sync Pulse-Width bit

1 = Frame Sync pulse is one serial word length wide (as defined by MODE<32,16>/WLENGTH<4:0>)
0 = Frame Sync pulse is one clock (SCKx) wide

bit 2-0 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits

Controls the number of serial words transmitted per Sync pulse.
111 = Reserved
110 = Reserved
101 = Generates a Frame Sync pulse on every 32 serial words
100 = Generates a Frame Sync pulse on every 16 serial words
011 = Generates a Frame Sync pulse on every 8 serial words
010 = Generates a Frame Sync pulse on every 4 serial words
001 = Generates a Frame Sync pulse on every 2 serial words (value used by audio protocols)
000 = Generates a Frame Sync pulse on each serial word

Note 1: AUDEN can only be written when the SPIEN bit = 0.
2: AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3: URDTEN is only valid when IGNTUR = 1.
4: AUDMOD<1:0> can only be written when the SPIEN bit = 0 and is only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

REGISTER 19-13: PMRDIN: PARALLEL MASTER PORT READ INPUT DATA REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RDATAIN<15:8>[2]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RDATAIN<7:0>[2]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RDATAIN<15:0>:** Port Read Input Data bits[2]

Note 1: This register is only used when the DUALBUF bit (PMCONH<1>) is set to ‘1’ and exclusively for reads. If the DUALBUF bit is ‘0’, the PMDIN1 register (Register 19-7) is used for reads instead of PMRDIN.

2: Only used when MODE16 = 1.

26.1 Current Bias Generator Control Registers

REGISTER 26-1: BIASCON: CURRENT BIAS GENERATOR CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	I10EN3	I10EN2	I10EN1	I10EN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Current Bias Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14-4 **Unimplemented:** Read as ‘0’

bit 3 **I10EN3:** 10 µA Enable for Output 3 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 2 **I10EN2:** 10 µA Enable for Output 2 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 1 **I10EN1:** 10 µA Enable for Output 1 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

bit 0 **I10EN0:** 10 µA Enable for Output 0 bit
1 = 10 µA output is enabled
0 = 10 µA output is disabled

REGISTER 28-7: DMTPSCNTL: DMT POST-CONFIGURE COUNT STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT<15:0>:** Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

REGISTER 28-8: DMTPSCNTH: DMT POST-CONFIGURE COUNT STATUS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT<31:16>:** Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles[1]	Status Flags Affected
61	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit Literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit Literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
62	MOVPAG	MOVPAG #lit10,DSRPAG	Move 10-bit Literal to DSRPAG	1	1	None
		MOVPAG #lit8,TBLPAG	Move 8-bit Literal to TBLPAG	1	1	None
		MOVPAG Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAG Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
64	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and Store Accumulator	1	1	None
65	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
66	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
67	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd, AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
68	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Signed(Ws)	1	1	None
		MUL.SS Wb,Ws,Acc	Accumulator = Signed(Wb) * Signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU Wb,Ws,Acc	Accumulator = Signed(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Acc	Accumulator = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Signed(Ws)	1	1	None
		MUL.US Wb,Ws,Acc	Accumulator = Unsigned(Wb) * Signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MUL.UU Wb,#lit5,Acc	Accumulator = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU Wb,Ws,Acc	Accumulator = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MULW.SS Wb,Ws,Wnd	Wnd = Signed(Wb) * Signed(Ws)	1	1	None
		MULW.SU Wb,Ws,Wnd	Wnd = Signed(Wb) * Unsigned(Ws)	1	1	None
		MULW.US Wb,Ws,Wnd	Wnd = Unsigned(Wb) * Signed(Ws)	1	1	None
		MULW.UU Wb,Ws,Wnd	Wnd = Unsigned(Wb) * Unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.SU Wb,#lit5,Wnd	Wnd = Signed(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	Wnd = Unsigned(Wb) * Unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

2: The divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

32.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

32.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

32.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

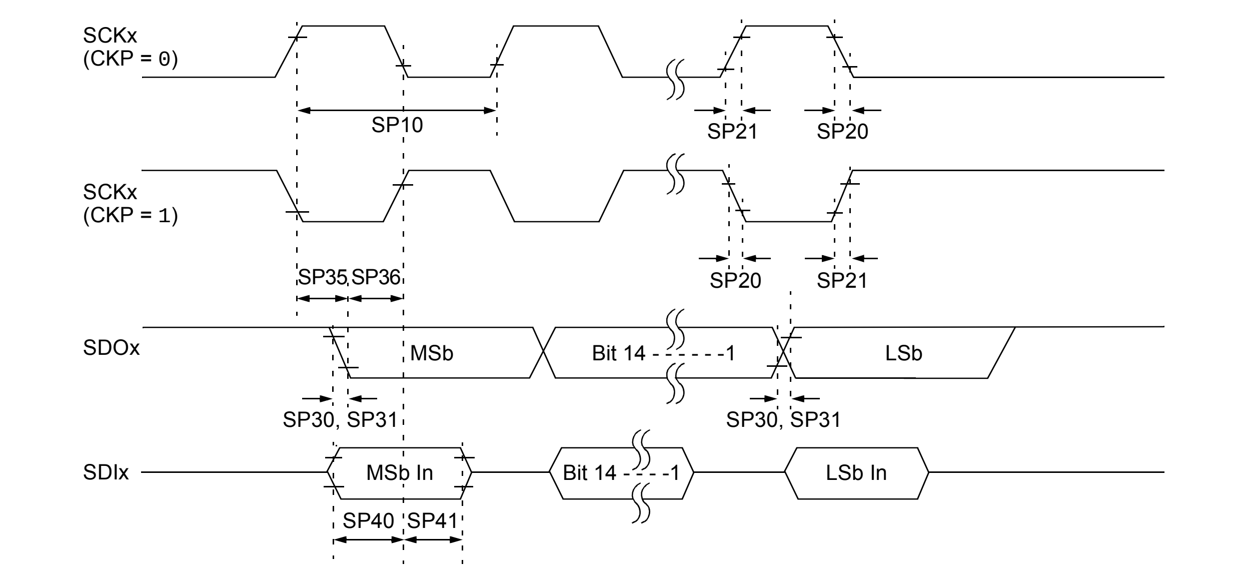
- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

32.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

FIGURE 33-10: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 33-1 for load conditions.

TABLE 33-30: SPIx MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristic[1]**	**Min.**	**Typ.[2]**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCKx Frequency	—	—	15	MHz	Using PPS pins
			—	—	40	MHz	SPIx dedicated pins
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	Using PPS pins
			20	—	—	ns	SPIx dedicated pins
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			10	—	—	ns	SPIx dedicated pins
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			15	—	—	ns	SPIx dedicated pins

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.