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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

| Product Status | Active |
|----------------------------|--|
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 100MHz |
| Connectivity | CANbus, I ² C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT |
| Number of I/O | 53 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24К х 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 20x12b; D/A 3x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck256mp506-e-pt |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

dsPIC33CK256MP508 FAMILY



5.5.4 ECC CONTROL REGISTERS

REGISTER 5-6: ECCCONL: ECC FAULT INJECTION CONFIGURATION REGISTER LOW

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|--------|-----|-----|-----|-----|-----|-----|--------|
| — | — | — | — | — | — | — | _ |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| — | — | — | — | — | — | — | FLTINJ |
| bit 7 | | | | | • | | bit 0 |
| | | | | | | | , |

Legend:

bit 0

| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
|-------------------|------------------|------------------------------------|--------------------|
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-1 Unimplemented: Read as '0'

FLTINJ: Fault Injection Sequence Enable bit

1 = Enabled

0 = Disabled

REGISTER 5-7: ECCCONH: ECC FAULT INJECTION CONFIGURATION REGISTER HIGH

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--------------|----------------------------------|--|-------------------------------------|------------------------------------|------------------------------------|--------------------|-------|
| | | | FLT2P | TR<7:0> | | | |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | | | FLT1P | TR<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| Lanandi | | | | | | | |
| Legena: | I I.:4 | | | | | -l (0) | |
| R = Readab | ie dit | vv = vvritable | DIT | U = Unimplemented bit, read | | as U | |
| -n = Value a | t POR | '1' = Bit is set | | '0' = Bit is cleared | | x = Bit is unknown | |
| | 11111111 00110111 = • | • Fault injection | 5 Fault injectio (bit inversion) | on occurs) occurs on bit | 55 of ECC bit o | order | |
| | 00000001 = 00000000 = | Fault injectionFault injection | (bit inversion) (bit inversion) |) occurs on bit) occurs on bit | 1 of ECC bit on 0 of ECC bit on | rder rder | |
| bit 0 | FLT1PTR<7 | :0>: ECC Fault | njection Bit P | ointer 1 bits | | | |
| | 11111111 00110111 = • • | 00111000 = No Fault injection | Fault injectio occurs on bit | n occurs 55 of ECC bit | order | | |
| | 00000001 = 000000000 = | Fault injection Fault injection | occurs on bit occurs on bit | 1 of ECC bit o 0 of ECC bit o | rder rder | | |

REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

| U-0 | U-0 | R-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|-----------------|---------------------------------------|-------------------|-----------------|------------------|------------------|--------------------|------------------|
| | | VHOLD | — | ILR3 | ILR2 | ILR1 | ILR0 |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| VECNUM7 | VECNUM6 | VECNUM5 | VECNUM4 | VECNUM3 | VECNUM2 | VECNUM1 | VECNUM0 |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |
| R = Readable | bit | W = Writable | bit | U = Unimpler | mented bit, reac | l as '0' | |
| -n = Value at F | POR | '1' = Bit is set | | '0' = Bit is cle | ared | x = Bit is unkr | nown |
| | | | | | | | |
| bit 15-14 | Unimplemen | ted: Read as ' | כ' | | | | |
| bit 13 | VHOLD: Vect | or Number Ca | oture Enable b | bit | | | |
| | 1 = VECNUM | 1<7:0> bits read | l current value | of vector numb | per encoding tre | e (i.e., highest p | priority pending |
| | nterrupt) | umber latched iu | nto VECNIUM∢ | <7·0> at Interru | int Acknowledge | and retained u | Intil nevt IACK |
| hit 12 | | ted: Read as ' | | | princip | | |
| bit 11_8 | | | ot Priority Lev | al hite | | | |
| bit 11-0 | 1111 = CPU | Interrunt Priorit | v Level is 15 | | | | |
| | | interrupt i nom | | | | | |
| | 0001 = CPU | Interrupt Priorit | y Level is 1 | | | | |
| | 0000 = CPU | Interrupt Priorit | y Level is 0 | | | | |
| bit 7-0 | VECNUM<7:0 | D>: Vector Num | ber of Pendin | g Interrupt bits | 6 | | |
| | 11111111 = 2 | 255, Reserved | ; do not use | | | | |
| | | 9 IC1 – Input (| Canture 1 | | | | |
| | 00001000 = 8 | 8, INT0 – Exter | nal Interrupt (|) | | | |
| | 00000111 = 7, Reserved; do not use | | | | | | |
| | 00000110 = 6, Generic soft error trap | | | | | | |
| | 00000101 = | 5, Reserved; d | o not use | | | | |
| | 00000100 = 4 | 4, Math error tr | ар | | | | |
| | 00000011 = 3 | 3, Slack error t | lap h trop | | | | |
| | 00000010 = 1 | 2, Generic fial | n tran | | | | |
| | 00000000 = (| 0, Oscillator fai | l trap | | | | |

| R/W-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| ICM3R7 | ICM3R6 | ICM3R5 | ICM3R4 | ICM3R3 | ICM3R2 | ICM3R1 | ICM3R0 |
| bit 15 | • | | | | | | bit 8 |
| | | | | | | | |
| R/W-0 |
| TCKI3R7 | TCKI3R6 | TCKI3R5 | TCKI3R4 | TCKI3R3 | TCKI3R2 | TCKI3R1 | TCKI3R0 |
| bit 7 | | | | | | | bit 0 |

REGISTER 8-19: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5

|--|

| Legend: | | | |
|-------------------|------------------|-----------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read | as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 ICM3R<7:0>: Assign SCCP Capture 3 (ICM3) Input to the Corresponding RPn Pin bits See Table 8-4.

bit 7-0 TCKI3R<7:0>: Assign SCCP Timer3 (TCKI3) Input to the Corresponding RPn Pin bits See Table 8-4.

REGISTER 8-20: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ICM4R7 | ICM4R6 | ICM4R5 | ICM4R4 | ICM4R3 | ICM4R2 | ICM4R1 | ICM4R0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TCKI4R7 | TCKI4R6 | TCKI4R5 | TCKI4R4 | TCKI4R3 | TCKI4R2 | TCKI4R1 | TCKI4R0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|-------------------|------------------|-----------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read | l as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 ICM4R<7:0>: Assign SCCP Capture 4 (ICM4) Input to the Corresponding RPn Pin bits See Table 8-4.

bit 7-0 TCKI4R<7:0>: Assign SCCP Timer4 (TCKI4) Input to the Corresponding RPn Pin bits See Table 8-4.

| REGISTER 9-3: | PLLFBD: PLL FEEDBACK DIVIDER REGISTER |
|---------------|---------------------------------------|
| | |

| U-0 | U-0 | U-0 | U-0 | r-0 | r-0 | r-0 | r-0 |
|--------------|----------------|--|----------------|------------------|------------------|-----------------|-------|
| — | — | — | — | — | — | _ | — |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-0 |
| | | | PLLFB | DIV<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | r = Reserved b | pit | | | | |
| R = Readab | ole bit | W = Writable t | pit | U = Unimpler | nented bit, read | d as '0' | |
| -n = Value a | at POR | '1' = Bit is set | | '0' = Bit is cle | ared | x = Bit is unkr | nown |
| | | | | | | | |
| bit 15-12 | Unimpleme | nted: Read as '0 | , | | | | |
| bit 11-8 | Reserved: N | /laintain as '0' | | | | | |
| bit 7-0 | PLLFBDIV< | 7:0>: PLL Feedb | oack Divider b | its (also denote | ed as 'M', PLL r | nultiplier) | |
| | 11111111 = | Reserved | | | | | |
| | 11001000 = | 200 Maximum ⁽¹ |) | | | | |
| | 10010110 = | 150 (default) | | | | | |
| | 00010000 = | [:] 16 Minimum ⁽¹⁾ | | | | | |
| | 00000010 = | Reserved | | | | | |

- 00000001 = Reserved 00000000 = Reserved
- **Note 1:** The allowed range is 16-200 (decimal). The rest of the values are reserved and should be avoided. The power on the default feedback divider is 150 (decimal) with an 8 MHz FRC input clock. The VCO frequency is 1.2 GHz.

REGISTER 10-2: DMACHn: DMA CHANNEL n CONTROL REGISTER

| U-0 | U-0 | U-0 | r-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|--------|-----|-----|-----|-----|-------|-----------------------|----------------------|
| — | — | — | — | — | NULLW | RELOAD ⁽¹⁾ | CHREQ ⁽³⁾ |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---------|---------|---------|---------|---------|---------|-------|-------|
| SAMODE1 | SAMODE0 | DAMODE1 | DAMODE0 | TRMODE1 | TRMODE0 | SIZE | CHEN |
| bit 7 | | | | | | | bit 0 |

| Legend: | r = Reserved bit | | |
|-------------------|------------------|-----------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read | l as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

| bit 15-13 | Unimplemented: Read as '0' |
|------------|--|
| bit 12 | Reserved: Maintain as '0' |
| bit 11 | Unimplemented: Read as '0' |
| bit 10 | NULLW: Null Write Mode bit |
| | 1 = A dummy write is initiated to DMASRCn for every write to DMADSTn 0 = No dummy write is initiated |
| bit 9 | RELOAD: Address and Count Reload bit ⁽¹⁾ |
| | 1 = DMASRCn, DMADSTn and DMACNTn registers are reloaded to their previous values upon the start of the next operation 0 = DMASRCn, DMADSTn and DMACNTn are not reloaded on the start of the next operation⁽²⁾ |
| bit 8 | CHREQ: DMA Channel Software Request bit ⁽³⁾ |
| | 1 = A DMA request is initiated by software; automatically cleared upon completion of a DMA transfer 0 = No DMA request is pending |
| bit 7-6 | SAMODE<1:0>: Source Address Mode Selection bits |
| | 11 = DMASRCn is used in Peripheral Indirect Addressing and remains unchanged 10 = DMASRCn is decremented based on the SIZE bit after a transfer completion 01 = DMASRCn is incremented based on the SIZE bit after a transfer completion 00 = DMASRCn remains unchanged after a transfer completion |
| bit 5-4 | DAMODE<1:0>: Destination Address Mode Selection bits |
| | 11 = DMADSTn is used in Peripheral Indirect Addressing and remains unchanged 10 = DMADSTn is decremented based on the SIZE bit after a transfer completion 01 = DMADSTn is incremented based on the SIZE bit after a transfer completion 00 = DMADSTn remains unchanged after a transfer completion |
| bit 3-2 | TRMODE<1:0>: Transfer Mode Selection bits |
| | 11 = Repeated Continuous 10 = Continuous 01 = Repeated One-Shot 00 = One-Shot |
| bit 1 | SIZE: Data Size Selection bit |
| | 1 = Byte (8-bit) 0 = Word (16-bit) |
| bit 0 | CHEN: DMA Channel Enable bit |
| | 1 = The corresponding channel is enabled 0 = The corresponding channel is disabled |
| Note 1: On | Ity the original DMACNTn is required to be stored to recover the original DMASRCn and DMADSTn values. |

- 2: DMACNTn will always be reloaded in Repeated mode transfers, regardless of the state of the RELOAD bit.
- 3: The number of transfers executed while CHREQ is set depends on the configuration of TRMODE<1:0>.

REGISTER 12-9: LOGCONY: COMBINATORIAL PWM LOGIC CONTROL REGISTER y⁽²⁾ (CONTINUED)

- bit 7 S1yPOL: Combinatorial PWM Logic Source #1 Polarity bit 1 = Input is inverted 0 = Input is positive logic bit 6 S2yPOL: Combinatorial PWM Logic Source #2 Polarity bit 1 = Input is inverted 0 = Input is positive logic bit 5-4 **PWMLFy<1:0>:** Combinatorial PWM Logic Function Selection bits 11 = Reserved 10 = PWMS1y ^ PWMS2y (XOR) 01 = PWMS1y & PWMS2y (AND) 00 = PWMS1y | PWMS2y (OR)bit 3 Unimplemented: Read as '0' PWMLFyD<2:0>: Combinatorial PWM Logic Destination Selection bits⁽³⁾ bit 2-0 111 = Logic function is assigned to PWM8H or PWM8L pin 110 = Logic function is assigned to PWM7H or PWM7L pin 101 = Logic function is assigned to PWM6H or PWM6L pin
 - 100 = Logic function is assigned to PWM5H or PWM5L pin
 - 011 = Logic function is assigned to PWM4H or PWM4L pin
 - 010 = Logic function is assigned to PWM3H or PWM3L pin
 - 001 = Logic function is assigned to PWM2H or PWM2L pin
 - 000 = No assignment, combinatorial PWM logic function is disabled
- **Note 1:** Logic function input will be connected to '0' if the PWM channel is not present.
 - 2: 'y' denotes a common instance (A-F).
 - **3:** Instances of y = A, C, E of LOGCONy assign logic function output to the PWMxL pin. Instances of y = B, D, F of LOGCONy assign logic function to the PWMxH pin.

| R/W-0 | R-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---------------|-----------------------------------|--|------------------------------|-------------------|------------------|-----------------|-----------------|
| SLPEN | ACTIVE | | — | BCLKMOD | BCLKSEL1 | BCLKSEL0 | HALFDPLX |
| bit 15 | | | | | | | bit 8 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| RUNOVE | | STSFL1 | STSFI 0 | COEN | UTXINV | FLO1 | FL Q0 |
| bit 7 | | 0.011 | 0.0100 | | • | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |
| R = Readable | e bit | W = Writable b | oit | U = Unimplem | nented bit, read | l as '0' | |
| -n = Value at | POR | '1' = Bit is set | | '0' = Bit is clea | ared | x = Bit is unkr | nown |
| bit 15 | SI DEN: Run (| During Sleen Fi | nable bit | | | | |
| bit 10 | | G clock runs du | ring Sleep | | | | |
| | 0 = UART BR | G clock is turne | d off during SI | еер | | | |
| bit 14 | ACTIVE: UAR | T Running Stat | us bit | | | | |
| | | ck request is ac | tive (user can | not update the | | ODEH register | rs) |
| bit 13-12 | Unimplement | ed: Read as '0 | | | | | 5) |
| bit 11 | BCLKMOD: B | aud Clock Gen | eration Mode | Select bit | | | |
| 2 | 1 = Uses fract | ional Baud Rate | e Generation | 001001.211 | | | |
| | 0 = Uses lega | cy divide-by-x c | ounter for bau | d clock generati | on (x = 4 or 16 | depending on | the BRGH bit) |
| bit 10-9 | BCLKSEL<1: | 0>: Baud Clock | Source Selec | tion bits | | | |
| | 11 = AFvco/3 | | | | | | |
| | 10 = FOSC 01 = Reserved | d | | | | | |
| | 00 = Fosc/2 (I | FP) | | | | | |
| bit 8 | HALFDPLX: L | JART Half-Dup | lex Selection N | /lode bit | | | |
| | 1 = Half-Duple | ex mode: UxTX | is driven as ar | n output when t | ransmitting and | tri-stated whe | n TX is Idle |
| hit 7 | | x mode: Ux I X I | s driven as an | output at all tim | es when both l | JARIEN and U | I XEN are set |
| DIL 7 | 1 = When an | Overflow Error | | tition is detecte | d the RX shift | er continues tr | run so as to |
| | remain sy | inchronized wit | h incoming R | K data; data is i | not transferred | to UxRXREG | when it is full |
| | (i.e., no U | xRXREG data | is overwritten) | | | | Para da la fa |
| | 0 = when an (Legacy n | Overflow Error node) | (UERR) cond | lition is detecte | a, the RX shift | er stops accep | ting new data |
| bit 6 | URXINV: UAR | T Receive Pola | arity bit | | | | |
| | 1 = Inverts RX 0 = Input is no | (polarity; Idle s t inverted; Idle | tate is low state is high | | | | |
| bit 5-4 | STSEL<1:0>: | Number of Sto | p Bits Selectio | n bits | | | |
| | 11 = 2 Stop bi | ts sent, 1 check | ked at receive | | | | |
| | 10 = 2 Stop bi | ts sent, 2 check | ked at receive | ivo | | | |
| | 00 = 1 Stop bi | t sent, 1 checke | ed at receive | | | | |
| bit 3 | COEN: Enable | e Legacy Check | sum (C0) Trar | smit and Rece | ive bit | | |
| | 1 = Checksum | n Mode 1 (enhar | nced LIN chec | ksum in LIN mo | de; add all TX/ | RX words in all | other modes) |
| | 0 = Checksum | n Mode 0 (legad | y LIN checksu | Im in LIN mode | ; not used in al | I other modes) | |
| | | | | | | | |

REGISTER 16-2: UXMODEH: UARTX CONFIGURATION REGISTER HIGH

REGISTER 16-7: UxRXREG: UARTx RECEIVE BUFFER REGISTER

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|--------|-----|-----|-------|--------|-----|-----|-------|
| _ | — | — | — | | — | — | — |
| bit 15 | - | | | • | | | bit 8 |
| | | | | | | | |
| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | | | RXREC | G<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |

| Legend: | | | |
|-------------------|------------------|-----------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read | l as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **RXREG<7:0>:** Received Character Data bits 7-0

REGISTER 16-8: UXTXREG: UARTX TRANSMIT BUFFER REGISTER

| W-x | U-0 |
|--------|-----|-----|-----|-----|-----|-----|-------|
| LAST | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TXREG7 | TXREG6 | TXREG5 | TXREG4 | TXREG3 | TXREG2 | TXREG1 | TXREG0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|-------------------|------------------|-----------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read | l as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

| bit 15 LASI: Last Byte Indicator for Smart Card Support |
|---|
|---|

bit 14-8 Unimplemented: Read as '0'

bit 7-0 TXREG<7:0>: Transmitted Character Data bits 7-0

If the buffer is full, further writes to the buffer are ignored.

REGISTER 17-4: SPIxSTATL: SPIx STATUS REGISTER LOW (CONTINUED)

- bit 3 SPITBE: SPIx Transmit Buffer Empty Status bit 1 = SPIxTXB is empty 0 = SPIxTXB is not empty Standard Buffer Mode: Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR. Automatically cleared in hardware when SPIxBUF is written, loading SPIxTXB. Enhanced Buffer Mode: Indicates TXELM<5:0> = 000000. bit 2 Unimplemented: Read as '0' bit 1 SPITBF: SPIx Transmit Buffer Full Status bit 1 = SPIxTXB is full 0 = SPIxTXB not full Standard Buffer Mode: Automatically set in hardware when SPIxBUF is written, loading SPIxTXB. Automatically cleared in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR. Enhanced Buffer Mode: Indicates TXELM<5:0> = 111111. SPIRBF: SPIx Receive Buffer Full Status bit bit 0 1 = SPIxRXB is full 0 = SPIxRXB is not full Standard Buffer Mode: Automatically set in hardware when SPIx transfers data from SPIxRXSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB. Enhanced Buffer Mode: Indicates RXELM<5:0> = 111111.
- **Note 1:** SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

REGISTER 19-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER (CONTINUED)

- bit 3 CS1P: Chip Select 1 Polarity bit⁽¹⁾ 1 = Active-high 0 = Active-low bit 2 Unimplemented: Read as '0' bit 1 WRSP: Write Strobe Polarity bit For Slave Modes and Master Mode 2 (MODE<1:0> (PMMODE<9:8>) = 00, 01, 10): 1 = Write strobe is active-high (PMWR) 0 = Write strobe is active-low (PMWR) For Master Mode 1 (MODE<1:0> (PMMODE<9:8>) = 11): 1 = Enables strobe active-high (PMENB) 0 = Enables strobe active-low (PMENB) bit 0 RDSP: Read Strobe Polarity bit For Slave Modes and Master Mode 2 (MODE<1:0> (PMMODE<9:8>) = 00, 01, 10): 1 = Read strobe is active-high (PMRD) 0 = Read strobe is active-low (PMRD)For Master Mode 1 (MODE<1:0> (PMMODE<9:8>) = 11): 1 = Read/write strobe is active-high (PMRD/PMWR) 0 = Read/write strobe is active-low (PMRD/PMWR)
- **Note 1:** These bits have no effect when their corresponding pins are used as address lines.

REGISTER 23-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

- bit 2-0 DS1<2:0>: Data Selection MUX 1 Signal Selection bits
 - 111 = SCCP4 auxiliary out
 - 110 = SCCP2 auxiliary out
 - 101 = Reserved
 - 100 = REFCLKO output
 - 011 = INTRC/LPRC clock source
 - 010 = CLC3 out
 - 001 = System clock (FCY)
 - 000 = CLCINA I/O pin
- Note 1: Valid only when SPI is used on PPS.

REGISTER 24-11: PTGADJ: PTG ADJUST REGISTER⁽¹⁾

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|------------------|-------|------------------|-------|------------------|-----------------|-----------------|-------|
| | | | PTGAI | DJ<15:8> | | | |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | | | PTGA | .DJ<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit | | W = Writable k | oit | U = Unimpler | mented bit, rea | ad as '0' | |
| -n = Value at F | 'OR | '1' = Bit is set | | '0' = Bit is cle | ared | x = Bit is unkr | nown |

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits This register holds the user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 register using the PTGADD command.

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 24-12: PTGL0: PTG LITERAL 0 REGISTER^(1,2)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--------------------|-------|------------------|-------|------------------|-----------------|----------------|-------|
| | | | PTGL | _0<15:8> | | | |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | | | PTG | L0<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |
| R = Readable bit W | | W = Writable bi | it | U = Unimpler | mented bit, rea | ad as '0' | |
| -n = Value at F | POR | '1' = Bit is set | | '0' = Bit is cle | ared | x = Bit is unk | nown |

bit 15-0 PTGL0<15:0>: PTG Literal 0 Register bits

This register holds the 6-bit value to be written to the CNVCHSEL<5:0> bits (ADCON3L<5:0>) with the PTGCTRL Step command.

- Note 1: These bits are read-only when the module is executing Step commands.
 - 2: The PTG strobe output is typically connected to the ADC Channel Select register. This allows the PTG to directly control ADC channel switching. See the specific device data sheet for connections of the PTG output.

26.0 CURRENT BIAS GENERATOR (CBG)

- Note 1: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Current Bias Generator (CBG)" (DS70005253) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Current Bias Generator (CBG) consists of two classes of current sources: 10 μ A and 50 μ A sources. The major features of each current source are:

- 10 µA Current Sources:
 - Current sourcing only
 - Up to four independent sources
- 50 µA Current Sources:
 - Selectable current sourcing or sinking
 - Selectable current mirroring for sourcing and sinking

A simplified block diagram of the CBG module is shown in Figure 26-1.





REGISTER 30-21: WDTCONL: WATCHDOG TIMER CONTROL REGISTER LOW

| R/W-0 | U-0 | U-0 | R-y | R-y | R-y | R-y | R-y | |
|---|---|--|------------------------|---|------------------------|------------------------|-------------------------|--|
| ON ^(1,2) | _ | _ | RUNDIV4 ⁽³⁾ | RUNDIV3 ⁽³⁾ | RUNDIV2 ⁽³⁾ | RUNDIV1 ⁽³⁾ | RUNDIV0 ⁽³⁾ | |
| bit 15 | | | | | | | bit 8 | |
| | | | | | | | | |
| R | R | R-y | R-y | R-y | R-y | R-y | R/W-0, HS | |
| CLKSEL1 | ^(3,5) CLKSEL0 ^(3,5) | SLPDIV4 ⁽³⁾ | SLPDIV3 ⁽³⁾ | SLPDIV2 ⁽³⁾ | SLPDIV1 ⁽³⁾ | SLPDIV0 ⁽³⁾ | WDTWINEN ⁽⁴⁾ | |
| bit 7 | | | | | | | bit 0 | |
| | | | | | | | | |
| Legend: | nd: HS = Hardware Settable bit | | y = Value fror | n Configuratior | n bit on POR | | | |
| R = Reada | able bit | W = Writable | bit | U = Unimplen | nented bit, rea | d as '0' | | |
| -n = Value | at POR | '1' = Bit is set | | '0' = Bit is cle | ared | x = Bit is unkr | iown | |
| bit 15 ON: Watchdog Timer Enable bit^(1,2) 1 = Enables the Watchdog Timer if it is not enabled by the device configuration 0 = Disables the Watchdog Timer if it was enabled in software | | | | | | | | |
| bit 14-13 | Unimplemen | ted: Read as ' |)' | | | | | |
| bit 12-8 | RUNDIV<4:0 | >: WDT Run M | ode Postscaler | ⁻ Status bits ⁽³⁾ | | | | |
| | 11111 = Divi | de by 2 ^ 30 = 1 | ,073,741,824 | | | | | |
| | 11110 = Divi | de by 2 ^ 29 = 5 | 526,870,912 | | | | | |
| | 00001 = Divid 00000 = Divid | 00001 = Divide by 2 ^ 2, 4 00000 = Divide by 2 ^ 1, 2 | | | | | | |
| bit 7-6 | CLKSEL<1:0 | >: WDT Run M | ode Clock Sel | ect Status bits ⁽ | 3,5) | | | |
| | 11 = LPRC C | scillator | | | | | | |
| | 01 = Reserve | d | | | | | | |
| | 00 = SYSCL | K | | | (2) | | | |
| bit 5-1 | SLPDIV<4:0> | Sleep and Idl | e Mode WDT I | Postscaler Stat | us bits ⁽³⁾ | | | |
| | 11111 = Divi 11110 = Divi | 11111 = Divide by 2 ^ 30 = 1,073,741,824 11110 = Divide by 2 ^ 29 = 526,870,912 | | | | | | |
| | 00001 = Divi 00000 = Divi | de by 2 ^ 2, 4 de by 2 ^ 1, 2 | | | | | | |
| bit 0 | WDTWINEN: | Watchdog Tim | er Window Ena | able bit ⁽⁴⁾ | | | | |
| | 1 = Enables \ 0 = Disables ' | Vindow mode Window mode | | | | | | |
| Note 1: | A read of this bit v | will result in a '1 | ' if the WDT is | enabled by the | e device config | juration or by s | oftware. | |
| 2: | The user's softwar following the instr | re should not re uction that clea | ead or write the | e peripheral's S s ON bit. | FRs in the SY | SCLK cycle im | mediately | |

- **3:** These bits reflect the value of the Configuration bits.
- 4: The WDTWINEN bit reflects the status of the Configuration bit if the bit is set. If the bit is cleared, the value is controlled by software.
- 5: The available clock sources are device-dependent.

FIGURE 33-17: UARTX MODULE I/O TIMING CHARACTERISTICS



TABLE 33-35: UARTX MODULE I/O TIMING REQUIREMENTS

| Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ | | | | | | | |
|---|---------|---|------|---------------------|------|-------|------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| UA10 | TUABAUD | UARTx Baud Time | 40 | | | ns | |
| UA11 | FBAUD | UARTx Baud Frequency | — | _ | 25 | Mbps | |
| UA20 | TCWF | Start Bit Pulse Width to Trigger UARTx Wake-up | 50 | _ | | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

| | MILLIMETERS | | | |
|--------------------------|-------------|----------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | Ν | 48 | | |
| Lead Pitch | е | 0.50 BSC | | |
| Overall Height | А | - | - | 1.20 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | ø | 0° | 3.5° | 7° |
| Overall Width | E | 9.00 BSC | | |
| Overall Length | D | 9.00 BSC | | |
| Molded Package Width | E1 | 7.00 BSC | | |
| Molded Package Length | D1 | 7.00 BSC | | |
| Lead Thickness | С | 0.09 | - | 0.16 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.
- 3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. DatumsA-B and to be determined at center line between leads where leads exit plastic body at datum plane

Microchip Technology Drawing C04-300-PT Rev A Sheet 2 of 2

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|--------------------------|----|-------------|----------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | Е | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X28) | X1 | | | 0.30 |
| Contact Pad Length (X28) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

| ECCCONH (ECC Fault Injection |
|---|
| Configuration High)88 |
| ECCCONL (ECC Fault Injection |
| Configuration Low)88 |
| ECCSTATH (ECC System Status Display High)90 |
| ECCSTATL (ECC System Status Display Low)90 |
| FALTREG Configuration |
| FBOOT Configuration |
| FBSLIM Configuration |
| FBISEQ Configuration |
| FDEVOPT Configuration |
| FDMT Configuration |
| FDMTCNTH Configuration |
| FDMTICNTL Configuration |
| FDMTIVTL Configuration |
| FDIVITIVIL Configuration 515 |
| FICD Configuration 514 |
| FOSC Configuration 511 |
| FOSCSEL Configuration 510 |
| FPOR Configuration |
| FSCL (Frequency Scale) |
| FSEC Configuration 500 |
| FSIGN Configuration |
| Minimum Poriod) 260 |
| EWDT Configuration 512 |
| 12CxCONH (I2Cx Control High) 307 |
| I2CXCONH (I2CX Control Low) 397 |
| I2CXNCONE (I2CX CONTO LOW) |
| I2CXMISK (I2CX Slave Mode Address Mask) |
| IBIASCONH (Current Bias Generator Current |
| Source Control High) 479 |
| |
| |
| Current Source Control Low) 480 |
| Current Source Control Low) |
| Current Source Control Low) |
| Current Source Control Low) |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXxHLD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXxHLD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXxHLD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXxHLD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXxLDD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTEG (Interrupt Control 4) 113 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXXHLD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTREG (Interrupt Control 4) 113 INTXTMRH (Interval x Timer High) 344 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXxCNTL (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTREG (Interrupt Control and Status) 113 INTxTMRH (Interval x Timer High) 344 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Low) 346 INDXxCNTL (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTREG (Interrupt Control and Status) 113 INTxTMRH (Interval x Timer High) 344 INTxTMRL (Interval x Timer Low) 344 INTXHLDH (Interval x Timer Hold High) 345 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXxHLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTTREG (Interrupt Control and Status)113INTxTMRH (Interval x Timer High)344INTXHLDH (Interval x Timer Low)345INTXHLDL (Interval x Timer Hold Low)345 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXxHLD (Index x Counter Low)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control and Status)113INTXTMRH (Interval x Timer High)344INTXHLDH (Interval x Timer Hold High)345INTXHLDL (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXxHLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control and Status)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Hold) 346 INDXxHLD (Index x Counter Low) 346 INDXXHLD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTREG (Interrupt Control and Status) 113 INTXTMRH (Interval x Timer High) 344 INTXTMRL (Interval x Timer Hold High) 345 INTXXHLDH (Interval x Timer Hold Low) 345 LATx (Output Data for PORTx) 120 LFSR (Linear Feedback Shift) 269 LOGCONy (Combinatorial PWM Logic 101 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Hold) 346 INDXxHLD (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTREG (Interrupt Control and Status) 113 INTXTMRH (Interval x Timer High) 344 INTXTMRL (Interval x Timer Hold High) 345 INTXHLDH (Interval x Timer Hold Low) 345 LATx (Output Data for PORTx) 120 LFSR (Linear Feedback Shift) 269 LOGCONy (Combinatorial PWM Logic 265 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter How) 346 INDXxCNTL (Index x Counter How) 346 INDXXHLD (Index x Counter How) 346 INDXXHLD (Index x Counter How) 346 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTREG (Interrupt Control and Status) 113 INTXTMRH (Interval x Timer High) 344 INTXTMRL (Interval x Timer Hold High) 345 INTXXHLDH (Interval x Timer Hold Low) 345 LATx (Output Data for PORTx) 120 LFSR (Linear Feedback Shift) 269 LOGCONy (Combinatorial PWM Logic Control y) 265 MBISTCON (MBIST Control) 49 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXxHLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTTREG (Interrupt Control 4)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Duty Cycle)261 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXxHLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTTREG (Interrupt Control and Status)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Duty Cycle)261MPER (Master Period)262 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXxHLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTTREG (Interrupt Control and Status)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Duty Cycle)261MPER (Master Period)262MPHASE (Master Phase)261 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXXHLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTTREG (Interrupt Control and Status)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Duty Cycle)261MPER (Master Period)262MPHASE (Master Phase)261NVMADR (Nonvolatile Memory Lower Address)86 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTREG (Interrupt Control 4) 112 INTTREG (Interrupt Control and Status) 113 INTXTMRH (Interval x Timer High) 344 INTXTMRL (Interval x Timer Hold High) 345 INTXHLDH (Interval x Timer Hold Low) 345 LATx (Output Data for PORTx) 120 LFSR (Linear Feedback Shift) 269 LOGCONy (Combinatorial PWM Logic 261 MPER (Master Duty Cycle) 261 MPER (Master Period) 262 MPHASE (Master Phase) 261 NVMADR (Nonvolatile Memory Lower Address) 86 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTTREG (Interrupt Control 4) 113 INTXTMRH (Interval x Timer High) 344 INTXTMRL (Interval x Timer Hold High) 345 INTXHLDH (Interval x Timer Hold Low) 345 INTXHLDL (Interval x Timer Hold Low) 345 LATx (Output Data for PORTx) 120 LFSR (Linear Feedback Shift) 269 LOGCONy (Combinatorial PWM Logic 261 MPER (Master Duty Cycle) 261 MPER (Master Period) 262 MPHASE (Master Phase) 261 NVMADR (Nonvolatile Memory Lower Address) 86 NVMCON (Nonvolatile Memory (NVM) Control) 84 |
| Current Source Control Low) 480 INDXxCNTH (Index x Counter High) 346 INDXxCNTL (Index x Counter Hold) 347 INTCON1 (Interrupt Control 1) 108 INTCON2 (Interrupt Control 2) 110 INTCON3 (Interrupt Control 3) 111 INTCON4 (Interrupt Control 4) 112 INTREG (Interrupt Control 4) 113 INTXTMRH (Interval x Timer High) 344 INTXTMRL (Interval x Timer Hold High) 345 INTXHLDH (Interval x Timer Hold Low) 345 LATx (Output Data for PORTx) 120 LFSR (Linear Feedback Shift) 269 LOGCONy (Combinatorial PWM Logic 261 MPER (Master Period) 262 MPHASE (Master Phase) 261 NVMADR (Nonvolatile Memory Lower Address) 86 NVMADRU (Nonvolatile Memory (NVM) Control) 84 NVMKEY (Nonvolatile Memory Key) 87 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control 4)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Duty Cycle)261MPER (Master Phase)261NVMADR (Nonvolatile Memory Lower Address)86NVMCON (Nonvolatile Memory (NVM) Control)84NVMSRCADR (NVM Source Data Address)87 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXxCNTL (Index x Counter Low)346INDXXLLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control and Status)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Duty Cycle)261MPER (Master Period)262MPHASE (Master Phase)261NVMADR (Nonvolatile Memory Lower Address)86NVMCON (Nonvolatile Memory (NVM) Control)84NVMSRCADR (NVM Source Data Address)87ODCx (Open-Drain Enable for PORTx)120 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter How)346INDXXCNTL (Index x Counter Low)346INDXXHLD (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTTREG (Interrupt Control and Status)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Hold High)345INTXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Duty Cycle)261MPER (Master Period)262MPHASE (Master Phase)261NVMADR (Nonvolatile Memory Lower Address)86NVMCON (Nonvolatile Memory (NVM) Control)84NVMSRCADR (NVM Source Data Address)87ODCx (Open-Drain Enable for PORTx)120OSCCON (Oscillator Control)189 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control 4)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Low)344INTXHLDH (Interval x Timer Hold High)345INTXXHLDL (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Period)262MPHASE (Master Phase)261NVMADR (Nonvolatile Memory Lower Address)86NVMCON (Nonvolatile Memory (NVM) Control)84NVMSRCADR (NVM Source Data Address)87ODCx (Open-Drain Enable for PORTx)120OSCCUN (FRC Oscillator Tuning)194 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control 4)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Low)344INTXTMRL (Interval x Timer Hold High)345INTXXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Period)262MPHASE (Master Phase)261NVMADR (Nonvolatile Memory Lower Address)86NVMCON (Nonvolatile Memory (NVM) Control)84NVMSRCADR (NVM Source Data Address)87ODCx (Open-Drain Enable for PORTx)120OSCCON (PWM Clock Control)259 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control 4)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Low)344INTXTMRL (Interval x Timer Hold High)345INTXXHLDH (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Period)262MPHASE (Master Phase)261NVMADRU (Nonvolatile Memory Lower Address)86NVMCON (Nonvolatile Memory Upper Address)86NVMKEY (Nonvolatile Memory Key)87NVMSRCADR (NVM Source Data Address)87ODCx (Open-Drain Enable for PORTx)120OSCCON (Oscillator Control)189OSCTUN (FRC Oscillator Tuning)194PCLKCON (PWM Clock Control)259PGxCAP (PWM Generator x Capture)289 |
| Current Source Control Low)480INDXxCNTH (Index x Counter High)346INDXxCNTL (Index x Counter Hold)347INTCON1 (Interrupt Control 1)108INTCON2 (Interrupt Control 2)110INTCON3 (Interrupt Control 3)111INTCON4 (Interrupt Control 4)112INTREG (Interrupt Control 4)113INTXTMRH (Interval x Timer High)344INTXTMRL (Interval x Timer Low)344INTXTMRL (Interval x Timer Hold High)345INTXHLDL (Interval x Timer Hold Low)345LATx (Output Data for PORTx)120LFSR (Linear Feedback Shift)269LOGCONy (Combinatorial PWM Logic Control y)265MBISTCON (MBIST Control)49MDC (Master Period)262MPHASE (Master Phase)261NVMADRU (Nonvolatile Memory Lower Address)86NVMCON (Nonvolatile Memory Upper Address)86NVMSRCADR (NVM Source Data Address)87ODCx (Open-Drain Enable for PORTx)120OSCCON (Oscillator Control)189OSCTUN (FRC Oscillator Tuning)194PCLKCON (PWM Clock Control)259PGxCONH (PWM Generator x Capture)289PGxCONH (PWM Generator x Control High)271 |

| PGxDC (PWM Generator x Duty Cycle) | 285 |
|--|---|
| Adjustment) | 000 |
| Aujustment) | 200 |
| PGXDTH (PVVM Generator x Dead-Time Hign) | 288 |
| PGxDTL (PWM Generator x Dead-Time Low) | 288 |
| PGxEVTH (PWM Generator x Event High) | 278 |
| PGxEVTL (PWM Generator x Event Low) | 277 |
| PGxIOCONH (PWM Generator x | |
| I/O Control High) | 276 |
| PGxIOCONI (PWM Generator x | |
| | 275 |
| Devi EDU (DWM Concreter v Looding Edge | 215 |
| POLEBR (PWW Generator x Leading-Edge | 004 |
| | 284 |
| PGxLEBL (PWM Generator x Leading-Edge | |
| Blanking Low) | 283 |
| PGxPER (PWM Generator x Period) | 286 |
| PGxPHASE (PWM Generator x Phase) | 285 |
| PGxSTAT (PWM Generator x Status) | 273 |
| PGxTRIGA (PWM Generator x Trigger A) | 287 |
| PCyTRICR (PWM Concreter x Trigger P) | 207 |
| POUTDIOC (DWM Cenerator v Trigger C) | 207 |
| | 201 |
| PGxyPCIH (PWM Generator xy PCI High) | 281 |
| PGxyPCIL (PWM Generator xy PCI Low) | 279 |
| PLLDIV (PLL Output Divider) | 195 |
| PLLFBD (PLL Feedback Divider) | 193 |
| PMADDR (PMP Address) | 407 |
| PMAEN (PMP Pin Enable) | 410 |
| PMCONI (PMP Control) | 102 |
| DMCONUL/DMD Control Lligh) | 402 |
| | 404 |
| PMD1 (PMD1 Control) | 496 |
| PMD2 (PMD2 Control) | 497 |
| PMD3 (PMD3 Control) | 498 |
| PMD4 (PMD4 Control) | 499 |
| PMD6 (PMD6 Control) | 500 |
| PMD7 (PMD7 Control) | 501 |
| PMD8 (PMD8 Control) | 502 |
| PMDIN1 (PMP Data Input/Output Low) | 409 |
| PMDIN2 (PMP Data Input/Output High) | 409 |
| PMDOLIT1 (PMP Data Output Low) | 100 |
| PMDOUTT (FMF Data Output Low) | 400 |
| | 400 |
| | 405 |
| PMRADDR (PMP Read Address) | 413 |
| PMRDIN (PMP Read Input Data) | 414 |
| PMSTAT (PMP Status) | 411 |
| PMWADDR (PMP Write Address) | 412 |
| PORTx (Input Data for PORTx) | |
| POSxCNTH (Position x Counter High) | 119 |
| POSyCNTL (Position & Counter Low) | 119 340 |
| | 119 340 |
| POSVELD (Position & Counter Hold) | 119 340 340 |
| POSxHLD (Position x Counter Hold) | 119 340 340 341 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) | 119 340 340 341 466 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) | 119 340 340 341 466 462 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger | 119 340 340 341 466 462 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) | 119 340 340 341 466 462 462 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) | 119 340 340 341 466 462 462 465 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) | 119 340 340 341 466 462 462 465 465 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) | 119 340 340 341 466 462 462 465 465 465 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) PTGCST (PTG Control/Status I ow) | 119 340 340 341 466 462 462 465 465 465 461 459 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGCHOLD (PTG Hold) | 119 340 340 341 466 462 462 465 465 465 461 459 463 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGCOLIM (PTG Counter 0 Limit) PTGCOLIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGHOLD (PTG Hold) | 119 340 340 341 466 462 465 465 465 465 461 459 463 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGCOLIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGL0 (PTG Literal 0) | 119 340 340 341 466 462 465 465 465 465 465 465 465 465 465 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC0LIM (PTG Counter 1 Limit) PTGC0N (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGL0 (PTG Literal 0) PTGQPTR (PTG Step Queue Pointer) PTGC0 F Control Control Control | 119 340 340 341 466 462 465 465 465 465 465 465 465 465 463 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGC0N (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGL0 (PTG Literal 0) PTGQUEn (PTG Step Queue n Pointer) PTGQUEn (PTG Step Queue n Pointer) | 119 340 340 341 466 462 465 465 465 465 465 465 465 465 466 467 467 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGL0 (PTG Literal 0) PTGQUER (PTG Step Queue Pointer) PTGQUEn (PTG Step Delay Limit) | 119 340 341 466 462 465 465 465 465 465 465 465 466 467 466 467 464 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGL0 (PTG Literal 0) PTGQUEn (PTG Step Queue Pointer) PTGSDLIM (PTG Step Delay Limit) PTGT0LIM (PTG Timer0 Limit) | 119 340 340 341 466 462 465 465 465 465 465 465 466 467 467 467 464 463 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGC0N (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGL0 (PTG Literal 0) PTGQUER (PTG Step Queue Pointer) PTGQUEn (PTG Step Delay Limit) PTGT0LIM (PTG Timer0 Limit) PTGT1LIM (PTG Timer1 Limit) | 119 340 340 341 466 462 465 465 465 465 465 465 465 466 467 467 464 463 464 |
| POSxHLD (Position x Counter Hold) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable Low) PTGBTEH (PTG Broadcast Trigger Enable High) PTGC0LIM (PTG Counter 0 Limit) PTGC1LIM (PTG Counter 1 Limit) PTGCON (PTG Control/Status High) PTGCST (PTG Control/Status Low) PTGHOLD (PTG Hold) PTGQUTR (PTG Step Queue Pointer) PTGQUEn (PTG Step Delay Limit) PTGT0LIM (PTG Timer0 Limit) PTGT1LIM (PTG Timer1 Limit) | 119 340 341 466 462 462 465 465 465 465 465 465 465 466 467 466 467 466 467 464 463 464 267 |

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| Microchip Tradema Architecture — Flash Memory Fam Program Memory S Product Group — Pin Count — Tape and Reel Flag Temperature Range Package Pattern | dsPIC 33 CK 64 MP 508 T 1 / PT - XXX rk ily ize (Kbyte) (if applicable) | Examples: dsPIC33CK256MP506-I/PT: dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, SMPS, 64-Pin, Industrial Temperature, TQFP Package. | | | | |
|--|--|--|--|--|--|--|
| Architecture: | 33 = 16-Bit Digital Signal Controller | | | | | |
| Product Group: | MP = Motor Control/Power Supply | | | | | |
| Pin Count: | 02 = 28-pin 03 = 36-pin 04 = 48-pin 06 = 64-pin 08 = 80-pin | | | | | |
| Temperature Range: | $ \begin{array}{rcl} & = & -40^{\circ}\text{C to } +85^{\circ}\text{C (Industrial)} \\ \text{E} & = & -40^{\circ}\text{C to } +125^{\circ}\text{C (Extended)} \end{array} $ | | | | | |
| Package: | ackage:SS = Plastic Shrink Small Outline - (28-pin) 5.30 mm body (SSOP) 2N = Ultra Thin Plastic Quad Flat, No Lead - (28-pin) 6x6 mm body (UQFN) M5 = Ultra Thin Plastic Quad Flat, No Lead - (36-pin) 5x5 mm body (UQFN) PT = Thin Quad Flatpack - (48-pin) 7x7 mm body (TQFP) PT = Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) MR = Plastic Quad Flat, No Lead - (64-pin) 9x9 mm body (QFN) PT = Plastic Thin Quad Flatpack - (80-pin) 12x12 mm body (TQFP) | | | | | |