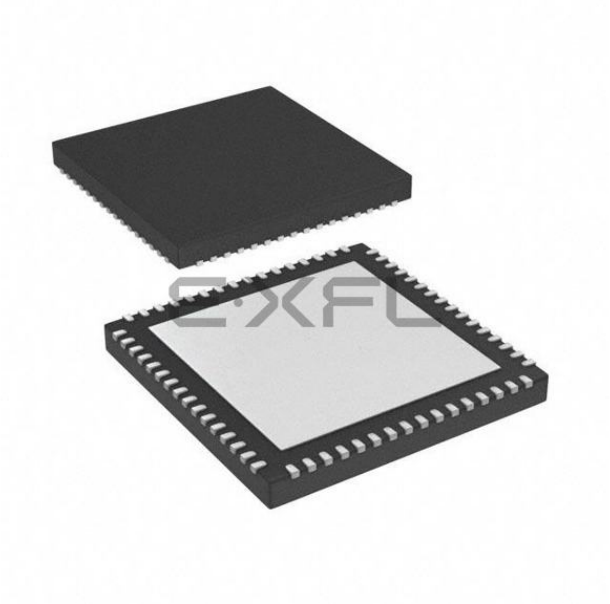

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What is "Embedded - Microcontrollers"?

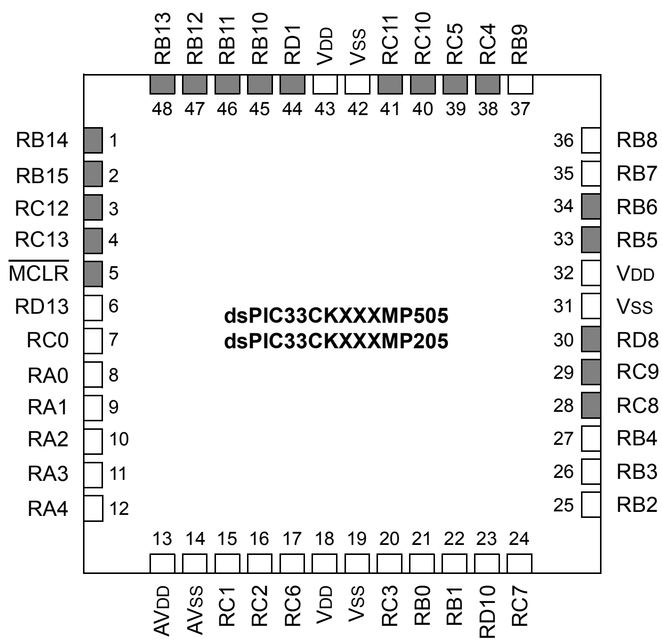
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck256mp506-i-mr

Pin Diagrams (Continued)

48-Pin TQFP, UQFN



Note: Shaded pins are up to 5 VDC tolerant.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name[(1)]	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	Yes	UART2 Clear-to-Send
U2RTS	O	—	Yes	UART2 Request-to-Send
U2RX	I	ST	Yes	UART2 receive
U2TX	O	—	Yes	UART2 transmit
U2DSR	I	ST	Yes	UART2 Data-Set-Ready
U2DTR	O	—	Yes	UART2 Data-Terminal-Ready
U3CTS	I	ST	Yes	UART3 Clear-to-Send
U3RTS	O	—	Yes	UART3 Request-to-Send
U3RX	I	ST	Yes	UART3 receive
U3TX	O	—	Yes	UART3 transmit
U3DSR	I	ST	Yes	UART3 Data-Set-Ready
U3DTR	O	—	Yes	UART3 Data-Terminal-Ready
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1
SDI1	I	ST	Yes	SPI1 data in
SDO1	O	—	Yes	SPI1 data out
SS1	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O
SCK2	I/O	ST	Yes[(3)]	Synchronous serial clock input/output for SPI2
SDI2	I	ST	Yes[(3)]	SPI2 data in
SDO2	O	—	Yes[(3)]	SPI2 data out
SS2	I/O	ST	Yes[(3)]	SPI2 slave synchronization or frame pulse I/O
SCK3	I/O	ST	Yes	Synchronous serial clock input/output for SPI3
SDI3	I	ST	Yes	SPI3 data in
SDO3	O	—	Yes	SPI3 data out
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2
SCL3	I/O	ST	No	Synchronous serial clock input/output for I2C3
SDA3	I/O	ST	No	Synchronous serial data input/output for I2C3
ASCL3	I/O	ST	No	Alternate synchronous serial clock input/output for I2C3
ASDA3	I/O	ST	No	Alternate synchronous serial data input/output for I2C3
QEIA1-QEIA2	I	ST	Yes	QEI Inputs A1 and A2
QEIB1-QEIB2	I	ST	Yes	QEI Inputs B1 and B2
QEINDX1-QEINDX2	I	ST	Yes	QEI Index Inputs 1 and 2
QEIHOM1-QEIHOM2	I	ST	Yes	QEI Home Inputs 1 and 2
QEICMP1-QEICMP2	O	—	Yes	QEI Comparator Outputs 1 and 2
SENT1-SENT2	I	ST	Yes	SENT1 and SENT2 inputs
SENT1OUT-SENT2OUT	O	—	Yes	SENT1 and SENT2 outputs

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer; DIG = Digital

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.
2: PWM4L and PWM4H pins are available on PPS as well as dedicated.
3: SPI2 supports dedicated pins as well as PPS on 48, 64 and 80-pin devices.

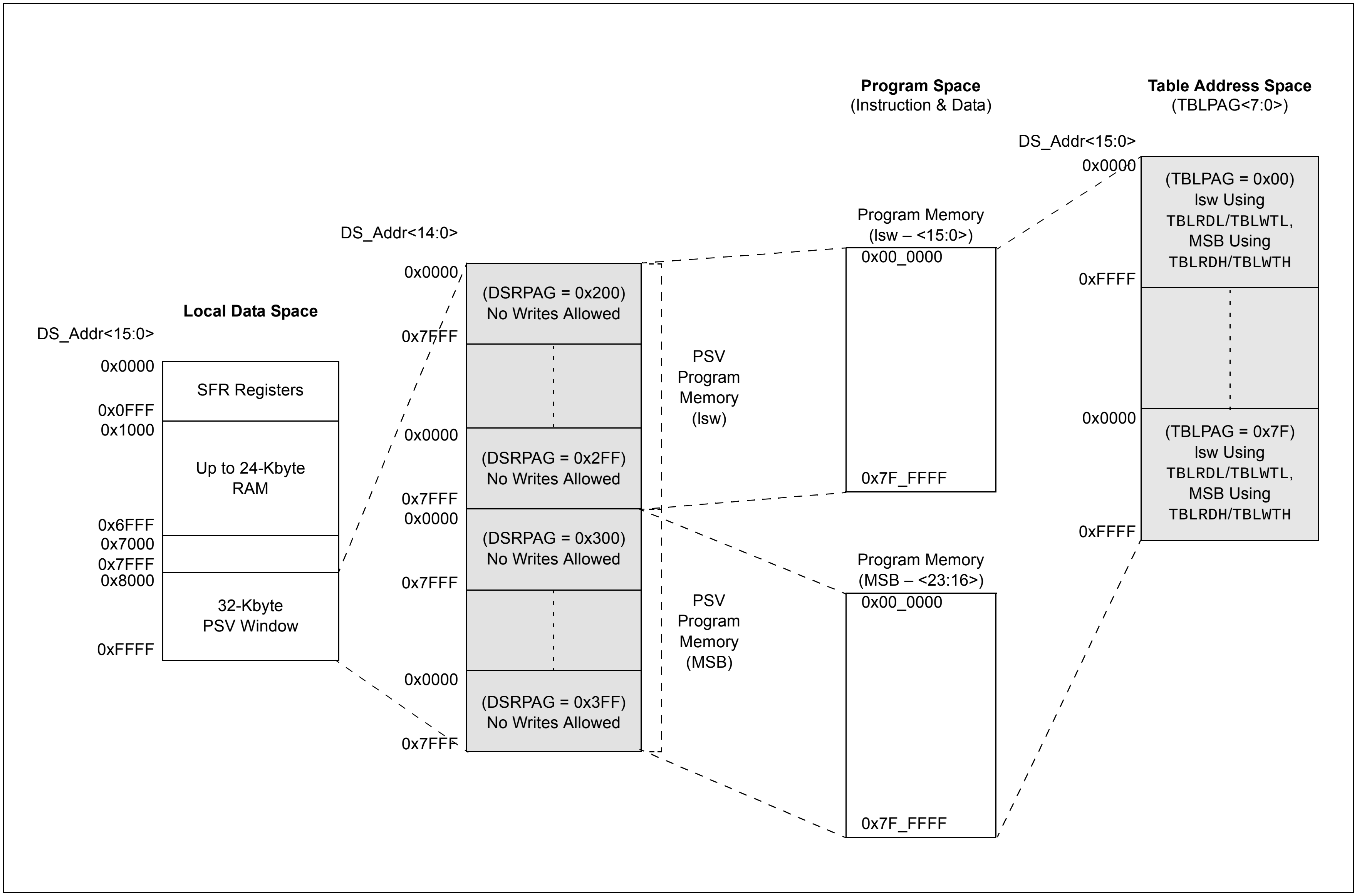
TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name[(1)]	Pin Type	Buffer Type	PPS	Description
PGD1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1
PGC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1
PGD2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2
PGC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2
PGD3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3
PGC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AV_{DD}	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AV_{SS}	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
V_{DD}	P	—	No	Positive supply for peripheral logic and I/O pins
V_{SS}	P	—	No	Ground reference for logic and I/O pins

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer; DIG = Digital

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.
2: PWM4L and PWM4H pins are available on PPS as well as dedicated.
3: SPI2 supports dedicated pins as well as PPS on 48, 64 and 80-pin devices.

FIGURE 4-12: PAGED DATA MEMORY SPACE



REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY<7:0>:** NVM Key Register bits (write-only)

REGISTER 5-5: NVMSRCADR: NVM SOURCE DATA ADDRESS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMSRCADR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMSRCADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **NVMSRCADR<15:0>:** NVM Source Data Address bits

The RAM address of the data to be programmed into Flash when the NVMOP<3:0> bits are set to row programming.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

8.5.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

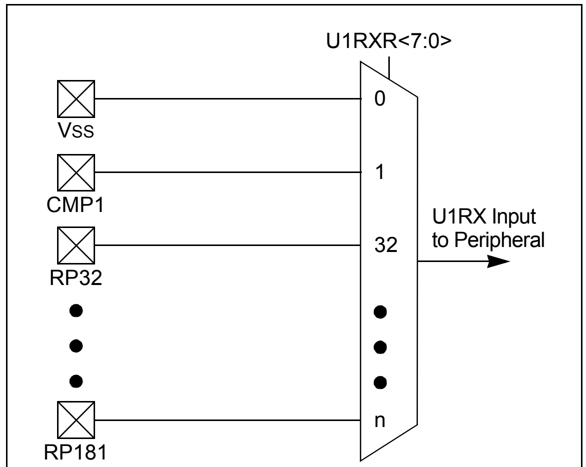
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

8.5.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping. Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit index value maps the RPn pin with the corresponding value, or internal signal, to that peripheral. See Table 8-4 for a list of available inputs.

For example, Figure 8-2 illustrates remappable pin selection for the U1RX input.

FIGURE 8-2: REMAPPABLE INPUT FOR U1RX



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1'). Physical connection to a pin can be made through RP32 through RP71. There are internal signals and virtual pins that can be connected to an input. Table 8-4 shows the details of the input assignment.

8.5.8 I/O HELPFUL TIPS

1. In some cases, certain pins, as defined in Table 33-15 under “Injection Current”, have internal protection diodes to V_{DD} and V_{SS}. The term, “Injection Current”, is also referred to as “Clamp Current”. On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or lesser than the data sheet absolute maximum ratings, with respect to the V_{SS} and V_{DD} supplies. Note that when the user application forward biases either of the high or low-side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the V_{DD} and V_{SS} power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins, by default, after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a ‘`0`’, regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Select for PORTx registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a ‘`0`’.

Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = `0x0`, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name, from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1; this indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(V_{DD} – 0.8), not V_{DD}. This value is still above the minimum V_{IH} of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the V_{OH}/I_{OH} and V_{OL}/I_{OL} DC characteristics specification. The respective I_{OH} and I_{OL} current rating only applies to maintaining the corresponding output at or above the V_{OH}, and at or below the V_{OL} levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum V_{IH}/V_{IL} levels. An I/O pin output can safely sink or source any current less than that listed in the Absolute Maximum Ratings in **Section 33.0 “Electrical Characteristics”** of this data sheet. For example:

   V_{OH} = 2.4v @ I_{OH} = -8 mA and V_{DD} = 3.3V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current < 12 mA is technically permitted. Refer to the V_{OH}/I_{OH} graphs in **Section 34.0 “DC and AC Device Characteristics Graphs”** for additional information.

REGISTER 8-66: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-8	**RP57R<5:0>:** Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 8-7 for peripheral function numbers)
bit 7-6	**Unimplemented:** Read as ‘0’
bit 5-0	**RP56R<5:0>:** Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 8-7 for peripheral function numbers)

REGISTER 8-67: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP59R5	RP59R4	RP59R3	RP59R2	RP59R1	RP59R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP58R5	RP58R4	RP58R3	RP58R2	RP58R1	RP58R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-8	**RP59R<5:0>:** Peripheral Output Function is Assigned to RP59 Output Pin bits (see Table 8-7 for peripheral function numbers)
bit 7-6	**Unimplemented:** Read as ‘0’
bit 5-0	**RP58R<5:0>:** Peripheral Output Function is Assigned to RP58 Output Pin bits (see Table 8-7 for peripheral function numbers)

REGISTER 12-2: FSCL: FREQUENCY SCALE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **FSCL<15:0>:** Frequency Scale Register bits
The value in this register is added to the frequency scaling accumulator at each pwm_master_clk. When the accumulated value exceeds the value of FSMINPER, a clock pulse is produced.

REGISTER 12-3: FSMINPER: FREQUENCY SCALING MINIMUM PERIOD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **FSMINPER<15:0>:** Frequency Scaling Minimum Period Register bits
This register holds the minimum clock period (maximum clock frequency) that can be produced by the frequency scaling circuit.

REGISTER 13-3: ADCON2L: ADC CONTROL REGISTER 2 LOW

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
REFCIE	REFERCIE	—	EIEN	—	SHREISEL2(1)	SHREISEL1(1)	SHREISEL0(1)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SHRADCS6	SHRADCS5	SHRADCS4	SHRADCS3	SHRADCS2	SHRADCS1	SHRADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **REFCIE:** Band Gap and Reference Voltage Ready Common Interrupt Enable bit
1 = Common interrupt will be generated when the band gap will become ready
0 = Common interrupt is disabled for the band gap ready event

bit 14 **REFERCIE:** Band Gap or Reference Voltage Error Common Interrupt Enable bit
1 = Common interrupt will be generated when a band gap or reference voltage error is detected
0 = Common interrupt is disabled for the band gap and reference voltage error event

bit 13 **Unimplemented:** Read as ‘0’

bit 12 **EIEN:** Early Interrupts Enable bit
1 = The early interrupt feature is enabled for the input channel interrupts (when the EISTATx flag is set)
0 = The individual interrupts are generated when conversion is done (when the ANxRDY flag is set)

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **SHREISEL<2:0>:** Shared Core Early Interrupt Time Selection bits(1)
111 = Early interrupt is set and interrupt is generated 8 TADCORE clocks prior to when the data is ready
110 = Early interrupt is set and interrupt is generated 7 TADCORE clocks prior to when the data is ready
101 = Early interrupt is set and interrupt is generated 6 TADCORE clocks prior to when the data is ready
100 = Early interrupt is set and interrupt is generated 5 TADCORE clocks prior to when the data is ready
011 = Early interrupt is set and interrupt is generated 4 TADCORE clocks prior to when the data is ready
010 = Early interrupt is set and interrupt is generated 3 TADCORE clocks prior to when the data is ready
001 = Early interrupt is set and interrupt is generated 2 TADCORE clocks prior to when the data is ready
000 = Early interrupt is set and interrupt is generated 1 TADCORE clock prior to when the data is ready

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **SHRADCS<6:0>:** Shared ADC Core Input Clock Divider bits
These bits determine the number of TCORESRC (Source Clock Periods) for one shared TADCORE (Core Clock Period).
1111111 = 254 Source Clock Periods
...
0000011 = 6 Source Clock Periods
0000010 = 4 Source Clock Periods
0000001 = 2 Source Clock Periods
0000000 = 2 Source Clock Periods

Note 1: For the 6-bit shared ADC core resolution (SHRRES<1:0> = 00), the SHREISEL<2:0> settings, from ‘100’ to ‘111’, are not valid and should not be used. For the 8-bit shared ADC core resolution (SHRRES<1:0> = 01), the SHREISEL<2:0> settings, ‘110’ and ‘111’, are not valid and should not be used.

REGISTER 13-31: ADFLxCON: ADC DIGITAL FILTER x CONTROL REGISTER (x = 0, 1, 2, 3) (CONTINUED)

bit 4-0	**FLCHSEL<4:0>:** Oversampling Filter Input Channel Selection bits `11111` = Reserved `...` `11010` = Reserved `11001` = Band gap, 1.2V (AN25) `11000` = Temperature sensor (AN24) `10111` = AN23 `...` `00011` = AN3 `00010` = AN2 `00001` = AN1 `00000` = AN0

REGISTER 16-14: UxRXCHK: UARTx RECEIVE CHECKSUM REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXCHK<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **RXCHK<7:0>:** Receive Checksum bits (calculated from RX words)

LIN Modes:
C0EN = 1: Sum of all received data + addition carries, including PID.
C0EN = 0: Sum of all received data + addition carries, excluding PID.

LIN Slave:
Cleared when Break is detected.

LIN Master/Slave:
Cleared when Break is detected.

Other Modes:
C0EN = 1: Sum of every byte received + addition carries.
C0EN = 0: Value remains unchanged.

22.4 Input Capture Mode

Input Capture mode is used to capture a timer value from an independent timer base, upon an event, on an input pin or other internal trigger source. The input capture features are useful in applications requiring frequency (time period) and pulse measurement. Figure 22-6 depicts a simplified block diagram of Input Capture mode.

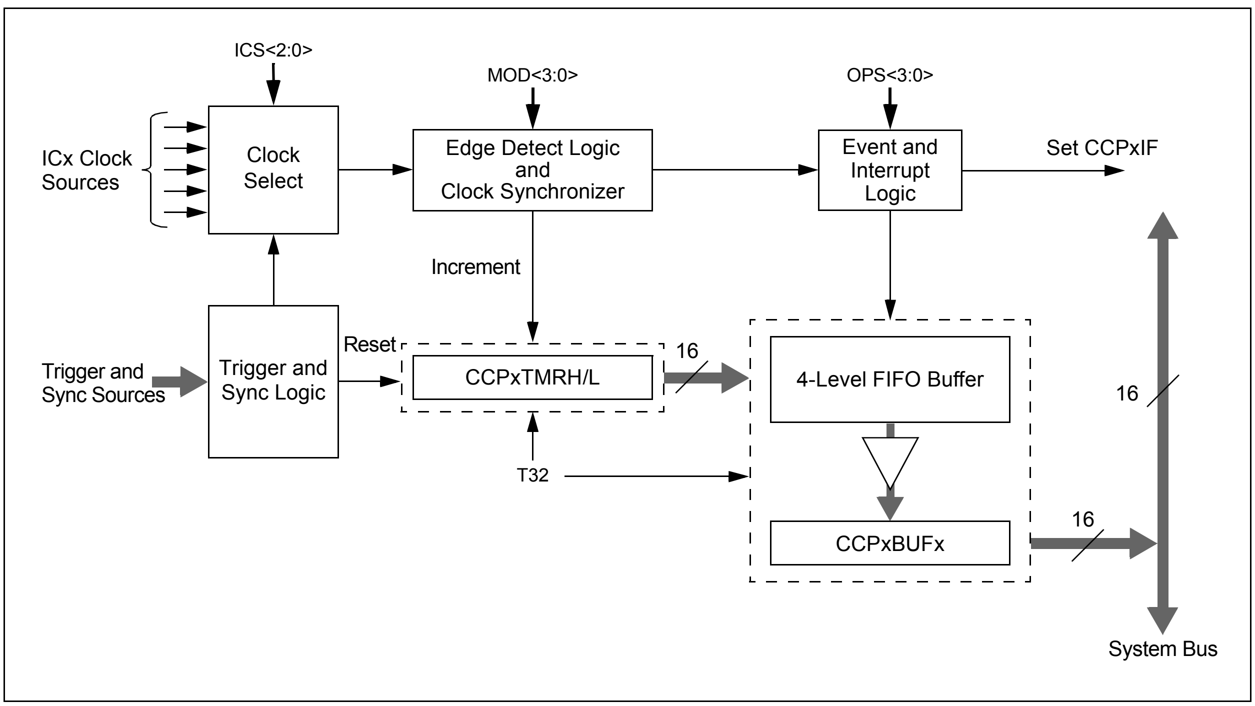
Input Capture mode uses a dedicated 16/32-bit, synchronous, up counting timer for the capture function. The timer value is written to the FIFO when a capture event occurs. The internal value may be read (with a synchronization delay) using the CCPxTMRH/L register.

To use Input Capture mode, the CCSEL bit (CCPxCON1L<4>) must be set. The T32 and the MOD<3:0> bits are used to select the proper Capture mode, as shown in Table 22-3.

TABLE 22-3: INPUT CAPTURE x MODES

MOD<3:0> (CCPxCON1L<3:0>)	T32 (CCPxCON1L<5>)	Operating Mode
0000	0	Edge Detect (16-bit capture)
0000	1	Edge Detect (32-bit capture)
0001	0	Every Rising (16-bit capture)
0001	1	Every Rising (32-bit capture)
0010	0	Every Falling (16-bit capture)
0010	1	Every Falling (32-bit capture)
0011	0	Every Rising/Falling (16-bit capture)
0011	1	Every Rising/Falling (32-bit capture)
0100	0	Every 4th Rising (16-bit capture)
0100	1	Every 4th Rising (32-bit capture)
0101	0	Every 16th Rising (16-bit capture)
0101	1	Every 16th Rising (32-bit capture)

FIGURE 22-6: INPUT CAPTURE x BLOCK DIAGRAM



REGISTER 23-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

bit 3	**G1D2T:** Gate 1 Data Source 2 True Enable bit 1 = Data Source 2 signal is enabled for Gate 1 0 = Data Source 2 signal is disabled for Gate 1
bit 2	**G1D2N:** Gate 1 Data Source 2 Negated Enable bit 1 = Data Source 2 inverted signal is enabled for Gate 1 0 = Data Source 2 inverted signal is disabled for Gate 1
bit 1	**G1D1T:** Gate 1 Data Source 1 True Enable bit 1 = Data Source 1 signal is enabled for Gate 1 0 = Data Source 1 signal is disabled for Gate 1
bit 0	**G1D1N:** Gate 1 Data Source 1 Negated Enable bit 1 = Data Source 1 inverted signal is enabled for Gate 1 0 = Data Source 1 inverted signal is disabled for Gate 1

REGISTER 28-7: DMTPSCNTL: DMT POST-CONFIGURE COUNT STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT<15:0>:** Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

REGISTER 28-8: DMTPSCNTH: DMT POST-CONFIGURE COUNT STATUS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT<31:16>:** Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

REGISTER 30-6: FWDT CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FWDTEN	SWDTPS4	SWDTPS3	SWDTPS2	SWDTPS1	SWDTPS0	WDTWIN1	WDTWIN0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
WINDIS	RCLKSEL1	RCLKSEL0	RWDTPS4	RWDTPS3	RWDTPS2	RWDTPS1	RWDTPS0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as ‘1’

bit 15 **FWDTEN:** Watchdog Timer Enable bit
1 = WDT is enabled in hardware
0 = WDT controller via the ON bit (WDTCONL<15>)

bit 14-10 **SWDTPS<4:0>:** Sleep Mode Watchdog Timer Period Select bits
11111 = Divide by 2 ^ 30 = 1,073,741,824
11110 = Divide by 2 ^ 29 = 526,870,912
...
00001 = Divide by 2 ^ 2, 4
00000 = Divide by 2 ^ 1, 2

bit 9-8 **WDTWIN<1:0>:** Watchdog Timer Window Select bits
11 = WDT window is 25% of the WDT period
10 = WDT window is 37.5% of the WDT period
01 = WDT window is 50% of the WDT period
00 = WDT Window is 75% of the WDT period

bit 7 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in Non-Window mode
0 = Watchdog Timer is in Window mode

bit 6-5 **RCLKSEL<1:0>:** Watchdog Timer Clock Select bits
11 = LPRC clock
10 = Uses FRC when WINDIS = 0, system clock is not INTOSC/LPRC and device is not in Sleep; otherwise, uses INTOSC/LPRC
01 = Uses peripheral clock when system clock is not INTOSC/LPRC and device is not in Sleep; otherwise, uses INTOSC/LPRC
00 = Reserved

bit 4-0 **RWDTPS<4:0>:** Run Mode Watchdog Timer Period Select bits
11111 = Divide by 2 ^ 30 = 1,073,741,824
11110 = Divide by 2 ^ 29 = 526,870,912
...
00001 = Divide by 2 ^ 2, 4
00000 = Divide by 2 ^ 1, 2

REGISTER 30-17: FBOOT CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	U-1	U-1	U-1	R/PO-1	R/PO-1
—	—	—	—	—	—	BTMODE<1:0>	
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as ‘1’

bit 1-0 **BTMODE<1:0>:** Device Partition Mode Configuration Status bits
11 = Single Partition mode
10 = Dual Partition mode
01 = Protected Dual Partition mode (Partition 1 is write-protected when inactive)
00 = Reserved; do not use

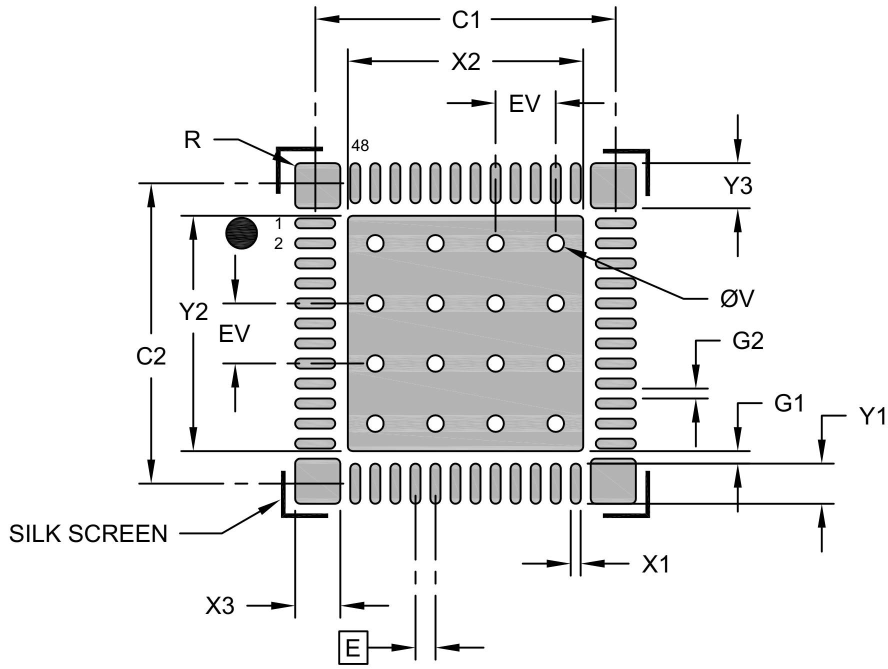
TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
89	`SL`	`SL`	`f`	f = Left Shift f	1	1	C,N,OV,Z
		`SL`	`f,WREG`	WREG = Left Shift f	1	1	C,N,OV,Z
		`SL`	`Ws,Wd`	Wd = Left Shift Ws	1	1	C,N,OV,Z
		`SL`	`Wb,Wns,Wnd`	Wnd = Left Shift Wb by Wns	1	1	N,Z
		`SL`	`Wb,#lit5,Wnd`	Wnd = Left Shift Wb by lit5	1	1	N,Z
91	`SUB`	`SUB`	`Acc`	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		`SUB`	`f`	f = f – WREG	1	1	C,DC,N,OV,Z
		`SUB`	`f,WREG`	WREG = f – WREG	1	1	C,DC,N,OV,Z
		`SUB`	`#lit10,Wn`	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		`SUB`	`Wb,Ws,Wd`	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		`SUB`	`Wb,#lit5,Wd`	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
92	`SUBB`	`SUBB`	`f`	f = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		`SUBB`	`f,WREG`	WREG = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		`SUBB`	`#lit10,Wn`	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		`SUBB`	`Wb,Ws,Wd`	Wd = Wb – Ws – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		`SUBB`	`Wb,#lit5,Wd`	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
93	`SUBR`	`SUBR`	`f`	f = WREG – f	1	1	C,DC,N,OV,Z
		`SUBR`	`f,WREG`	WREG = WREG – f	1	1	C,DC,N,OV,Z
		`SUBR`	`Wb,Ws,Wd`	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		`SUBR`	`Wb,#lit5,Wd`	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
94	`SUBBR`	`SUBBR`	`f`	f = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		`SUBBR`	`f,WREG`	WREG = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		`SUBBR`	`Wb,Ws,Wd`	Wd = Ws – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		`SUBBR`	`Wb,#lit5,Wd`	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
95	`SWAP`	`SWAP.b`	`Wn`	Wn = Nibble Swap Wn	1	1	None
		`SWAP`	`Wn`	Wn = Byte Swap Wn	1	1	None
96	`TBLRDH`	`TBLRDH`	`Ws,Wd`	Read Prog<23:16> to Wd<7:0>	1	5	None
97	`TBLRDL`	`TBLRDL`	`Ws,Wd`	Read Prog<15:0> to Wd	1	5	None
98	`TBLWTH`	`TBLWTH`	`Ws,Wd`	Write Ws<7:0> to Prog<23:16>	1	2	None
99	`TBLWTL`	`TBLWTL`	`Ws,Wd`	Write Ws to Prog<15:0>	1	2	None
101	`ULNK`	`ULNK`		Unlink Frame Pointer	1	1	SFA
104	`XOR`	`XOR`	`f`	f = f .XOR. WREG	1	1	N,Z
		`XOR`	`f,WREG`	WREG = f .XOR. WREG	1	1	N,Z
		`XOR`	`#lit10,Wn`	Wd = lit10 .XOR. Wd	1	1	N,Z
		`XOR`	`Wb,Ws,Wd`	Wd = Wb .XOR. Ws	1	1	N,Z
		`XOR`	`Wb,#lit5,Wd`	Wd = Wb .XOR. lit5	1	1	N,Z
105	`ZE`	`ZE`	`Ws,Wnd`	Wnd = Zero-Extend Ws	1	1	C,Z,N

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.
2: The divide instructions must be preceded with a “`REPEAT #5`” instruction, such that they are executed six consecutive times.

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			4.70
Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X48)	X1			0.20
Contact Pad Length (X48)	Y1			0.80
Corner Anchor Pad Width (X4)	X3			0.90
Corner Anchor Pad Length (X4)	Y3			0.90
Pad Corner Radius (X 20)	R			0.10
Contact Pad to Center Pad (X48)	G1	0.25		
Contact Pad to Contact Pad	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2442A-M4

