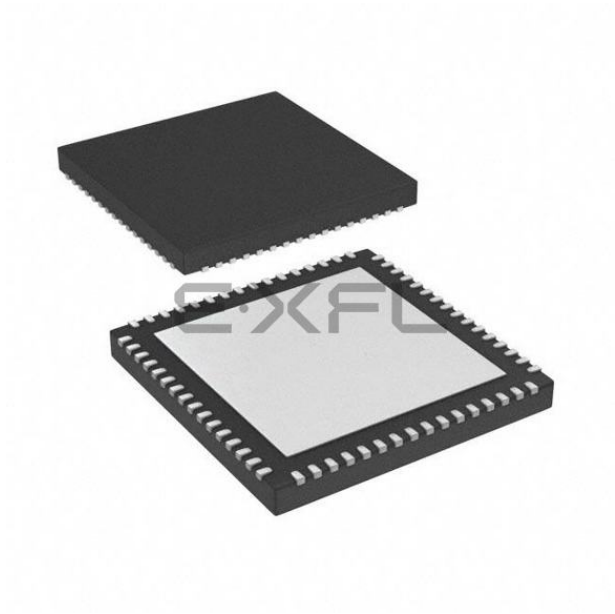
Microchip Technology - DSPIC33CK256MP506T-I/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck256mp506t-i-mr

TABLE 4-10: SFR BLOCK 900h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
PTG			CCP1CON3H	95A	0000------0-00--	CCP3PRL	9AC	1111111111111111
PTGCST	900	--00-00000x---00	CCP1STATL	95C	-----0--00xx0000	CCP3PRH	9AE	1111111111111111
PTGCON	902	000000000000-000	CCP1STATH	95E	----------00000	CCP3RAL	9B0	0000000000000000
PTGBTE	904	xxxxxxxxxxxxxxxx	CCP1TMRL	960	0000000000000000	CCP3RBL	9B4	0000000000000000
PTGBTEH	906	0000000000000000	CCP1TMRH	962	0000000000000000	CCP3BUFL	9B8	0000000000000000
PTGHOLD	908	0000000000000000	CCP1PRL	964	1111111111111111	CCP3BUFH	9BA	0000000000000000
PTGT0LIM	90C	0000000000000000	CCP1PRH	966	1111111111111111	CCP4CON1L	9BC	--00000000000000
PTGT1LIM	910	0000000000000000	CCP1RAL	968	0000000000000000	CCP4CON1H	9BE	00--000000000000
PTGSDLIM	914	0000000000000000	CCP1RBL	96C	0000000000000000	CCP4CON2L	9C0	00-0----00000000
PTGC0LIM	918	0000000000000000	CCP1BUFL	970	0000000000000000	CCP4CON2H	9C2	-------100-00000
PTGC1LIM	91C	0000000000000000	CCP1BUFH	972	0000000000000000	CCP4CON3H	9C6	0000------0-00--
PTGADJ	920	0000000000000000	CCP2CON1L	974	--00000000000000	CCP4STATL	9C8	-----0--00xx0000
PTGL0	924	0000000000000000	CCP2CON1H	976	00--000000000000	CCP4STATH	9CA	----------00000
PTGQPTR	928	----------00000	CCP2CON2L	978	00-0----00000000	CCP4TMRL	9CC	0000000000000000
PTGQUE0	930	xxxxxxxxxxxxxxxx	CCP2CON2H	97A	0------100-00000	CCP4TMRH	9CE	0000000000000000
PTGQUE1	932	xxxxxxxxxxxxxxxx	CCP2CON3H	97E	0000------0-00--	CCP4PRL	9D0	1111111111111111
PTGQUE2	934	xxxxxxxxxxxxxxxx	CCP2STATL	980	-----0--00xx0000	CCP4PRH	9D2	1111111111111111
PTGQUE3	936	xxxxxxxxxxxxxxxx	CCP2STATH	982	----------00000	CCP4RAL	9D4	0000000000000000
PTGQUE4	938	xxxxxxxxxxxxxxxx	CCP2TMRL	984	0000000000000000	CCP4RBL	9D8	0000000000000000
PTGQUE5	93A	xxxxxxxxxxxxxxxx	CCP2TMRH	986	0000000000000000	CCP4BUFL	9DC	0000000000000000
PTGQUE6	93C	xxxxxxxxxxxxxxxx	CCP2PRL	988	1111111111111111	CCP4BUFH	9DE	0000000000000000
PTGQUE7	93E	xxxxxxxxxxxxxxxx	CCP2PRH	98A	1111111111111111	CCP5CON1L	9E0	--00000000000000
PTGQUE8	940	xxxxxxxxxxxxxxxx	CCP2RAL	98C	0000000000000000	CCP5CON1H	9E2	00--000000000000
PTGQUE9	942	xxxxxxxxxxxxxxxx	CCP2RBL	990	0000000000000000	CCP5CON2L	9E4	00-0----00000000
PTGQUE10	944	xxxxxxxxxxxxxxxx	CCP2BUFL	994	0000000000000000	CCP5CON2H	9E6	-------100-00000
PTGQUE11	946	xxxxxxxxxxxxxxxx	CCP2BUFH	996	0000000000000000	CCP5CON3H	9EA	0000------0-00--
PTGQUE12	948	xxxxxxxxxxxxxxxx	CCP3CON1L	998	--00000000000000	CCP5STATL	9EC	-----0--00xx0000
PTGQUE13	94A	xxxxxxxxxxxxxxxx	CCP3CON1H	99A	00--000000000000	CCP5STATH	9EE	----------00000
PTGQUE14	94C	xxxxxxxxxxxxxxxx	CCP3CON2L	99C	00-0----00000000	CCP5TMRL	9F0	0000000000000000
PTGQUE15	94E	xxxxxxxxxxxxxxxx	CCP3CON2H	99E	-------100-00000	CCP5TMRH	9F2	0000000000000000
CCP			CCP3CON3H	9A2	0000------0-00--	CCP5PRL	9F4	1111111111111111
CCP1CON1L	950	--00000000000000	CCP3STATL	9A4	-----0--00xx0000	CCP5PRH	9F6	1111111111111111
CCP1CON1H	952	00--000000000000	CCP3STATH	9A6	----------00000	CCP5RAL	9F8	0000000000000000
CCP1CON2L	954	00-0----00000000	CCP3TMRL	9A8	0000000000000000	CCP5RBL	9FC	0000000000000000
CCP1CON2H	956	-------100-00000	CCP3TMRH	9AA	0000000000000000			

Legend: x = unknown or indeterminate value; "-" = unimplemented bits. Address values are in hexadecimal. Reset values are in binary.

4.4.5 INTERFACING PROGRAM AND DATA MEMORY SPACES

The dsPIC33CK256MP508 family architecture uses a 24-bit wide Program Space (PS) and a 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33CK256MP508 family devices provides two methods by which Program Space can be accessed during operation:

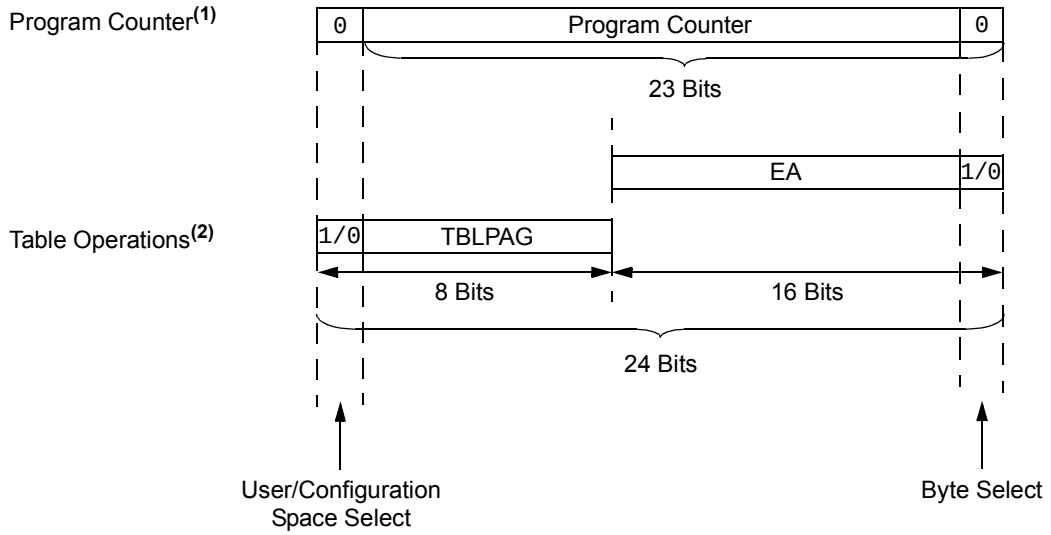
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-20: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xxx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		

FIGURE 4-16: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

5.4 ICSP™ Write Inhibit

ICSP Write Inhibit is an access restriction feature that, when activated, restricts all of Flash memory. Once activated, ICSP Write Inhibit permanently prevents ICSP Flash programming and erase operations, and cannot be deactivated. This feature is intended to prevent alteration of Flash memory contents, with behavior similar to One-Time-Programmable (OTP) devices.

RTSP, including erase and programming operations, is not restricted when ICSP Write Inhibit is activated; however, code to perform these actions must be programmed into the device before ICSP Write Inhibit is activated. This allows for a bootloader-type application to alter Flash contents with ICSP Write Inhibit activated.

Entry into ICSP and Enhanced ICSP modes is not affected by ICSP Write Inhibit. In these modes, it will continue to be possible to read configuration memory space and any user memory space regions which are not code protected. With ICSP writes inhibited, an attempt to set WR (NVMCON<15>) = 1 will maintain WR = 0, and instead, set WRERR (NVMCON<13>) = 1. All Enhanced ICSP erase and programming commands will have no effect with self-checked programming commands returning a FAIL response opcode (PASS if the destination already exactly matched the requested programming data).

Once ICSP Write Inhibit is activated, it is not possible for a device executing in Debug mode to erase/write Flash, nor can a debug tool switch the device to Production mode. ICSP Write Inhibit should therefore only be activated on devices programmed for production.

The JTAG port, when enabled, can be used to map ICSP signals to JTAG I/O pins. All Flash erase/programming operations initiated via the JTAG port will therefore also be blocked after activating ICSP Write Inhibit.

5.4.1 ACTIVATING ICSP™ WRITE INHIBIT

Caution: It is not possible to deactivate ICSP Write Inhibit.

ICSP Write Inhibit is activated by executing a pair of NVMCON double-word programming commands to save two 16-bit activation values in the configuration memory space. The target NVM addresses and values required for activation are shown in Table 5-1. Once both addresses contain their activation values, ICSP Write Inhibit will take permanent effect on the next device Reset. Neither address can be reset, erased or otherwise modified, through any means, after being successfully programmed, even if one of the addresses has not been programmed.

Only the lower 16 data bits stored at the activation addresses are evaluated; the upper 8 bits and second 24-bit word written by the double-word programming (NVMOP<3:0>) should be written as '0's. The addresses can be programmed in any order and also during separate ICSP/Enhanced ICSP/RTSP sessions, but any attempt to program an incorrect 16-bit value or use a row programming operation to program the values will be aborted without altering the existing data.

TABLE 5-1: ICSP™ WRITE INHIBIT ACTIVATION ADDRESSES AND DATA

	Configuration Memory Address	ICSP Write Inhibit Activation Value
Write Lock 1	0x801034	0x006D63
Write Lock 2	0x801038	0x006870

REGISTER 8-8: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
ON	—	—	—	CNSTYLE	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Change Notification (CN) Control for PORTx On bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CNSTYLE:** Change Notification Style Selection bit
1 = Edge style (detects edge transitions, CNFx<15:0> bits are used for a Change Notification event)
0 = Mismatch style (detects change from last port read, CNSTATx<15:0> bits are used for a Change Notification event)

bit 10-0 **Unimplemented:** Read as '0'

REGISTER 8-9: CNEN0x: INTERRUPT CHANGE NOTIFICATION ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNEN0x<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CNEN0x<15:0>:** Interrupt Change Notification Enable for PORTx bits
1 = Interrupt-on-change (from the last read value) is enabled for PORTx[n]
0 = Interrupt-on-change is disabled for PORTx[n]

TABLE 8-5: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)

Input Name(1)	Function Name	Register	Register Bits
SPI2 Clock Input	SCK2IN	RPINR22	SCK2R<7:0>
SPI2 Slave Select	$\overline{SS2}$	RPINR23	SS2R<7:0>
CAN1 Input	CAN1RX	RPINR26	CAN1RXR<7:0>
UART3 Receive	U3RX	RPINR27	U3RXR<7:0>
UART3 Data-Set-Ready	$\overline{U3DSR}$	RPINR27	U3DSRR<7:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<7:0>
SPI3 Clock Input	SCK3IN	RPINR29	SCK3R<7:0>
SPI3 Slave Select	$\overline{SS3}$	RPINR30	SS3R<7:0>
MCCP Timer9	TCKI9	RPINR32	TCKI9R<7:0>
MCCP Capture 9	ICM9	RPINR33	ICM9R<7:0>
xCCP Fault C	OCFC	RPINR37	OCFCR<7:0>
PWM Input 17	PCI17	RPINR37	PCI17R<7:0>
PWM Input 18	PCI18	RPINR38	PCI18R<7:0>
PWM Input 12	PCI12	RPINR42	PCI12R<7:0>
PWM Input 13	PCI13	RPINR42	PCI13R<7:0>
PWM Input 14	PCI14	RPINR43	PCI14R<7:0>
PWM Input 15	PCI15	RPINR43	PCI15R<7:0>
PWM Input 16	PCI16	RPINR44	PCI16R<7:0>
SENT1 Input	SENT1	RPINR44	SENT1R<7:0>
SENT2 Input	SENT2	RPINR45	SENT2R<7:0>
CLC Input A	CLCINA	RPINR45	CLCINAR<7:0>
CLC Input B	CLCINB	RPINR46	CLCINBR<7:0>
CLC Input C	CLCINC	RPINR46	CLCINCR<7:0>
CLC Input D	CLCIND	RPINR47	CLCINDR<7:0>
ADC Trigger Input (ADTRIG31)	ADCTRG	RPINR47	ADCTRGR<7:0>
xCCP Fault D	OCFD	RPINR48	OCFDR<7:0>
UART1 Clear-to-Send	$\overline{U1CTS}$	RPINR48	U1CTSR<7:0>
UART2 Clear-to-Send	$\overline{U2CTS}$	RPINR49	U2CTSR<7:0>
UART3 Clear-to-Send	$\overline{U3CTS}$	RPINR49	U3CTSR<7:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

TABLE 8-7: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
$\overline{\text{U1RTS}}$	000010	RPn tied to UART1 Request-to-Send
U2TX	000011	RPn tied to UART2 Transmit
$\overline{\text{U2RTS}}$	000100	RPn tied to UART2 Request-to-Send
SDO1	000101	RPn tied to SPI1 Data Output
SCK1	000110	RPn tied to SPI1 Clock Output
$\overline{\text{SS1}}$	000111	RPn tied to SPI1 Slave Select
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{\text{SS2}}$	001010	RPn tied to SPI2 Slave Select
SDO3	001011	RPn tied to SPI3 Data Output
SCK3	001100	RPn tied to SPI3 Clock Output
$\overline{\text{SS3}}$	001101	RPn tied to SPI3 Slave Select
REFCLKO	001110	RPn tied to Reference Clock Output
OCM1	001111	RPn tied to SCCP1 Output
OCM2	010000	RPn tied to SCCP2 Output
OCM3	010001	RPn tied to SCCP3 Output
OCM4	010010	RPn tied to SCCP4 Output
OCM5	010011	RPn tied to SCCP5 Output
OCM6	010100	RPn tied to SCCP6 Output
CAN1	010101	RPn tied to CAN1 Output
CMP1	010111	RPn tied to Comparator 1 Output
CMP2	011000	RPn tied to Comparator 2 Output
CMP3	011001	RPn tied to Comparator 3 Output
U3TX	011011	RPn tied to UART3 Transmit
$\overline{\text{U3RTS}}$	011100	RPn tied to UART3 Request-to-Send
PWM4H	100010	RPn tied to PWM4H Output
PWM4L	100011	RPn tied to PWM4L Output
PWMEA	100100	RPn tied to PWM Event A Output
PWMEB	100101	RPn tied to PWM Event B Output
QEICMP1	100110	RPn tied to QEI1 Comparator Output
QEICMP2	100111	RPn tied to QEI2 Comparator Output
CLC1OUT	101000	RPn tied to CLC1 Output
CLC2OUT	101001	RPn tied to CLC2 Output
OCM7	101010	RPn tied to SCCP7 Output
OCM8	101011	RPn tied to SCCP8 Output
PWMEC	101100	RPn tied to PWM Event C Output
PWMED	101101	RPn tied to PWM Event D Output
PTGTRG24	101110	PTG Trigger Output 24
PTGTRG25	101111	PTG Trigger Output 25
SENT1OUT	110000	RPn tied to SENT1 Output
SENT2OUT	110001	RPn tied to SENT2 Output

REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2(1)	DOZE1(1)	DOZE0(1)	DOZEN(2,3)	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8

U-0	U-0	r-0	r-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	—	—	PLLPRE3(4)	PLLPRE2(4)	PLLPRE1(4)	PLLPRE0(4)
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit and the processor clock, and the peripheral clock ratio is set to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits(1)
111 = FP divided by 128
110 = FP divided by 64
101 = FP divided by 32
100 = FP divided by 16
011 = FP divided by 8 (default)
010 = FP divided by 4
001 = FP divided by 2
000 = FP divided by 1

bit 11 **DOZEN:** Doze Mode Enable bit(2,3)
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock and peripheral clock ratio is forced to 1:1

bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **Reserved:** Read as '0'

Note 1: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

2: This bit is cleared when the ROI bit is set and an interrupt occurs.

3: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

4: PLLPRE<3:0> may be updated while the PLL is operating, but the VCO may overshoot.

11.2 Can Control Registers

REGISTER 11-1: C1CONH: CAN CONTROL REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	S/HC-0	R/W-1	R/W-0	R/W-0
TXBWS3	TXBWS2	TXBWS1	TXBWS0	ABAT	REQOP2	REQOP1	REQOP0
bit 15							bit 8

R-1	R-0	R-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
OPMOD2	OPMOD1	OPMOD0	TXQEN(1)	STEF(1)	SERRLOM(1)	ESIGM(1)	RTXAT(1)
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **TXBWS<3:0>:** Transmit Bandwidth Sharing bits
1111-1100 = 4096
1011 = 2048
1010 = 1024
1001 = 512
1000 = 256
0111 = 128
0110 = 64
0101 = 32
0100 = 16
0011 = 8
0010 = 4
0001 = 2
0000 = No delay

bit 11 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Sets Restricted Operation mode
110 = Sets Normal CAN 2.0 mode; error frames on CAN FD frames
101 = Sets External Loopback mode
100 = Sets Configuration mode
011 = Sets Listen Only mode
010 = Sets Internal Loopback mode
001 = Sets Disable mode
000 = Sets Normal CAN FD mode; supports mixing of full CAN FD and classic CAN 2.0 frames

bit 7-5 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Restricted Operation mode
110 = Module is in Normal CAN 2.0 mode; error frames on CAN FD frames
101 = Module is in External Loopback mode
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Internal Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal CAN FD mode; supports mixing of full CAN FD and classic CAN 2.0 frames

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 11-48: C1BDIAG1H: CAN BUS DIAGNOSTICS REGISTER 1 HIGH

R/W-0	R/W-0	R/C-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR	—	DBIT1ERR	DBIT0ERR
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXBOERR	—	NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DLCMM:** DLC Mismatch bit
During a transmission or reception, the specified DLC is larger than the PLSIZE<2:0> of the FIFO element.

bit 14 **ESI:** ESI Flag of a Received CAN FD Message Set bit

bit 13 **DCRCERR:** Same as for nominal bit rate

bit 12 **DSTUFERR:** Same as for nominal bit rate

bit 11 **DFORMERR:** Same as for nominal bit rate

bit 10 **Unimplemented:** Read as '0'

bit 9 **DBIT1ERR:** Same as for nominal bit rate

bit 8 **DBIT0ERR:** Same as for nominal bit rate

bit 7 **TXBOERR:** Device Went to Bus Off bit (and auto-recovered)

bit 6 **Unimplemented:** Read as '0'

bit 5 **NCRCERR:** Received Message with CRC Incorrect Checksum bit
The CRC checksum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.

bit 4 **NSTUFERR:** Received Message with Illegal Sequence bit
More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.

bit 3 **NFORMERR:** Received Frame Fixed Format bit
A fixed format part of a received frame has the wrong format.

bit 2 **NACKERR:** Transmitted Message Not Acknowledged bit
Transmitted message was not acknowledged.

bit 1 **NBIT1ERR:** Transmitted Message Recessive Level bit
During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant.

bit 0 **NBIT0ERR:** Transmitted Message Dominant Level bit
During the transmission of a message (or Acknowledge bit, active error flag or overload flag), the device wanted to send a dominant level (data or identifier bit of logical value '0'), but the monitored bus value was recessive. During bus off recovery, this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the bus off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).

REGISTER 12-13: PGxCONH: PWM GENERATOR x CONTROL REGISTER HIGH (CONTINUED)

bit 6 **TRGMOD:** PWM Generator Trigger Mode Selection bit
1 = PWM Generator operates in Retriggerable mode
0 = PWM Generator operates in Single Trigger mode

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **SOCS<3:0>:** Start-of-Cycle Selection bits(1,2,3)
1111 = TRIG bit or PCI Sync function only (no hardware trigger source is selected)
1110-0101 = Reserved
0100 = Trigger output selected by PG4 or PG8 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0011 = Trigger output selected by PG3 or PG7 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0010 = Trigger output selected by PG2 or PG6 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0001 = Trigger output selected by PG1 or PG5 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0000 = Local EOC – PWM Generator is self-triggered

Note 1: The PCI selected Sync signal is always available to be OR'd with the selected SOC signal per the SOCS<3:0> bits if the PCI Sync function is enabled.

2: The source selected by the SOCS<3:0> bits MUST operate from the same clock source as the local PWM Generator. If not, the source must be routed through the PCI Sync logic so the trigger signal may be synchronized to the PWM Generator clock domain.

3: PWM Generators are grouped into groups of four: PG1-PG4 and PG5-PG8, if available. Any generator within a group of four may be used to trigger another generator within the same group.

REGISTER 13-25: ADSTATL: ADC DATA READY STATUS REGISTER LOW

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
AN<15:8>RDY							
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
AN<7:0>RDY							
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **AN<15:0>RDY:** Common Interrupt Enable for Corresponding Analog Inputs bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

REGISTER 13-26: ADSTATH: ADC DATA READY STATUS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
—	—	—	—	—	—	AN<25:24>RDY	
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
AN<23:16>RDY							
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AN<25:16>RDY:** Common Interrupt Enable for Corresponding Analog Inputs bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

REGISTER 17-2: SPIxCON1H: SPIx CONTROL REGISTER 1 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AUDEN(1)	SPISGNEXT	IGNROV	IGNTUR	AUDMONO(2)	URDTEN(3)	AUDMOD1(4)	AUDMOD0(4)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT2	FRMCNT1	FRMCNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AUDEN:** Audio Codec Support Enable bit(1)
- 1 = Audio protocol is enabled; MSTEN controls the direction of both SCKx and frame (a.k.a. LRC), and this module functions as if FRMEN = 1, FRMSYNC = MSTEN, FRMCNT<2:0> = 001 and SMP = 0, regardless of their actual values
- 0 = Audio protocol is disabled

bit 14 **SPISGNEXT:** SPIx Sign-Extend RX FIFO Read Data Enable bit
- 1 = Data from RX FIFO is sign-extended
- 0 = Data from RX FIFO is not sign-extended

bit 13 **IGNROV:** Ignore Receive Overflow bit
- 1 = A Receive Overflow (ROV) is NOT a critical error; during ROV, data in the FIFO is not overwritten by the receive data
- 0 = A ROV is a critical error that stops SPI operation

bit 12 **IGNTUR:** Ignore Transmit Underrun bit
- 1 = A Transmit Underrun (TUR) is NOT a critical error and data indicated by URDTEN is transmitted until the SPIxTXB is not empty
- 0 = A TUR is a critical error that stops SPI operation

bit 11 **AUDMONO:** Audio Data Format Transmit bit(2)
- 1 = Audio data is mono (i.e., each data word is transmitted on both left and right channels)
- 0 = Audio data is stereo

bit 10 **URDTEN:** Transmit Underrun Data Enable bit(3)
- 1 = Transmits data out of SPIxURDT register during Transmit Underrun conditions
- 0 = Transmits the last received data during Transmit Underrun conditions

bit 9-8 **AUDMOD<1:0>:** Audio Protocol Mode Selection bits(4)
- 11 = PCM/DSP mode
- 10 = Right Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
- 01 = Left Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
- 00 = I^2S mode: This module functions as if SPIFE = 0, regardless of its actual value

bit 7 **FRMEN:** Framed SPIx Support bit
- 1 = Framed SPIx support is enabled ($\overline{SSx}$ pin is used as the FSYNC input/output)
- 0 = Framed SPIx support is disabled

Note 1: AUDEN can only be written when the SPIEN bit = 0.
2: AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3: URDTEN is only valid when IGNTUR = 1.
4: AUDMOD<1:0> can only be written when the SPIEN bit = 0 and is only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

NOTES:

REGISTER 26-2: IBIASCONH: CURRENT BIAS GENERATOR 50 µA CURRENT SOURCE CONTROL HIGH REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	SHRSRCEN3	SHRSNKEN3	GENSRCEN3	GENSNKEN3	SRCEN3	SNKEN3
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	SHRSRCEN2	SHRSNKEN2	GENSRCEN2	GENSNKEN2	SRCEN2	SNKEN2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **SHRSRCEN3:** Share Source Enable for Output #3 bit
1 = Sourcing Current Mirror mode is enabled (uses reference from another source)
0 = Sourcing Current Mirror mode is disabled

bit 12 **SHRSNKEN3:** Share Sink Enable for Output #3 bit
1 = Sinking Current Mirror mode is enabled (uses reference from another source)
0 = Sinking Current Mirror mode is disabled

bit 11 **GENSRCEN3:** Generated Source Enable for Output #3 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 10 **GENSNKEN3:** Generated Sink Enable for Output #3 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 9 **SRCEN3:** Source Enable for Output #3 bit
1 = Current source is enabled
0 = Current source is disabled

bit 8 **SNKEN3:** Sink Enable for Output #3 bit
1 = Current sink is enabled
0 = Current sink is disabled

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **SHRSRCEN2:** Share Source Enable for Output #2 bit
1 = Sourcing Current Mirror mode is enabled (uses reference from another source)
0 = Sourcing Current Mirror mode is disabled

bit 4 **SHRSNKEN2:** Share Sink Enable for Output #2 bit
1 = Sinking Current Mirror mode is enabled (uses reference from another source)
0 = Sinking Current Mirror mode is disabled

bit 3 **GENSRCEN2:** Generated Source Enable for Output #2 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 2 **GENSNKEN2:** Generated Sink Enable for Output #2 bit
1 = Source generates the current source mirror reference
0 = Source does not generate the current source mirror reference

bit 1 **SRCEN2:** Source Enable for Output #2 bit
1 = Current source is enabled
0 = Current source is disabled

bit 0 **SNKEN2:** Sink Enable for Output #2 bit
1 = Current sink is enabled
0 = Current sink is disabled

27.1 Operational Amplifier Control Registers

REGISTER 27-1: AMPCON1L: OP AMP CONTROL REGISTER LOW

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
AMPON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	AMPEN3	AMPEN2	AMPEN1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AMPON:** Op Amp Enable/On bit
1 = Enables op amp modules if their respective AMPENx bits are also asserted
0 = Disables all op amp modules

bit 14-3 **Unimplemented:** Read as '0'

bit 2 **AMPEN3:** Op Amp #3 Enable bit
1 = Enables Op Amp #3 if the AMPON bit is also asserted
0 = Disables Op Amp #3

bit 1 **AMPEN2:** Op Amp #2 Enable bit
1 = Enables Op Amp #2 if the AMPON bit is also asserted
0 = Disables Op Amp #2

bit 0 **AMPEN1:** Op Amp #1 Enable bit
1 = Enables Op Amp #1 if the AMPON bit is also asserted
0 = Disables Op Amp #1

REGISTER 30-15: FALTREG CONFIGURATION REGISTER (CONTINUED)

bit 2-0 **CTXT1<2:0>:** Specifies the Alternate Working Register Set #1 with Interrupt Priority Levels (IPL) bits
111 = Not assigned
110 = Alternate Register Set #1 is assigned to IPL Level 7
101 = Alternate Register Set #1 is assigned to IPL Level 6
100 = Alternate Register Set #1 is assigned to IPL Level 5
011 = Alternate Register Set #1 is assigned to IPL Level 4
010 = Alternate Register Set #1 is assigned to IPL Level 3
001 = Alternate Register Set #1 is assigned to IPL Level 2
000 = Alternate Register Set #1 is assigned to IPL Level 1

REGISTER 30-16: FBTSEQ CONFIGURATION REGISTER

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IBSEQ11	IBSEQ10	IBSEQ9	IBSEQ8	IBSEQ7	IBSEQ6	IBSEQ5	IBSEQ4
bit 23							bit 16

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IBSEQ3	IBSEQ2	IBSEQ1	IBSEQ0	BSEQ11	BSEQ10	BSEQ9	BSEQ8
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
BSEQ7	BSEQ6	BSEQ5	BSEQ4	BSEQ3	BSEQ2	BSEQ1	BSEQ0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-12 **IBSEQ<11:0>:** Inverse Boot Sequence Number bits (Dual Partition modes only)
The one's complement of BSEQ<11:0>; must be calculated by the user and written into device programming.

bit 11-0 **BSEQ<11:0>:** Boot Sequence Number bits (Dual Partition modes only)
Relative value defining which partition will be active after a device Reset; the partition containing a lower boot number will be active.

TABLE 33-7: POWER-DOWN CURRENT (I_{PD})(2)

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended						
Parameter No.	**Characteristic**	**Typ.(1)**	**Max.**	**Units**	**Conditions**	
DC60	Base Power-Down Current	270	383	µA	-40°C	3.3V
		418.99	770	µA	+25°C	
		939.53	3820	µA	+85°C	
		5.59	14.95	mA	+125°C(3)	

Note 1: Data in the "Typ." column are for design guidance only and are not tested.

2: Base Sleep current (I_{PD}) is measured as follows:

- OSC1 pin is driven with external 8 MHz square wave with levels from 0.3V to V_{DD} – 0.3V
- OSC2 is configured as an I/O in the Configuration Words (OSCIOFCN (FOSC<2>) = 0)
- FSCM is disabled (FCKSM<1:0> (FOSC<7:6>) = 01)
- Watchdog Timer is disabled (FWDT<15> = 0 and WDTCONL<15> = 0)
- All I/O pins (except OSC1) are configured as outputs and driving low
- No peripheral modules are operating or being clocked (defined PMDx bits are all '1's)
- JTAG is disabled (JTAGEN (FICD<5>) = 0)
- The regulators are in Standby mode (VREGS (RCON<8>) = 0
- The regulators are in Low-Power mode (LPWREN (VREGCON<15>) = 1

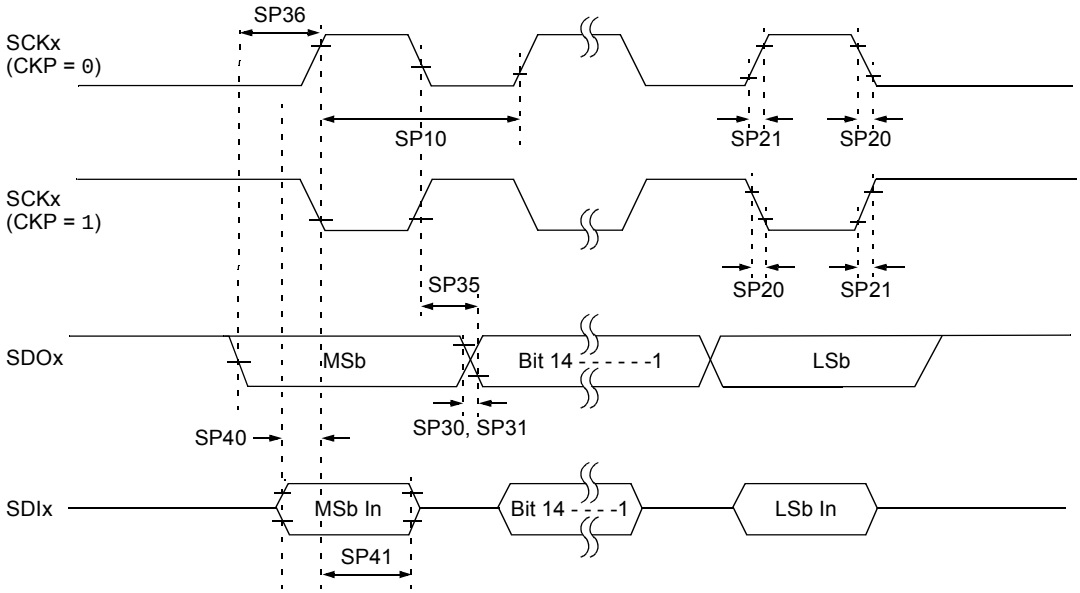
3: The regulators are in High-Power mode (LPWREN (VREGCON<15>) = 0.

TABLE 33-8: DOZE CURRENT (I_{DOZE})

Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Parameter No.	**Typ.(1)**	**Max.**	**Doze Ratio**	**Units**	**Conditions**		
DC70	18.19	20	1:2	mA	-40°C	3.3V	70 MIPS
	12.66	15	1:128	mA			
	17.54	20.15	1:2	mA	+25°C		
	12.39	14.7	1:128	mA			
	17.85	22.1	1:2	mA	+85°C		
	12.7	16.5	1:128	mA			
	20.32	30.45	1:2	mA	+125°C		
	15.17	25.05	1:128	mA			
DC71	22.3	25.55	1:2	mA	-40°C	3.3V	100 MIPS
	14.83	17.25	1:128	mA			
	21.86	25.05	1:2	mA	+25°C		
	14.55	16.95	1:128	mA			
	22.16	26.65	1:2	mA	+85°C		
	14.86	18.7	1:128	mA			
	24.62	35.55	1:2	mA	+125°C		
	17.31	27.3	1:128	mA			

Note 1: Data in the "Typ." column are for design guidance only and are not tested.

FIGURE 33-9: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 33-1 for load conditions.

TABLE 33-29: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

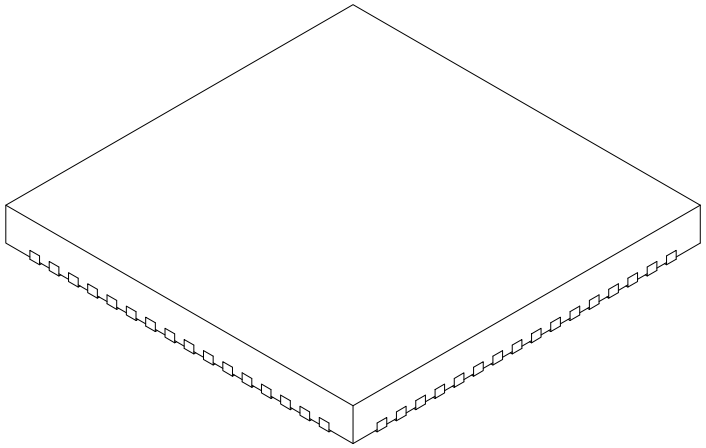
Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCKx Frequency	—	—	15	MHz	Using PPS pins
			—	—	40	MHz	SPIx dedicated pins
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	Using PPS pins
			3	—	—	ns	SPIx dedicated pins
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			10	—	—	ns	SPIx dedicated pins
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	Using PPS pins
			15	—	—	ns	SPIx dedicated pins

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

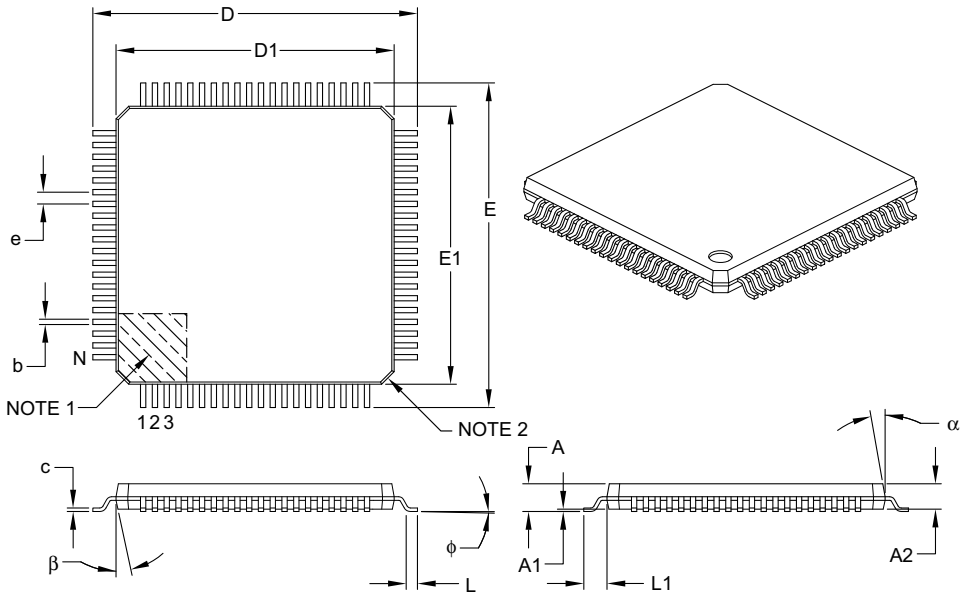
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B