Microchip Technology - DSPIC33CK32MP202T-I/2N Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck32mp202t-i-2n

TABLE 6: 48-PIN TQFP, UQFN

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/RB14	25	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	**RP47**/PWM1L/RB15	26	PGD2/OA2IN-/AN8/**RP35**/RB3
3	**RP60**/PWM8H/RC12	27	PGC2/OA2IN+/**RP36**/RB4
4	**RP61**/PWM8L/RC13	28	**RP56**/ASDA1/SCK2/RC8
5	$\overline{\text{MCLR}}$	29	**RP57**/ASCL1/SDI2/RC9
6	ANN2/**RP77**/RD13	30	**RP72**/SDO2/PCI19/RD8
7	AN12/ANN0/**RP48**/RC0	31	VSS
8	OA1OUT/AN0/CMP1A/IBIAS0/RA0	32	VDD
9	OA1IN-/ANA1/RA1	33	PGD3/**RP37**/PWM6L/SDA2/RB5
10	OA1IN+/AN9/RA2	34	PGC3/**RP38**/PWM6H/SCL2/RB6
11	DACOUT1/AN3/CMP1C/RA3	35	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
12	OA3OUT/AN4/CMP3B/IBIAS3/RA4	36	PGD1/AN10/**RP40**/SCL1/RB8
13	AVDD	37	PGC1/AN11/**RP41**/SDA1/RB9
14	AVSS	38	**RP52**/PWM5H/ASDA2/RC4
15	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	39	**RP53**/PWM5L/ASCL2/RC5
16	OA3IN+/AN14/CMP2B/ISRC1/**RP50**/RC2	40	**RP58**/PWM7H/RC10
17	AN17/ANN1/IBIAS1/**RP54**/RC6	41	**RP59**/PWM7L/RC11
18	VDD	42	VSS
19	VSS	43	VDD
20	AN15/CMP2A/IBIAS2/**RP51**/RC3	44	**RP65**/PWM4H/RD1
21	OSCI/CLKI/AN5/**RP32**/RB0	45	TMS/**RP42**/PWM3H/RB10
22	OSCO/CLKO/AN6/**RP33**/RB1	46	TCK/**RP43**/PWM3L/RB11
23	AN18/CMP3C/ISRC3/**RP74**/RD10	47	TDI/**RP44**/PWM2H/RB12
24	AN16/ISRC2/**RP55**/RC7	48	**RP45**/PWM2L/RB13

Note: **RPn** represents remappable peripheral functions.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
AN0-AN23	I	Analog	No	Analog input channels
ANA0-ANA2	I	Analog	No	Analog alternate inputs
ANN0-ANN2	I	Analog	No	Analog negative inputs
ADTRG	I	ST	Yes	ADC Trigger Input 31
CLKI	I	ST/ CMOS	No	External Clock (EC) source input. Always associated with OSCI pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSCO pin function.
OSCI	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSCO	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output
REFOI	I	ST	Yes	Reference clock input
INT0	I	ST	No	External Interrupt 0
INT1	I	ST	Yes	External Interrupt 1
INT2	I	ST	Yes	External Interrupt 2
INT3	I	ST	Yes	External Interrupt 3
IOCA<4:0>	I	ST	No	Interrupt-on-Change input for PORTA
IOCB<15:0>	I	ST	No	Interrupt-on-Change input for PORTB
IOCC<15:0>	I	ST	No	Interrupt-on-Change input for PORTC
IOCD<15:0>	I	ST	No	Interrupt-on-Change input for PORTD
IOCE<15:0>	I	ST	No	Interrupt-on-Change input for PORTE
RP32-RP71	I/O	ST	Yes	Remappable I/O ports
RA0-RA4	I/O	ST	No	PORTA is a bidirectional I/O port
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port
RC0-RC15	I/O	ST	No	PORTC is a bidirectional I/O port
RD0-RD15	I/O	ST	No	PORTD is a bidirectional I/O port
RE0-RE15	I/O	ST	No	PORTE is a bidirectional I/O port
T1CK	I	ST	Yes	Timer1 external clock input
CAN1RX	I	ST	Yes	CAN1 receive input
CAN1	O	—	Yes	CAN1 transmit output
$\overline{\text{U1CTS}}$	I	ST	Yes	UART1 Clear-to-Send
$\overline{\text{U1RTS}}$	O	—	Yes	UART1 Request-to-Send
U1RX	I	ST	Yes	UART1 receive
U1TX	O	—	Yes	UART1 transmit
$\overline{\text{U1DSR}}$	I	ST	Yes	UART1 Data-Set-Ready
$\overline{\text{U1DTR}}$	O	—	Yes	UART1 Data-Terminal-Ready

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer; DIG = Digital

Note 1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4L and PWM4H pins are available on PPS as well as dedicated.

3: SPI2 supports dedicated pins as well as PPS on 48, 64 and 80-pin devices.

TABLE 7-4: INTERRUPT PRIORITY REGISTERS

Register	Address	Bit 15	Bit14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPC0	840h	—	CNBIP2	CNBIP1	CNBIP0	—	CNAIP2	CNAIP1	CNAIP0	—	T1IP2	T1IP1	T1IP0	—	INT0IP2	INT0IP1	INT0IP0
IPC1	842h	—	CCT1IP2	CCT1IP1	CCT1IP0	—	CCP1IP2	CCP1IP1	CCP1IP0	—	—	—	—	—	DMA0IP2	DMA0IP1	DMA0IP0
IPC2	844h	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1TXIP2	SPI1TXIP1	SPI1TXIP0	—	SPI1RXIP2	SPI1RXIP1	SPI1RXIP0	—	DMA1IP2	DMA1IP1	DMA1IP0
IPC3	846h	—	INT1IP2	INT1IP1	INT1IP0	—	NVMIP2	NVMIP1	NVMIP0	—	ECCSBEIP2	ECCSBEIP1	ECCSBEIP0	—	U1TXIP2	U1TXIP1	U1TXIP0
IPC4	848h	—	CNCIP2	CNCIP1	CNCIP0	—	DMA2IP2	DMA2IP1	DMA2IP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0
IPC5	84Ah	—	CCP2IP2	CCP2IP1	CCP2IP0	—	—	—	—	—	DMA3IP2	DMA3IP1	DMA3IP20	—	INT2IP2	INT2IP1	INT2IP0
IPC6	84Ch	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT3IP2	INT3IP1	INT3IP0	—	C1IP2	C1IP1	C1IP0	—	CCT2IP2	CCT2IP1	CCT2IP0
IPC7	84Eh	—	C1RXIP2	C1RXIP1	C1RXIP0	—	SPI2TXIP2	SPI2TXIP1	SPI2TXIP0	—	SPI2RXIP2	SPI2RXIP1	SPI2RXIP0	—	U2TXIP2	U2TXIP1	U2TXIP0
IPC8	850h	—	CCP3IP2	CCP3IP1	CCP3IP0	—	—	—	—	—	—	—	—	—	—	—	—
IPC9	852h	—	—	—	—	—	MI2C2IP2	MI2C2IP1	MI2C2IP0	—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	CCT3IP2	CCT3IP1	CCT3IP0
IPC10	854h	—	CCP5IP2	CCP5IP1	CCP5IP0	—	—	—	—	—	CCT4IP2	CCT4IP1	CCT4IP0	—	CCP4IP2	CCP4IP1	CCP4IP0
IPC11	856h	—	CCT6IP2	CCT6IP1	CCT6IP0	—	CCP6IP2	CCP6IP1	CCP6IP0	—	DMTIP2	DMTIP1	DMTIP0	—	CCT5IP2	CCT5IP1	CCT5IP0
IPC12	858h	—	CRCIP2	CRCIP1	CRCIP0	—	U2EIP2	U2EIP1	U2EIP0	—	U1EIP2	U1EIP1	U1EIP0	—	QEI1IP2	QEI1IP1	QEI1IP0
IPC13	85Ah	—	—	—	—	—	QEI2IP2	QEI2IP1	QEI2IP0	—	—	—	—	—	C1TXIP2	C1TXIP1	C1TXIP0
IPC14	85Ch	—	SPI3RXIP2	SPI3RXIP1	SPI3RXIP0	—	U3TXIP2	U3TXIP1	U3TXIP1	—	U3RXIP2	U3RXIP1	U3RXIP0	—	U3EIP2	U3EIP1	U3EIP0
IPC15	85Eh	—	PTGSTEPIP2	PTGSTEPIP1	PTGSTEPIP0	—	JTAGIP2	JTAGIP1	JTAGIP0	—	ICDIP2	ICDIP1	ICDIP0	—	SPI3TXIP2	SPI3TXIP1	SPI3TXIP0
IPC16	860h	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	I2C2BCIP2	I2C2BCIP1	I2C2BCIP0	—	I2C1BCIP2	I2C1BCIP1	I2C1BCIP0
IPC17	862h	—	PWM5IP2	PWM5IP1	PWM5IP0	—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0	—	PWM2IP2	PWM2IP1	PWM2IP0
IPC18	864h	—	CNDIP2	CNDIP1	CNDIP0	—	PWM8IP2	PWM8IP1	PWM8IP0	—	PWM7IP2	PWM7IP1	PWM7IP0	—	PWM6IP2	PWM6IP1	PWM6IP0
IPC19	866h	—	CMP3IP2	CMP3IP1	CMP3IP0	—	CMP2IP2	CMP2IP1	CMP2IP0	—	CMP1IP2	CMP1IP1	CMP1IP0	—	CNEIP2	CNEIP1	CNEIP0
IPC20	868h	—	PTG1IP2	PTG1IP1	PTG1IP0	—	PTG0IP2	PTG0IP1	PTG0IP0	—	PTGWDTIP2	PTGWDTIP1	PTGWDTIP0	—	—	—	—
IPC21	86Ah	—	SENT1EIP2	SENT1EIP1	SENT1EIP0	—	SENT1IP2	SENT1IP1	SENT1IP0	—	PTG3IP2	PTG3IP1	PTG3IP0	—	PTG2IP2	PTG2IP1	PTG2IP0
IPC22	86Ch	—	ADCAN0IP2	ADCAN0IP1	ADCAN0IP0	—	ADCIP2	ADCIP1	ADCIP0	—	SENT2EIP2	SENT2EIP1	SENT2EIP0	—	SENT2IP2	SENT2IP1	SENT2IP0
IPC23	86Eh	—	ADCAN4IP2	ADCAN4IP1	ADCAN4IP0	—	ADCAN3IP2	ADCAN3IP1	ADCAN3IP0	—	ADCAN2IP2	ADCAN2IP1	ADCAN2IP0	—	ADCAN1IP2	ADCAN1IP1	ADCAN1IP0
IPC24	870h	—	ADCAN8IP2	ADCAN8IP1	ADCAN8IP0	—	ADCAN7IP2	ADCAN7IP1	ADCAN7IP0	—	ADCAN6IP2	ADCAN6IP1	ADCAN6IP0	—	ADCAN5IP2	ADCAN5IP1	ADCAN5IP0
IPC25	872h	—	ADCAN12IP2	ADCAN12IP1	ADCAN12IP0	—	ADCAN11IP2	ADCAN11IP1	ADCAN11IP0	—	ADCAN10IP2	ADCAN10IP1	ADCAN10IP0	—	ADCAN9IP2	ADCAN9IP1	ADCAN9IP0
IPC26	874h	—	ADCAN16IP2	ADCAN16IP2	ADCAN16IP2	—	ADCAN15IP2	ADCAN15IP1	ADCAN15IP0	—	ADCAN14IP2	ADCAN14IP1	ADCAN14IP0	—	ADCAN13IP2	ADCAN13IP1	ADCAN13IP0
IPC27	876h	—	ADCAN20IP2	ADCAN20IP1	ADCAN20IP0	—	ADCAN19IP2	ADCAN19IP1	ADCAN19IP0	—	ADCAN18IP2	ADCAN18IP1	ADCAN18IP0	—	ADCAN17IP2	ADCAN17IP1	ADCAN17IP0
IPC28	878h	—	ADFLTIP2	ADFLTIP1	ADFLTIP0	—	ADCAN23IP2	ADCAN23IP1	ADCAN22IP0	—	ADCAN22IP2	ADCAN22IP1	ADCAN22IP0	—	ADCAN21IP2	ADCAN21IP1	ADCAN21IP0
IPC29	87Ah	—	ADCMP3IP2	ADCMP3IP1	ADCMP3IP0	—	ADCMP2IP2	ADCMP2IP1	ADCMP2IP0	—	ADCMP1IP2	ADCMP1IP1	ADCMP1IP0	—	ADCMP0IP2	ADCMP0IP1	ADCMP0IP0
IPC30	87Ch	—	ADFLTR3IP2	ADFLTR3IP1	ADFLTR3IP0	—	ADFLTR2IP2	ADFLTR2IP1	ADFLTR2IP0	—	ADFLTR1IP2	ADFLTR1IP1	ADFLTR1IP0	—	ADFLTR0IP2	ADFLTR0IP1	ADFLTR0IP0
IPC31	87Eh	—	SPI2GIP0	SPI2GIP1	SPI2GIP0	—	SPI1GIP2	SPI1GIP1	SPI1GIP0	—	CLC2PIP2	CLC2PIP1	CLC2PIP0	—	CLC1PIP2	CLC1PIP1	CLC1PIP0
IPC32	880h	—	—	—	—	—	—	—	—	—	—	—	—	—	SPI3GIP2	SPI3GIP1	SPI3GIP0
IPC33	882h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
IPC34	884h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: — = Unimplemented.

7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

7.3.1 KEY RESOURCES

- **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

7.4 Interrupt Control and Status Registers

The dsPIC33CK256MP508 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

7.4.0.1 INTCON1 through INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior, contains the Global Interrupt Enable bit (GIE) and the Alternate Interrupt Vector Table Enable bit (AIVTEN).

INTCON3 contains the status flags for the Auxiliary PLL and DO stack overflow status trap sources.

The INTCON4 register contains the Software Generated Hard Trap Status bit (SGHT).

7.4.0.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.4.0.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.0.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of seven priority levels.

7.4.0.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<7:0>) and Interrupt Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP<2:0> bits in the first position of IPC0 (IPC0<2:0>).

7.4.0.6 Status/Control Registers

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"dsPIC33E Enhanced CPU"** (DS70005158) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit, which together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

REGISTER 9-7: APLLFBD1: APLL FEEDBACK DIVIDER REGISTER

U-0	U-0	U-0	U-0	r-0	r-0	r-0	r-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0
APLLFBDIV<7:0>							
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **Reserved:** Maintain as '0'

bit 7-0 **APLLFBDIV<7:0>:** APLL Feedback Divider bits

11111111 = Reserved
...
11001000 = 200 maximum(1)
...
10010110 = 150 (default)
...
00010000 = 16 minimum(1)
...
00000010 = Reserved
00000001 = Reserved
00000000 = Reserved

Note 1: The allowed range is 16-200 (decimal). The rest of the values are reserved and should be avoided. The power-on default feedback divider is 150 (decimal) with an 8 MHz FRC input clock; the VCO frequency is 1.2 GHz.

REGISTER 9-10: REFOCONL: REFERENCE CLOCK CONTROL LOW REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HSC
ROEN	—	ROSIDL	ROOUT	ROSLP	—	ROSWEN	ROACTIV
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	ROSEL3	ROSEL2	ROSEL1	ROSEL0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROEN:** Reference Clock Enable bit
1 = Reference Oscillator is enabled on the REFCLKO pin
0 = Reference Oscillator is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSIDL:** Reference Clock Stop in Idle bit
1 = Reference Oscillator continues to run in Idle mode
0 = Reference Oscillator is disabled in Idle mode

bit 12 **ROOUT:** Reference Clock Output Enable bit
1 = Reference clock external output is enabled and available on the REFCLKO pin
0 = Reference clock external output is disabled

bit 11 **ROSLP:** Reference Clock Stop in Sleep bit
1 = Reference Oscillator continues to run in Sleep modes
0 = Reference Oscillator is disabled in Sleep modes

bit 10 **Unimplemented:** Read as '0'

bit 9 **ROSWEN:** Reference Clock Output Enable bit
1 = Clock divider change (requested by changes to RODIVx) is requested or is in progress (set in software, cleared by hardware upon completion)
0 = Clock divider change has completed or is not pending

bit 8 **ROACTIV:** Reference Clock Status bit
1 = Reference clock is active; do not change clock source
0 = Reference clock is stopped; clock source and configuration may be safely changed

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits
1111 = Reserved
... = Reserved
1000 = Reserved
0111 = REFI pin
0110 = FVCO/4
0101 = BFRC
0100 = LPRC
0011 = FRC
0010 = Primary Oscillator
0001 = Peripheral clock (FP)
0000 = System clock (FOSC)

REGISTER 11-29: C1TXQCONH: CAN TRANSMIT QUEUE CONTROL REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLSIZE2(1)	PLSIZE1(1)	PLSIZE0(1)	FSIZE4(1)	FSIZE3(1)	FSIZE2(1)	FSIZE1(1)	FSIZE0(1)
bit 15							bit 8

U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TXAT1	TXAT0	TXPRI4	TXPRI3	TXPRI2	TXPRI1	TXPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **PLSIZE<2:0>:** Payload Size bits(1)
111 = 64 data bytes
110 = 48 data bytes
101 = 32 data bytes
100 = 24 data bytes
011 = 20 data bytes
010 = 16 data bytes
001 = 12 data bytes
000 = 8 data bytes

bit 12-8 **FSIZE<4:0>:** FIFO Size bits(1)
11111 = FIFO is 32 messages deep
...
00010 = FIFO is 3 messages deep
00001 = FIFO is 2 messages deep
00000 = FIFO is 1 message deep

bit 7 **Unimplemented:** Read as '0'

bit 6-5 **TXAT<1:0>:** Retransmission Attempts bits
This feature is enabled when RTXAT (C1CONH<0>) is set.
11 = Unlimited number of retransmission attempts
10 = Unlimited number of retransmission attempts
01 = Three retransmission attempts
00 = Disables retransmission attempts

bit 4-0 **TXPRI<4:0>:** Message Transmit Priority bits
11111 = Highest message priority
...
00000 = Lowest message priority

Note 1: These bits can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 12-2: FSCL: FREQUENCY SCALE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FSCL<15:0>:** Frequency Scale Register bits
The value in this register is added to the frequency scaling accumulator at each pwm_master_clk. When the accumulated value exceeds the value of FSMINPER, a clock pulse is produced.

REGISTER 12-3: FSMINPER: FREQUENCY SCALING MINIMUM PERIOD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FSMINPER<15:0>:** Frequency Scaling Minimum Period Register bits
This register holds the minimum clock period (maximum clock frequency) that can be produced by the frequency scaling circuit.

REGISTER 12-15: PGxIOCONL: PWM GENERATOR x I/O CONTROL REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLMOD	SWAP	OVRENH	OVRENL	OVRDAT1	OVRDAT0	OSYNC1	OSYNC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	FFDAT1	FFDAT0	DBDAT1	DBDAT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CLMOD:** Current-Limit Mode Select bit
1 = If PCI current limit is active, then the PWMxH and PWMxL output signals are inverted (bit flipping), and the CLDAT<1:0> bits are not used
0 = If PCI current limit is active, then the CLDAT<1:0> bits define the PWM output levels

bit 14 **SWAP:** Swap PWM Signals to PWMxH and PWMxL Device Pins bit
1 = The PWMxH signal is connected to the PWMxL pin and the PWMxL signal is connected to the PWMxH pin
0 = PWMxH/L signals are mapped to their respective pins

bit 13 **OVRENH:** User Override Enable for PWMxH Pin bit
1 = OVRDAT1 provides data for output on the PWMxH pin
0 = PWM Generator provides data for the PWMxH pin

bit 12 **OVRENL:** User Override Enable for PWMxL Pin bit
1 = OVRDAT0 provides data for output on the PWMxL pin
0 = PWM Generator provides data for the PWMxL pin

bit 11-10 **OVRDAT<1:0>:** Data for PWMxH/PWMxL Pins if Override is Enabled bits
If OVERENH = 1, then OVRDAT1 provides data for PWMxH.
If OVERENL = 1, then OVRDAT0 provides data for PWMxL.

bit 9-8 **OSYNC<1:0>:** User Output Override Synchronization Control bits
11 = Reserved
10 = User output overrides via the OVRENH/L and OVRDAT<1:0> bits occur when specified by the UPDMOD<2:0> bits in the PGxCONH register
01 = User output overrides via the OVRENH/L and OVRDAT<1:0> bits occur immediately (as soon as possible)
00 = User output overrides via the OVRENH/L and OVRDAT<1:0> bits are synchronized to the local PWM time base (next Start-of-Cycle)

bit 7-6 **FLTDAT<1:0>:** Data for PWMxH/PWMxL Pins if Fault Event is Active bits
If Fault is active, then FLTDAT1 provides data for PWMxH.
If Fault is active, then FLTDAT0 provides data for PWMxL.

bit 5-4 **CLDAT<1:0>:** Data for PWMxH/PWMxL Pins if Current-Limit Event is Active bits
If current limit is active, then CLDAT1 provides data for PWMxH.
If current limit is active, then CLDAT0 provides data for PWMxL.

bit 3-2 **FFDAT<1:0>:** Data for PWMxH/PWMxL Pins if Feed-Forward Event is Active bits
If feed-forward is active, then FFDAT1 provides data for PWMxH.
If feed-forward is active, then FFDAT0 provides data for PWMxL.

bit 1-0 **DBDAT<1:0>:** Data for PWMxH/PWMxL Pins if Debug Mode is Active bits
If Debug mode is active and device halted, then DBDAT1 provides data for PWMxH.
If Debug mode is active and device halted, then DBDAT0 provides data for PWMxL.

REGISTER 14-2: DACCTRL2H: DAC CONTROL 2 HIGH REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	SSTIME<9:8>(1)	
bit 15							bit 8

R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
SSTIME<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SSTIME<9:0>:** Time from Start of Transition Mode until Steady-State Filter is Enabled bits(1)

Note 1: The value for SSTIME<9:0> should be greater than the TMODTIME<9:0> value.

REGISTER 14-3: DACCTRL2L: DAC CONTROL 2 LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	TMODTIME<9:8>(1)	
bit 15							bit 8

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
TMODTIME<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **TMODTIME<9:0>:** Transition Mode Duration bits(1)

Note 1: The value for TMODTIME<9:0> should be less than the SSTIME<9:0> value.

REGISTER 15-1: QEIxCON: QEIx CONTROL REGISTER (CONTINUED)

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits(3)
(interval timer, main timer (position counter), velocity counter and Index counter internal clock divider select)
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **CNTPOL:** Position and Index Counter/Timer Direction Select bit
1 = Counter direction is negative unless modified by external up/down signal
0 = Counter direction is positive unless modified by external up/down signal

bit 2 **GATEN:** External Count Gate Enable bit
1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter operation

bit 1-0 **CCM<1:0>:** Counter Control Mode Selection bits
11 = Internal Timer mode
10 = External Clock Count with External Gate mode
01 = External Clock Count with External Up/Down mode
00 = Quadrature Encoder mode

Note 1: When CCMx = 10 or CCMx = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.
2: When CCMx = 00, and QEAx and QEBx values match the Index Match Value (IMV), the POSxCNTH and POSxCNTL registers are reset.
3: The selected clock rate should be at least twice the expected maximum quadrature count rate.
4: Not all devices support this mode.
5: The QCAPEN and HCAPEN bits must be cleared during PIMODx Modes 2 through 7 to ensure proper functionality. Not all devices support HCAPEN.

REGISTER 15-4: QEIxSTAT: QEIx STATUS REGISTER (CONTINUED)

bit 2 **HOMIEN:** Home Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **IDXIRQ:** Status Flag for Index Event Status bit
1 = Index event has occurred
0 = No Index event has occurred

bit 0 **IDXIEN:** Index Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

REGISTER 16-7: UxRXREG: UARTx RECEIVE BUFFER REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
RXREG<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **RXREG<7:0>:** Received Character Data bits 7-0

REGISTER 16-8: UxTXREG: UARTx TRANSMIT BUFFER REGISTER

W-x	U-0	U-0	U-0	U-0	U-0	U-0	U-0
LAST	—	—	—	—	—	—	—
bit 15							bit 8

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
TXREG7	TXREG6	TXREG5	TXREG4	TXREG3	TXREG2	TXREG1	TXREG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **LAST:** Last Byte Indicator for Smart Card Support bit

bit 14-8 **Unimplemented:** Read as ‘0’

bit 7-0 **TXREG<7:0>:** Transmitted Character Data bits 7-0
If the buffer is full, further writes to the buffer are ignored.

19.0 PARALLEL MASTER PORT (PMP)

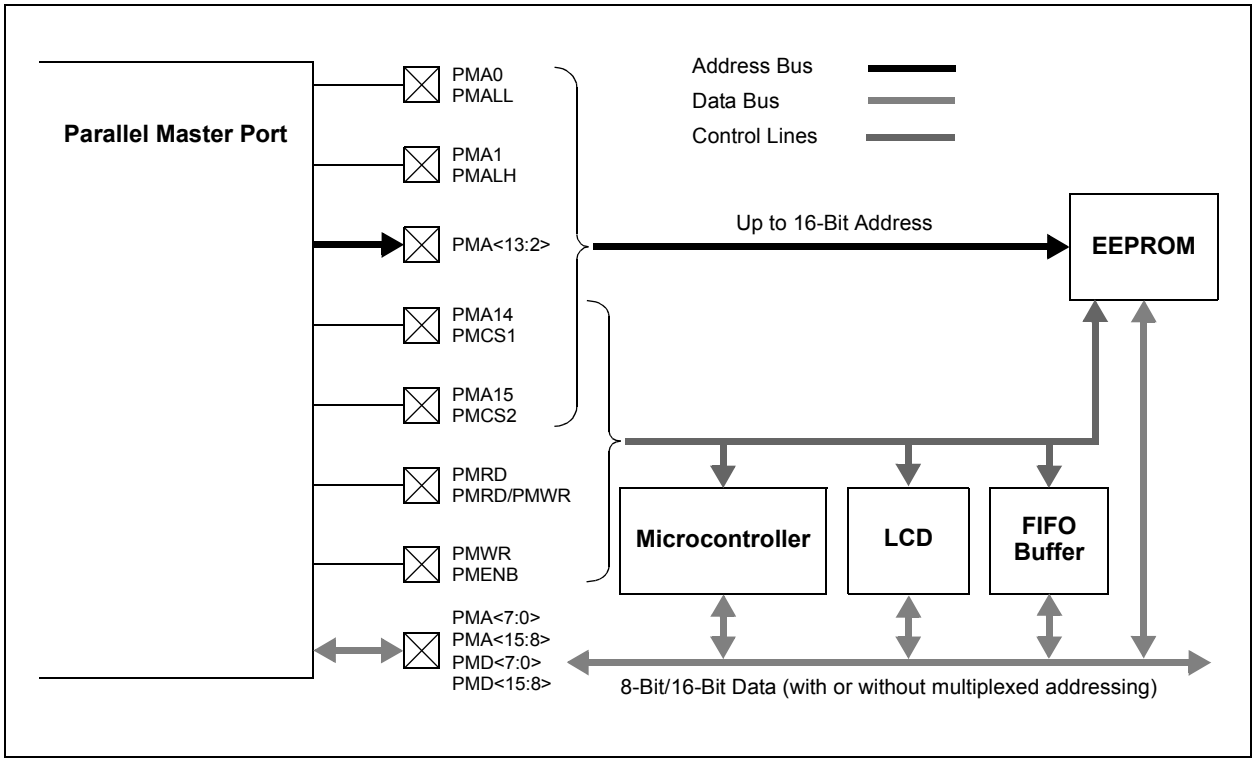
Note 1: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Parallel Master Port (PMP)"** (DS70005344) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Not all device variants include the PMP. Refer to Table 1 and Table 2 for availability.

The Parallel Master Port (PMP) is a parallel 8-bit/16-bit I/O module specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interfaces to parallel peripherals vary significantly, the PMP module is highly configurable. The key features of the PMP module include:

- Master and Slave Operating modes
- Up to 16 Programmable Address Lines
- Up to Two Chip Select Lines
- Programmable Strobe Options:
  - Individual read and write strobes or read/write strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
  - Address support
  - 4 bytes deep, auto-incrementing buffer
- Schmitt Trigger or TTL Input Buffers
- Programmable Wait States
- Dual Buffer Mode with Separate Read and Write Registers
- Read Initiate Control

FIGURE 19-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



REGISTER 19-2: PMCONH: PARALLEL MASTER PORT CONTROL HIGH REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W/HC-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
RDSTART(1)	—	—	—	—	—	DUALBUF	—
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **RDSTART:** Start a Read on PMP Bus bit(1)
- 1 = Starts a read cycle on the PMP bus
- 0 = No effect

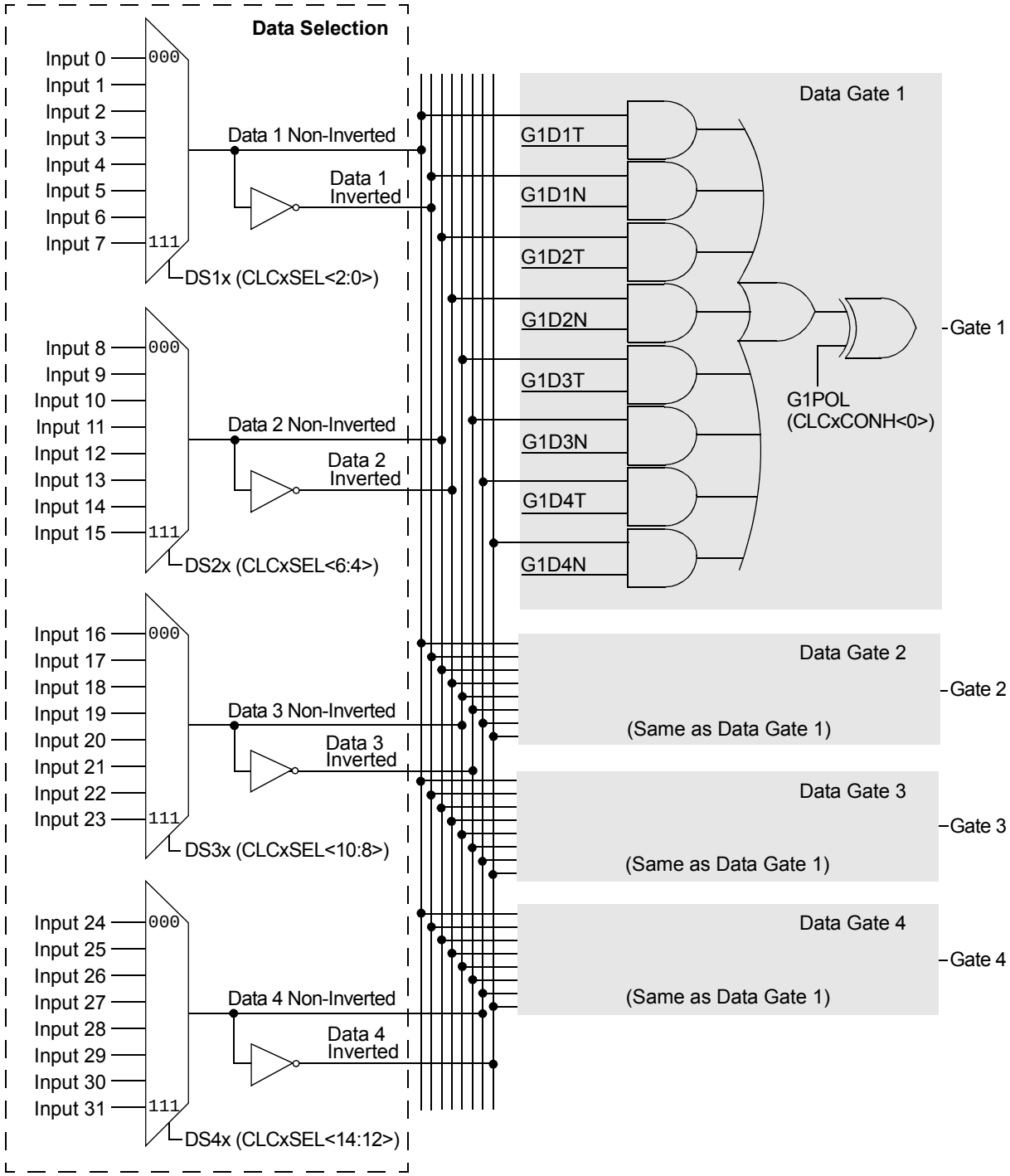
bit 6-2 **Unimplemented:** Read as '0'

bit 1 **DUALBUF:** PMP Dual Read/Write Buffers Enable bit (valid in Master mode only)
- 1 = PMP uses separate registers for reads and writes (PMRADDR, PMDINx, PMWADDR, PMDOUTx)
- 0 = PMP uses legacy registers (PMADDR, PMDINx)

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is cleared by HW at the end of the read cycle when BUSY (PMMODE<15>) = 0.

FIGURE 23-3: CLCx INPUT SOURCE SELECTION DIAGRAM



Note: All controls are undefined at power-up.

TABLE 30-2: dsPIC33CKXXMPX0X CONFIGURATION ADDRESSES

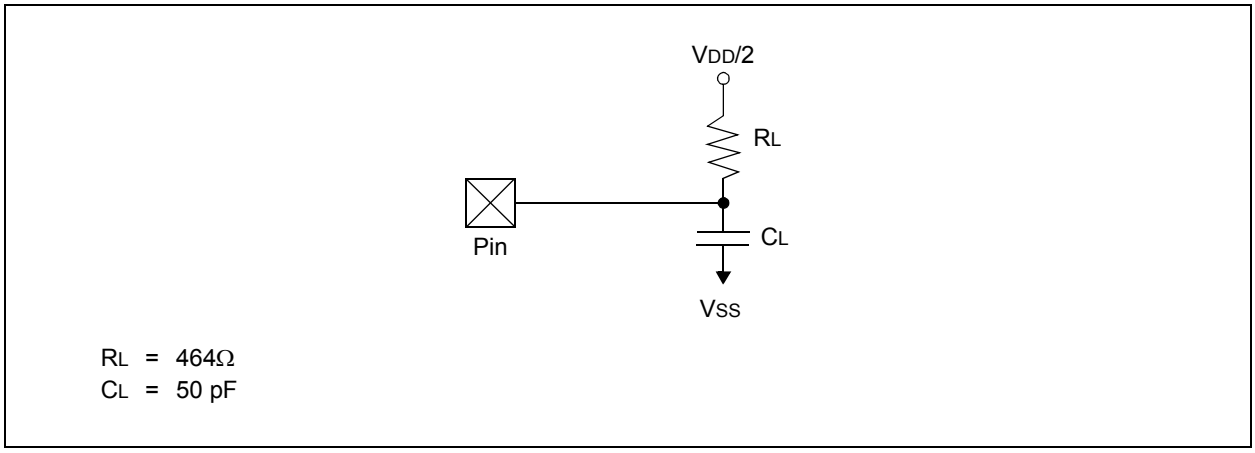
Register Name	Single Partition		Dual Partition, Active		Dual Partition, Inactive	
	64k	32k	64k	32k	64k	32k
FSEC(2)	0x00AF00	0x005F00	0x005F00	0x002F00	0x405F00	0x402F00
FBSLIM(2)	0x00AF10	0x005F10	0x005F10	0x002F10	0x405F10	0x402F10
FSIGN(2)	0x00AF14	0x005F14	0x005F14	0x002F14	0x405F14	0x402F14
FOSCSEL	0x00AF18	0x005F18	0x005F18	0x002F18	0x405F18	0x402F18
FOSC	0x00AF1C	0x005F1C	0x005F1C	0x002F1C	0x405F1C	0x402F1C
FWDT	0x00AF20	0x005F20	0x005F20	0x002F20	0x405F20	0x402F20
FPOR	0x00AF24	0x005F24	0x005F24	0x002F24	0x405F24	0x402F24
FICD	0x00AF28	0x005F28	0x005F28	0x002F28	0x405F28	0x402F28
FDMTIVTL	0x00AF2C	0x005F2C	0x005F2C	0x002F2C	0x405F2C	0x402F2C
FDMTIVTH	0x00AF30	0x005F30	0x005F30	0x002F30	0x405F30	0x402F30
FDMTCNTL	0x00AF34	0x005F34	0x005F34	0x002F34	0x405F34	0x402F34
FDMTCNTH	0x00AF38	0x005F38	0x005F38	0x002F38	0x405F38	0x402F38
FDMT	0x00AF3C	0x005F3C	0x005F3C	0x002F3C	0x405F3C	0x402F3C
FDEVOPT1	0x00AF40	0x005F40	0x005F40	0x002F40	0x405F40	0x402F40
FALTREG	0x00AF44	0x005F44	0x005F44	0x002F44	0x405F44	0x402F44
FBTSEQ	0x00AFFC	0x005FFC	0x005FFC	0x002FFC	0x405FFC	0x402FFC
FBOOT(1)	0x801800					

Note 1: FBOOT resides in calibration memory space.

2: Changes to the Inactive Partition Configuration Words affect how the Active Partition accesses the Inactive Partition.

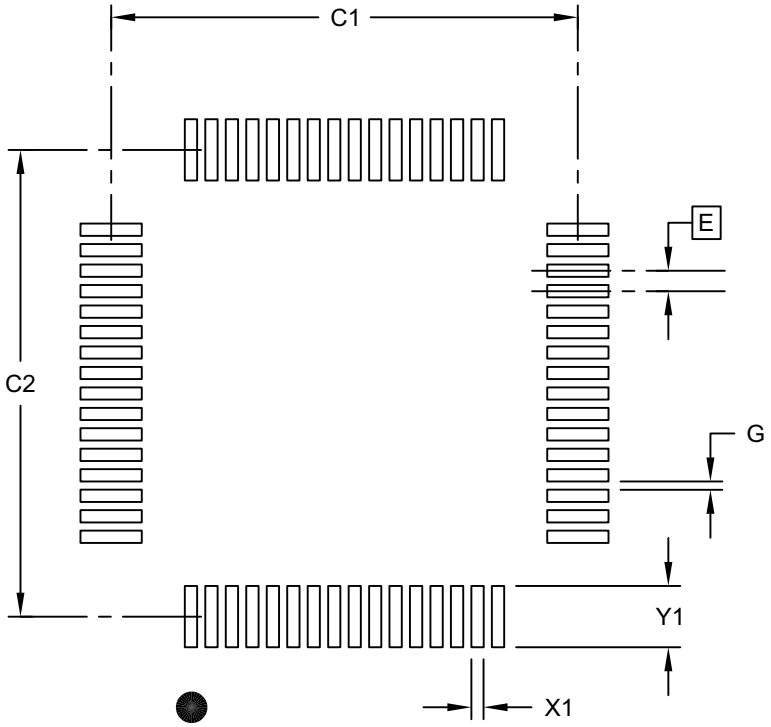
33.2 AC Characteristics and Timing Parameters

FIGURE 33-1: LOAD CONDITIONS FOR I/O SPECIFICATIONS



64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

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V

W

