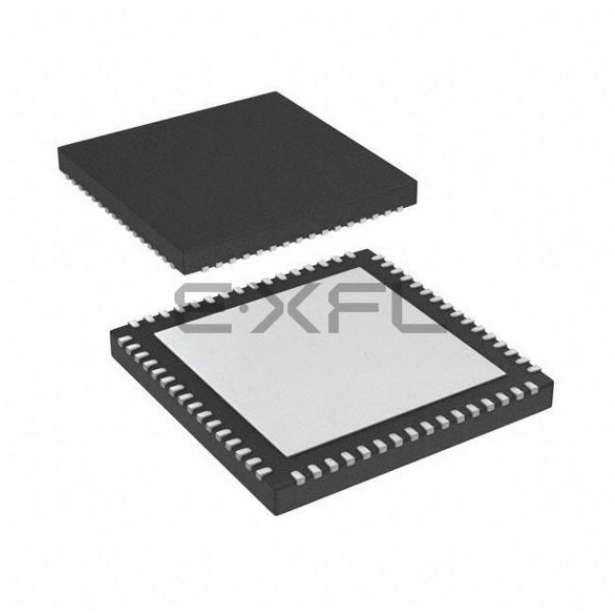

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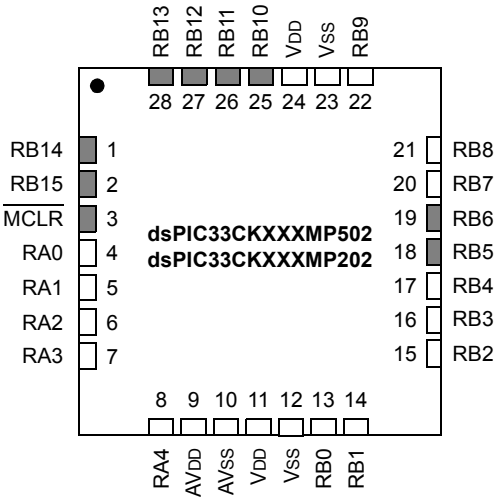
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 20x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck32mp206t-i-mr

Pin Diagrams (Continued)

28-Pin UQFN



Note: Shaded pins are up to 5 VDC tolerant.

TABLE 4: 28-PIN UQFN

Pin #	Function	Pin #	Function
1	**RP46**/PWM1H/RB14	15	OA2OUT/AN1/AN7/ANA0/CMP1D/CMP2D/CMP3D/**RP34**/SCL3/INT0/RB2
2	**RP47**/PWM1L/RB15	16	PGD2/OA2IN-/AN8/**RP35**/RB3
3	MCLR	17	PGC2/OA2IN+/**RP36**/RB4
4	OA1OUT/AN0/CMP1A/IBIAS0/RA0	18	PGD3/**RP37**/SDA2/RB5
5	OA1IN-/ANA1/RA1	19	PGC3/**RP38**/SCL2/RB6
6	OA1IN+/AN9/RA2	20	TDO/AN2/CMP3A/**RP39**/SDA3/RB7
7	DACOUT1/AN3/CMP1C/RA3	21	PGD1/AN10/**RP40**/SCL1/RB8
8	AN4/CMP3B/IBIAS3/RA4	22	PGC1/AN11/**RP41**/SDA1/RB9
9	AVDD	23	VSS
10	AVSS	24	VDD
11	VDD	25	TMS/**RP42**/PWM3H/RB10
12	VSS	26	TCK/**RP43**/PWM3L/RB11
13	OSCI/CLKI/AN5/**RP32**/RB0	27	TDI/**RP44**/PWM2H/RB12
14	OSCO/CLKO/AN6/**RP33**/RB1	28	**RP45**/PWM2L/RB13

Note: RPn represents remappable peripheral functions.

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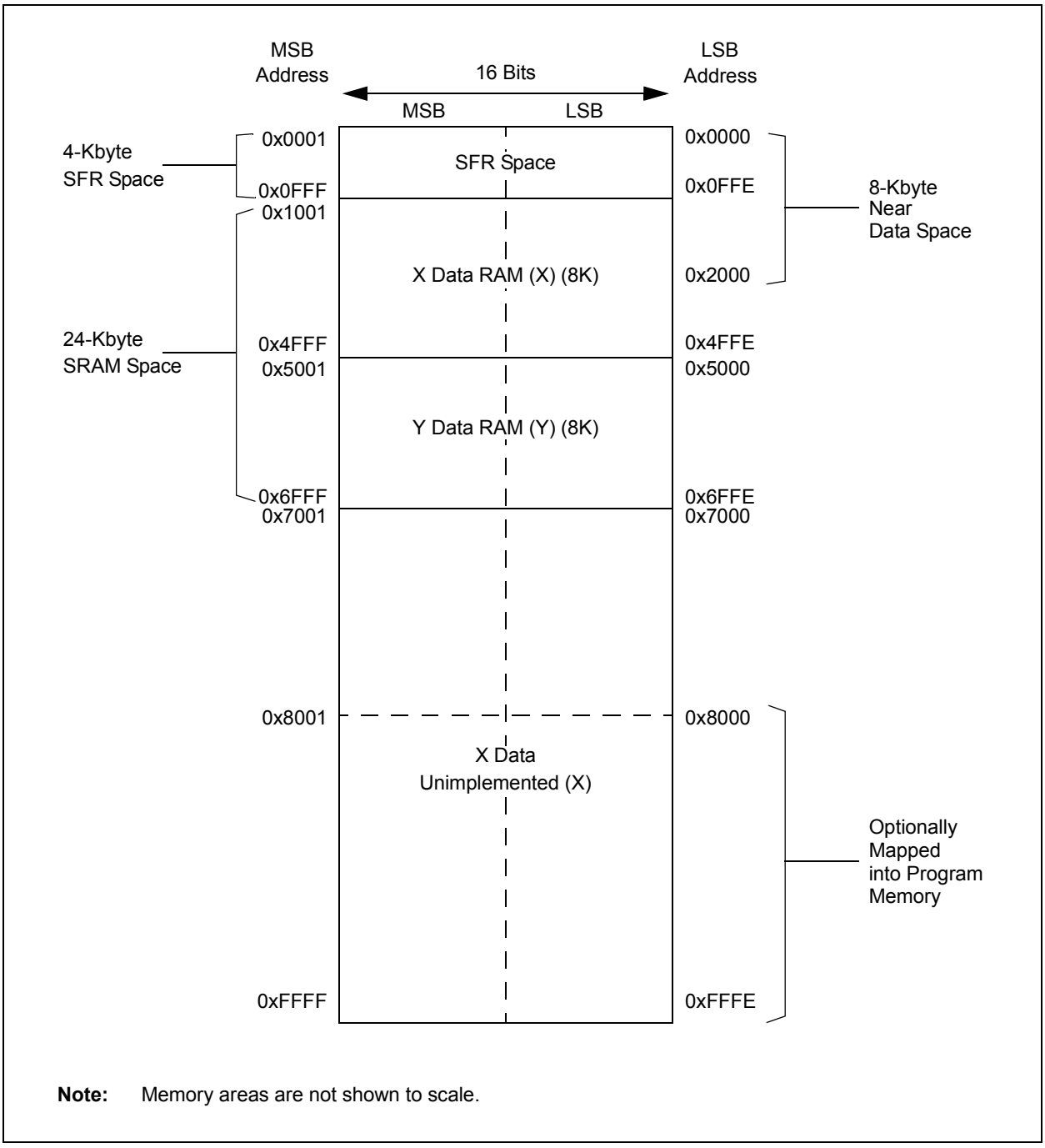
FIGURE 4-7: DATA MEMORY MAP FOR dsPIC33CK256MPX0X DEVICES



Note: Memory areas are not shown to scale.

8.5.10 PERIPHERAL PIN SELECT REGISTERS

REGISTER 8-13: RPCON: PERIPHERAL REMAPPING CONFIGURATION REGISTER(1)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	IOLOCK	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **IOLOCK:** Peripheral Remapping Register Lock bit
1 = All Peripheral Remapping registers are locked and cannot be written
0 = All Peripheral Remapping registers are unlocked and can be written

bit 10-0 **Unimplemented:** Read as ‘0’

Note 1: Writing to this register needs an unlock sequence.

REGISTER 8-14: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT1R7	INT1R6	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **INT1R<7:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
See Table 8-4.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 8-58: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 8-7 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 8-7 for peripheral function numbers)

REGISTER 8-59: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 8-7 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 8-7 for peripheral function numbers)

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REGISTER 9-7: APLLFBD1: APLL FEEDBACK DIVIDER REGISTER

U-0	U-0	U-0	U-0	r-0	r-0	r-0	r-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0
APLLFBDIV<7:0>							
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **Reserved:** Maintain as '0'

bit 7-0 **APLLFBDIV<7:0>:** APLL Feedback Divider bits

11111111 = Reserved
...
11001000 = 200 maximum(1)
...
10010110 = 150 (default)
...
00010000 = 16 minimum(1)
...
00000010 = Reserved
00000001 = Reserved
00000000 = Reserved

Note 1: The allowed range is 16-200 (decimal). The rest of the values are reserved and should be avoided. The power-on default feedback divider is 150 (decimal) with an 8 MHz FRC input clock; the VCO frequency is 1.2 GHz.

12.0 HIGH-RESOLUTION PWM WITH FINE EDGE PLACEMENT

Note 1: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Resolution PWM with Fine Edge Placement"** (DS70005320) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The High-Speed PWM (HSPWM) module is a Pulse-Width Modulated (PWM) module to support both motor control and power supply applications. This flexible module provides features to support many types of Motor Control (MC) and Power Control (PC) applications, including:

- AC-to-DC Converters
- DC-to-DC Converters
- AC and DC Motors: BLDC, PMSM, ACIM, SRM, etc.
- Inverters
- Battery Chargers
- Digital Lighting
- Power Factor Correction (PFC)

12.1 Features

- 8 Independent PWM Generators, each with Dual Outputs
- Operating modes:
  - Independent Edge mode
  - Variable Phase PWM mode
  - Center-Aligned mode
  - Double Update Center-Aligned mode
  - Dual Edge Center-Aligned mode
  - Dual PWM mode
- Output modes:
  - Complementary
  - Independent
  - Push-Pull
- Dead-Time Generator
- Leading-Edge Blanking (LEB)
- Output Override for Fault Handling
- Flexible Period/Duty Cycle Updating Options
- Programmable Control Inputs (PCI)
- Advanced Triggering Options
- 6 Combinatorial Logic Outputs
- 6 PWM Event Outputs

REGISTER 12-2: FSCL: FREQUENCY SCALE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSCL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FSCL<15:0>:** Frequency Scale Register bits
The value in this register is added to the frequency scaling accumulator at each pwm_master_clk. When the accumulated value exceeds the value of FSMINPER, a clock pulse is produced.

REGISTER 12-3: FSMINPER: FREQUENCY SCALING MINIMUM PERIOD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FSMINPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FSMINPER<15:0>:** Frequency Scaling Minimum Period Register bits
This register holds the minimum clock period (maximum clock frequency) that can be produced by the frequency scaling circuit.

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REGISTER 12-13: PGxCONH: PWM GENERATOR x CONTROL REGISTER HIGH (CONTINUED)

bit 6 **TRGMOD:** PWM Generator Trigger Mode Selection bit
1 = PWM Generator operates in Retriggerable mode
0 = PWM Generator operates in Single Trigger mode

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **SOCS<3:0>:** Start-of-Cycle Selection bits(1,2,3)
1111 = TRIG bit or PCI Sync function only (no hardware trigger source is selected)
1110-0101 = Reserved
0100 = Trigger output selected by PG4 or PG8 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0011 = Trigger output selected by PG3 or PG7 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0010 = Trigger output selected by PG2 or PG6 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0001 = Trigger output selected by PG1 or PG5 PGTRGSEL<2:0> bits (PGxEVTL<2:0>)
0000 = Local EOC – PWM Generator is self-triggered

Note 1: The PCI selected Sync signal is always available to be OR'd with the selected SOC signal per the SOCS<3:0> bits if the PCI Sync function is enabled.

2: The source selected by the SOCS<3:0> bits MUST operate from the same clock source as the local PWM Generator. If not, the source must be routed through the PCI Sync logic so the trigger signal may be synchronized to the PWM Generator clock domain.

3: PWM Generators are grouped into groups of four: PG1-PG4 and PG5-PG8, if available. Any generator within a group of four may be used to trigger another generator within the same group.

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REGISTER 13-4: ADCON2H: ADC CONTROL REGISTER 2 HIGH

R-0, HSC	R-0, HSC	U-0	r-0	r-0	r-0	R/W-0	R/W-0
REFRDY	REFERR	—	—	—	—	SHRSAMC9	SHRSAMC8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SHRSAMC7	SHRSAMC6	SHRSAMC5	SHRSAMC4	SHRSAMC3	SHRSAMC2	SHRSAMC1	SHRSAMC0
bit 7							bit 0

Legend:	r = Reserved bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **REFRDY:** Band Gap and Reference Voltage Ready Flag bit
1 = Band gap is ready
0 = Band gap is not ready

bit 14 **REFERR:** Band Gap or Reference Voltage Error Flag bit
1 = Band gap was removed after the ADC module was enabled (ADON = 1)
0 = No band gap error was detected

bit 13 **Unimplemented:** Read as '0'

bit 12-10 **Reserved:** Maintain as '0'

bit 9-0 **SHRSAMC<9:0>:** Shared ADC Core Sample Time Selection bits
These bits specify the number of shared ADC Core Clock Periods (TADCORE) for the shared ADC core sample time.
1111111111 = 1025 TADCORE
...
0000000001 = 3 TADCORE
0000000000 = 2 TADCORE

NOTES:

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17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The Serial Peripheral Interface (SPI) module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces. All devices in the dsPIC33CK256MP508 family include three SPI modules. On 48, 64 and 80-pin devices, SPI instance SPI2 can work up to 50 MHz speed when selected as a non-PPS pin. The selection is done using the SPI2PIN bit (FDEVOPT<13>). If the bit for SPI2PIN is '1', the PPS pin will be used. When SPI2PIN is '0', the SPI signals are routed to dedicated pins.

The module supports operation in two Buffer modes. In Standard mode, data is shifted through a single serial buffer. In Enhanced Buffer mode, data is shifted through a FIFO buffer. The FIFO level depends on the configured mode.

Note: FIFO depth for this device is 4 (in 8-Bit Data mode).

Variable length data can be transmitted and received, from 2 to 32 bits.

Note: Do not perform Read-Modify-Write operations (such as bit-oriented instructions) on the SPIxBUF register in either Standard or Enhanced Buffer mode.

The module also supports a basic framed SPI protocol while operating in either Master or Slave mode. A total of four framed SPI configurations are supported.

The module also supports Audio modes. Four different Audio modes are available.

- I^2S mode
- Left Justified mode
- Right Justified mode
- PCM/DSP mode

In each of these modes, the serial clock is free-running and audio data is always transferred.

If an audio protocol data transfer takes place between two devices, then usually one device is the Master and the other is the Slave. However, audio data can be transferred between two Slaves. Because the audio protocols require free-running clocks, the Master can be a third-party controller. In either case, the Master generates two free-running clocks: SCKx and LRC (Left, Right Channel Clock/$\overline{SSx}$/FSYNC).

The SPI serial interface consists of four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SSx}$: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPI module can be configured to operate using 2, 3 or 4 pins. In the 3-pin mode, $\overline{SSx}$ is not used. In the 2-pin mode, both SDOx and $\overline{SSx}$ are not used.

To set up the SPIx module for Audio mode:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   a) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with AUDEN (SPIxCON1H<15>) = 1.
4. Clear the SPIROV bit (SPIxSTATL<6>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

REGISTER 19-9: PMAEN: PARALLEL MASTER PORT PIN ENABLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN<15:14>		PTEN<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN<7:2>						PTEN<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **PTEN<15:14>:** PMCSx Strobe Enable bits
1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1(1)
0 = PMA15 and PMA14 function as port I/Os

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/Os

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
0 = PMA1 and PMA0 pads function as port I/Os

Note 1: The use of these pins as address or Chip Select lines is selected by the CSF<1:0> bits (PMCON<7:6>).

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

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21.1 Timer1 Control Register

REGISTER 21-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0
TON(1)	—	SIDL	TMWDIS	TMWIP	PRWIP	TECS1	TECS0
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
TGATE	—	TCKPS1	TCKPS0	—	TSYNC(1)	TCS(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TMWDIS:** Asynchronous Timer1 Write Disable bit
1 = Timer writes are ignored while a posted write to TMR1 or PR1 is synchronized to the asynchronous clock domain
0 = Back-to-back writes are enabled in Asynchronous mode

bit 11 **TMWIP:** Asynchronous Timer1 Write in Progress bit
1 = Write to the timer in Asynchronous mode is pending
0 = Write to the timer in Asynchronous mode is complete

bit 10 **PRWIP:** Asynchronous Period Write in Progress bit
1 = Write to the Period register in Asynchronous mode is pending
0 = Write to the Period register in Asynchronous mode is complete

bit 9-8 **TECS<1:0>:** Timer1 Extended Clock Select bits
11 = FRC clock
10 = FOSC
01 = TCY
00 = External Clock comes from the T1CK pin

bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

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REGISTER 22-4: CCPxCON2H: CCPx CONTROL 2 HIGH REGISTERS

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **OC<F:A>EN:** Output Enable/Steering Control bits(1)
1 = OCMx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCMx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 7-6 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output is defined by module operating mode (see Table 22-4)
01 = Time base rollover event (all modes)
00 = Disabled

bit 2-0 **ICS<2:0>:** Input Capture Source Select bits
111 = CLC4 output
110 = CLC3 output
101 = CLC2 output
100 = CLC1 output
011 = Comparator 3 output
010 = Comparator 2 output
001 = Comparator 1 output
000 = SCCP Input Capture x (ICx) pin (PPS)

Note 1: OCFEN through OCBEN (bits<13:9>) are implemented in the MCCP9 module only.

NOTES:

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REGISTER 29-3: PMD3: PERIPHERAL MODULE DISABLE 3 CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PMPMD
bit 15							bit 8

R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0
CRCMD	—	QEI2MD	—	U3MD	I2C3MD	I2C2MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **PMPMD:** PMP Module Disable bit
1 = PMP module is disabled
0 = PMP module is enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **QEI2MD:** QEI2 Module Disable bit
1 = QEI2 module is disabled
0 = QEI2 module is enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **U3MD:** UART3 Module Disable bit
1 = UART3 module is disabled
0 = UART3 module is enabled

bit 2 **I2C3MD:** I2C3 Module Disable bit
1 = I2C3 module is disabled
0 = I2C3 module is enabled

bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled

bit 0 **Unimplemented:** Read as '0'

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REGISTER 30-5: FOSC CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	U-1	R/PO-1
—	—	—	XTBST	XTCFG1	XTCFG0	—	PLLKEN(1)
bit 15							bit 8

R/PO-1	R/PO-1	U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	—	—	—	OSCIOFNC	POSCMD1	POSCMD0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-13 **Unimplemented:** Read as '1'

bit 12 **XTBST:** Oscillator Kick-Start Programmability bit
1 = Boosts the kick-start
0 = Default kick-start

bit 11-10 **XTCFG<1:0>:** Crystal Oscillator Drive Select bits
Current gain programmability for oscillator (output drive).
11 = Gain3 (use for 24-32 MHz crystals)
10 = Gain2 (use for 16-24 MHz crystals)
01 = Gain1 (use for 8-16 MHz crystals)
00 = Gain0 (use for 4-8 MHz crystals)

bit 9 **Unimplemented:** Read as '1'

bit 8 **PLLKEN:** PLL Lock Status Control bit(1)
1 = PLL lock signal will be used to disable PLL clock output if lock is lost
0 = PLL lock signal is not used; the PLL clock output will not be disabled if lock is lost

bit 7-6 **FCKSM<1:0>:** Clock Switching Mode bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5-3 **Unimplemented:** Read as '1'

bit 2 **OSCIOFNC:** OSCO Pin Function bit (except in XT and HS modes)
1 = OSCO is the clock output
0 = OSCO is the general purpose digital I/O pin

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode Select bits
11 = Primary Oscillator is disabled
10 = HS Crystal Oscillator mode (10 MHz-32 MHz)
01 = XT Crystal Oscillator mode (3.5 MHz-10 MHz)
00 = EC (External Clock) mode

Note 1: A time-out period will occur when the system clock switching logic requests the PLL clock source and the PLL is not already enabled.

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
20	CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO,Sleep
21	COM	COM	f	f = $\bar{f}$	1	1	N,Z
		COM	f,WREG	WREG = $\bar{f}$	1	1	N,Z
		COM	Ws,Wd	Wd = $\overline{Ws}$	1	1	N,Z
22	CP	CP	f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP	Wb,#lit8	Compare Wb with lit8	1	1	C,DC,N,OV,Z
		CP	Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
23	CP0	CP0	f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0	Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
24	CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,#lit8	Compare Wb with lit8, with Borrow	1	1	C,DC,N,OV,Z
		CPB	Wb,Ws	Compare Wb with Ws, with Borrow (Wb – Ws – $\overline{C}$)	1	1	C,DC,N,OV,Z
25	CPSEQ	CPSEQ	Wb,Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ	Wb,Wn,Expr	Compare Wb with Wn, Branch if =	1	1 (5)	None
26	CPSGT	CPSGT	Wb,Wn	Compare Wb with Wn, Skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT	Wb,Wn,Expr	Compare Wb with Wn, Branch if >	1	1 (5)	None
27	CPSLT	CPSLT	Wb,Wn	Compare Wb with Wn, Skip if <	1	1 (2 or 3)	None
		CPBLT	Wb,Wn,Expr	Compare Wb with Wn, Branch if <	1	1 (5)	None
28	CPSNE	CPSNE	Wb,Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None
		CPBNE	Wb,Wn,Expr	Compare Wb with Wn, Branch if ≠	1	1 (5)	None
29	CTXTSWP	CTXTSWP	#1it3	Switch CPU Register Context to Context Defined by lit3	1	2	None
30	CTXTSWP	CTXTSWP	Wn	Switch CPU Register Context to Context Defined by Wn	1	2	None
31	DAW.B	DAW.B	Wn	Wn = Decimal Adjust Wn	1	1	C
32	DEC	DEC	f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
33	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
34	DISI	DISI	#lit14	Disable Interrupts for k Instruction Cycles	1	1	None
35	DIVF	DIVF	Wm,Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
36	DIV.S(2)	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
37	DIV.U(2)	DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
38	DIVF2(2)	DIVF2	Wm,Wn	Signed 16/16-bit Fractional Divide (W1:W0 preserved)	1	6	N,Z,C,OV
39	DIV2.S(2)	DIV2.S	Wm,Wn	Signed 16/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
		DIV2.SD	Wm,Wn	Signed 32/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
40	DIV2.U(2)	DIV2.U	Wm,Wn	Unsigned 16/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
		DIV2.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide (W1:W0 preserved)	1	6	N,Z,C,OV
41	DO	DO	#lit15,Expr	Do Code to PC + Expr, lit15 + 1 Times	2	2	None
		DO	Wn,Expr	Do code to PC + Expr, (Wn) + 1 Times	2	2	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

2: The divide instructions must be preceded with a "REPEAT #5" instruction, such that they are executed six consecutive times.

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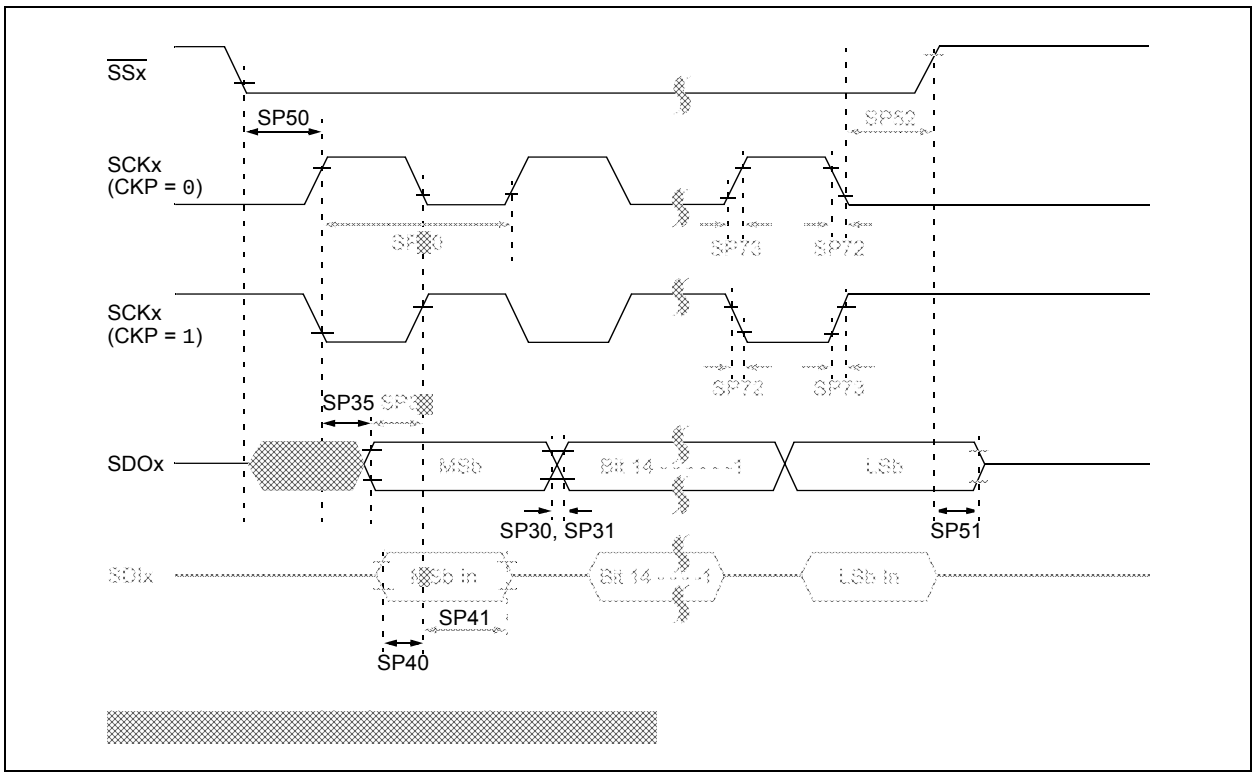
FIGURE 33-11: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 0) TIMING CHARACTERISTICS



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