Microchip Technology - DSPIC33CK32MP505T-I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck32mp505t-i-pt

3.4.3 CPU CONTROL REGISTERS

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA(3)	SB(3)	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(2)	R/W-0(2)	R/W-0(2)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(1)	IPL1(1)	IPL0(1)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(3)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(3)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulator A or B has overflowed
0 = Neither Accumulator A or B has overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulator A or B is saturated or has been saturated at some time
0 = Neither Accumulator A or B is saturated

bit 9 **DA:** DO Loop Active bit
1 = DO loop is in progress
0 = DO loop is not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33E/PIC24E Program Memory"** (DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33CK256MP508 family architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

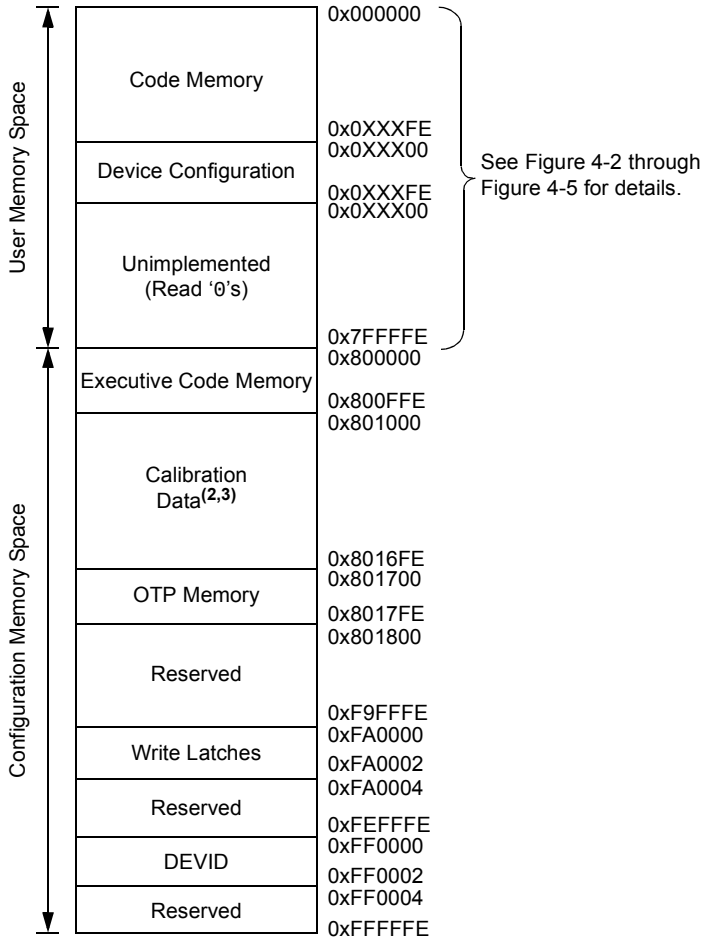
4.1 Program Address Space

The program address memory space of the dsPIC33CK256MP508 family devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.4.5 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to permit access to calibration data and Device ID sections of the configuration memory space.

The program memory maps for dsPIC33CK256MP508 devices are shown in Figure 4-1 through Figure 4-5.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33CKXXXMP50X/20X DEVICES(1)



Note 1: Memory areas are not shown to scale.
2: Calibration data area must be maintained during programming.
3: Calibration data area includes UDID, ICSP™ Write Inhibit and FBOOT registers locations.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0(1)	R/W-0(1)	R/W-0(1)	R/W-0	R/C-0	R-0	R/W-0	R/C-0
WR	WREN	WRERR	NVMSIDL(2)	SFTSWP	P2ACTIV	RPDF	URERR
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	—	—	—	NVMOP3(3,4)	NVMOP2(3,4)	NVMOP1(3,4)	NVMOP0(3,4)
bit 7							bit 0

Legend:	C = Clearable bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle Control bit(2)
- 1 = Flash voltage regulator goes into Standby mode during Idle mode
- 0 = Flash voltage regulator is active during Idle mode

bit 11 **SFTSWP:** Partition Soft Swap Status bit
- 1 = Partitions have been successfully swapped using the BOOTSWP instruction (soft swap)
- 0 = Awaiting successful partition swap using the BOOTSWP instruction or a device Reset will determine the Active Partition based on the FBTSEQ register

bit 10 **P2ACTIV:** Partition 2 Active Status bit
- 1 = Partition 2 Flash is mapped into the active region
- 0 = Partition 1 Flash is mapped into the active region

bit 9 **RPDF:** Row Programming Data Format bit
- 1 = Row data to be stored in RAM is in compressed format
- 0 = Row data to be stored in RAM is in uncompressed format

bit 8 **URERR:** Row Programming Data Underrun Error bit
- 1 = Indicates row programming operation has been terminated
- 0 = No data underrun error is detected

bit 7-4 **Unimplemented:** Read as '0'

Note 1: These bits can only be reset on a POR.

2: If this bit is set, there will be minimal power savings (I_{IDLE}), and upon exiting Idle mode, there is a delay (T_{VREG}) before Flash memory becomes operational.

3: All other combinations of NVMOP<3:0> are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

TABLE 8-4: REMAPPABLE PIN INPUTS (CONTINUED)

RPINRx<15:8> or RPINRx<7:0>	Function	Available on Ports
63	RP63	Port Pin RC15
64	RP64	Port Pin RD0
65	RP65	Port Pin RD1
66	RP66	Port Pin RD2
67	RP67	Port Pin RD3
68	RP68	Port Pin RD4
69	RP69	Port Pin RD5
70	RP70	Port Pin RD6
71	RP71	Port Pin RD7
72	RP72	Port Pin RD8
73	RP73	Port Pin RD9
74	RP74	Port Pin RD10
75	RP75	Port Pin RD11
76	RP76	Port Pin RD12
77	RP77	Port Pin RD13
78	RP78	Port Pin RD14
79	RP79	Port Pin RD15
80-175	RP80-RP175	Reserved
176	RP176	Virtual RPV0
177	RP177	Virtual RPV1
178	RP178	Virtual RPV2
179	RP179	Virtual RPV3
180	RP180	Virtual RPV4
181	RP181	Virtual RPV5

8.5.5 VIRTUAL CONNECTIONS

The dsPIC33CK256MP508 devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

REGISTER 8-68: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP61R5	RP61R4	RP61R3	RP61R2	RP61R1	RP61R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP60R5	RP60R4	RP60R3	RP60R2	RP60R1	RP60R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP61R<5:0>:** Peripheral Output Function is Assigned to RP61 Output Pin bits (see Table 8-7 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP60R<5:0>:** Peripheral Output Function is Assigned to RP60 Output Pin bits (see Table 8-7 for peripheral function numbers)

REGISTER 8-69: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP63R5	RP63R4	RP63R3	RP63R2	RP63R1	RP63R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP62R5	RP62R4	RP62R3	RP62R2	RP62R1	RP62R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP63R<5:0>:** Peripheral Output Function is Assigned to RP63 Output Pin bits (see Table 8-7 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP62R<5:0>:** Peripheral Output Function is Assigned to RP62 Output Pin bits (see Table 8-7 for peripheral function numbers)

TABLE 8-13: PPS INPUT CONTROL REGISTERS

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RPCON	—	—	—	—	IOLOCK	—	—	—	—	—	—	—	—	—	—	—
RPINR0	INT1R7	INT1R6	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0	—	—	—	—	—	—	—	—
RPINR1	INT3R7	INT3R6	INT3R5	INT3R4	INT3R3	INT3R2	INT3R1	INT3R0	INT2R7	INT2R6	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
RPINR2	T1CKR7	T1CKR6	T1CKR5	T1CKR4	T1CKR3	T1CKR2	T1CKR1	T1CKR0	—	—	—	—	—	—	—	—
RPINR3	ICM1R7	ICM1R6	ICM1R5	ICM1R4	ICM1R3	ICM1R2	ICM1R1	ICM1R0	TCKI1R7	TCKI1R6	TCKI1R5	TCKI1R4	TCKI1R3	TCKI1R2	TCKI1R1	TCKI1R0
RPINR4	ICM2R7	ICM2R6	ICM2R5	ICM2R4	ICM2R3	ICM2R2	ICM2R1	ICM2R0	TCKI2R7	TCKI2R6	TCKI2R5	TCKI2R4	TCKI2R3	TCKI2R2	TCKI2R1	TCKI2R0
RPINR5	ICM3R7	ICM3R6	ICM3R5	ICM3R4	ICM3R3	ICM3R2	ICM3R1	ICM3R0	TCKI3R7	TCKI3R6	TCKI3R5	TCKI3R4	TCKI3R3	TCKI3R2	TCKI3R1	TCKI3R0
RPINR6	ICM4R7	ICM4R6	ICM4R5	ICM4R4	ICM4R3	ICM4R2	ICM4R1	ICM4R0	TCKI4R7	TCKI4R	TCKI4R5	TCKI4R4	TCKI4R3	TCKI4R2	TCKI4R1	TCKI4R0
RPINR7	ICM5R7	ICM5R6	ICM5R5	ICM5R4	ICM5R3	ICM5R2	ICM5R1	ICM5R0	TCKI5R7	TCKI5R6	TCKI5R5	TCKI5R4	TCKI5R3	TCKI5R2	TCKI5R1	TCKI5R0
RPINR8	ICM6R7	ICM6R6	ICM6R5	ICM6R4	ICM6R3	ICM6R2	ICM6R1	ICM6R0	TCKI6R7	TCKI6R6	TCKI6R5	TCKI6R4	TCKI6R3	TCKI6R2	TCKI6R1	TCKI6R0
RPINR9	ICM7R7	ICM7R6	ICM7R5	ICM7R4	ICM7R3	ICM7R2	ICM7R1	ICM7R0	TCKI7R7	TCKI7R6	TCKI7R5	TCKI7R4	TCKI7R3	TCKI7R2	TCKI7R1	TCKI7R0
RPINR10	ICM8R7	ICM8R6	ICM8R5	ICM8R4	ICM8R3	ICM8R2	ICM8R1	ICM8R0	TCKI8R7	TCKI8R6	TCKI8R5	TCKI8R4	TCKI8R3	TCKI8R2	TCKI8R1	TCKI8R0
RPINR11	OCFBR7	OCFBR6	OCFBR5	OCFBR4	OCFBR3	OCFBR2	OCFBR1	OCFBR0	OCFAR7	OCFAR6	OCFAR5	OCFAR4	OCFAR3	OCFAR2	OCFAR1	OCFAR0
RPINR12	PCI9R7	PCI9R6	PCI9R5	PCI9R4	PCI9R3	PCI9R2	PCI9R1	PCI9R0	PCI8R7	PCI8R6	PCI8R5	PCI8R4	PCI8R3	PCI8R2	PCI8R1	PCI8R0
RPINR13	PCI11R7	PCI11R6	PCI11R5	PCI11R4	PCI11R3	PCI11R2	PCI11R1	PCI11R0	PCI10R7	PCI10R6	PCI10R5	PCI10R4	PCI10R3	PCI10R2	PCI10R1	PCI10R0
RPINR14	QEIB1R7	QEIB1R6	QEIB1R5	QEIB1R4	QEIB1R3	QEIB1R2	QEIB1R1	QEIB1R0	QEIA1R7	QEIA1R6	QEIA1R5	QEIA1R4	QEIA1R3	QEIA1R2	QEIA1R1	QEIA1R0
RPINR15	QEIHOM1R7	QEIHOM1R6	QEIHOM1R5	QEIHOM1R4	QEIHOM1R3	QEIHOM1R2	QEIHOM1R1	QEIHOM1R0	QEINDX1R7	QEINDX1R6	QEINDX1R5	QEINDX1R4	QEINDX1R3	QEINDX1R2	QEINDX1R1	QEINDX1R0
RPINR16	QEIB2R7	QEIB2R6	QEIB2R5	QEIB2R4	QEIB2R3	QEIB2R2	QEIB2R1	QEIB2R0	QEIA2R7	QEIA2R6	QEIA2R5	QEIA2R4	QEIA2R3	QEIA2R2	QEIA2R1	QEIA2R0
RPINR17	QEIHOM2R7	QEIHOM2R6	QEIHOM2R5	QEIHOM2R4	QEIHOM2R3	QEIHOM2R2	QEIHOM2R1	QEIHOM2R0	QEINDX2R7	QEINDX2R6	QEINDX2R5	QEINDX2R4	QEINDX2R3	QEINDX2R2	QEINDX2R1	QEINDX2R0
RPINR18	U1DSRR7	U1DSRR6	U1DSRR5	U1DSRR4	U1DSRR3	U1DSRR2	U1DSRR1	U1DSRR0	U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
RPINR19	U2DSRR7	U2DSRR6	U2DSRR5	U2DSRR4	U2DSRR3	U2DSRR2	U2DSRR1	U2DSRR0	U2RXR7	U2RXR6	U2RXR5	U2RXR4	U2RXR3	U2RXR2	U2RXR1	U2RXR0
RPINR20	SCK1R7	SCK1R6	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0	SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
RPINR21	REFOIR7	REFOIR6	REFOIR5	REFOIR4	REFOIR3	REFOIR2	REFOIR1	REFOIR0	SS1R7	SS1R6	SS1R5	SS1R4	SS1R3	SS1R2	SS1R1	SS1R0
RPINR22	SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0	SDI2R7	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
RPINR23	—	—	—	—	—	—	—	—	SS2R7	SS2R6	SS2R5	SS2R4	SS2R3	SS2R2	SS2R1	SS2R0
RPINR26	—	—	—	—	—	—	—	—	CAN1RXR7	CAN1RXR6	CAN1RXR5	CAN1RXR4	CAN1RXR3	CAN1RXR2	CAN1RXR1	CAN1RXR0
RPINR27	U3DSRR7	U3DSRR6	U3DSRR5	U3DSRR4	U3DSRR3	U3DSRR2	U3DSRR1	U3DSRR0	U3RXR7	U3RXR6	U3RXR5	U3RXR4	U3RXR3	U3RXR2	U3RXR1	U3RXR0
RPINR29	SCK3R7	SCK3R6	SCK3R5	SCK3R4	SCK3R3	SCK3R2	SCK3R1	SCK3R0	SDI3R7	SDI3R6	SDI3R5	SDI3R4	SDI3R3	SDI3R2	SDI3R1	SDI3R0
RPINR30	—	—	—	—	—	—	—	—	SS3R7	SS3R6	SS3R5	SS3R4	SS3R3	SS3R2	SS3R1	SS3R0
RPINR32	TCKI9R7	TCKI9R6	TCKI9R5	TCKI9R4	TCKI9R3	TCKI9R2	TCKI9R1	TCKI9R0	—	—	—	—	—	—	—	—
RPINR33	—	—	—	—	—	—	—	—	ICM9R7	ICM9R6	ICM9R5	ICM9R4	ICM9R3	ICM9R2	ICM9R1	ICM9R0
RPINR37	PCI17R7	PCI17R6	PCI17R5	PCI17R4	PCI17R3	PCI17R2	PCI17R1	PCI17R0	OCFCR7	OCFCR6	OCFCR5	OCFCR4	OCFCR3	OCFCR2	OCFCR1	OCFCR0
RPINR38	—	—	—	—	—	—	—	—	PCI18R7	PCI18R6	PCI18R5	PCI18R4	PCI18R3	PCI18R2	PCI18R1	PCI18R0
RPINR42	PCI13R7	PCI13R6	PCI13R5	PCI13R4	PCI13R3	PCI13R2	PCI13R1	PCI13R0	PCI12R7	PCI12R6	PCI12R5	PCI12R4	PCI12R3	PCI12R2	PCI12R1	PCI12R0
RPINR43	PCI15R7	PCI15R6	PCI15R5	PCI15R4	PCI15R3	PCI15R2	PCI15R1	PCI15R0	PCI14R7	PCI14R6	PCI14R5	PCI14R4	PCI14R3	PCI14R2	PCI14R1	PCI14R0
RPINR44	SENT1R7	SENT1R6	SENT1R5	SENT1R4	SENT1R3	SENT1R2	SENT1R1	SENT1R0	PCI16R7	PCI16R6	PCI16R5	PCI16R4	PCI16R3	PCI16R2	PCI16R1	PCI16R0
RPINR45	CLCINAR7	CLCINAR6	CLCINAR5	CLCINAR4	CLCINAR3	CLCINAR2	CLCINAR1	CLCINAR0	SENT2R7	SENT2R6	SENT2R5	SENT2R4	SENT2R3	SENT2R2	SENT2R1	SENT2R0
RPINR46	CLCINCR7	CLCINCR6	CLCINCR5	CLCINCR4	CLCINCR3	CLCINCR2	CLCINCR1	CLCINCR0	CLCINBR7	CLCINBR6	CLCINBR5	CLCINBR4	CLCINBR3	CLCINBR2	CLCINBR1	CLCINBR0
RPINR47	ADCTRGR7	ADCTRGR6	ADCTRGR5	ADCTRGR4	ADCTRGR3	ADCTRGR2	ADCTRGR1	ADCTRGR0	CLCINDR7	CLCINDR6	CLCINDR5	CLCINDR4	CLCINDR3	CLCINDR2	CLCINDR1	CLCINDR0
RPINR48	U1CTSR7	U1CTSR6	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0	OCFDR7	OCFDR6	OCFDR5	OCFDR4	OCFDR3	OCFDR2	OCFDR1	OCFDR0
RPINR49	U3CTSR7	U3CTSR6	U3CTSR5	U3CTSR4	U3CTSR3	U3CTSR2	U3CTSR1	U3CTSR0	U2CTSR7	U2CTSR6	U2CTSR5	U2CTSR4	U2CTSR3	U2CTSR2	U2CTSR1	U2CTSR0

REGISTER 11-7: C1TDCH: CAN TRANSMITTER DELAY COMPENSATION REGISTER HIGH(1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	EDGFLTEN	SID11EN
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	TDCMOD1	TDCMOD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **EDGFLTEN:** Enable Edge Filtering During Bus Integration State bit
1 = Edge filtering is enabled according to ISO11898-1:2015
0 = Edge filtering is disabled

bit 8 **SID11EN:** Enable 12-Bit SID in CAN FD Base Format Messages bit
1 = RRS is used as SID11 in CAN FD base format messages: SID<11:0> = {SID<10:0>, SID11}
0 = Does not use RRS; SID<10:0>

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **TDCMOD<1:0>:** Transmitter Delay Compensation Mode bits (Secondary Sample Point (SSP))
10-11 = Auto: Measures delay and adds TSEG1<4:0> (C1DBTCFGH<4:0>), adds TDCO<6:0>
01 = Manual: Does not measure, uses TDCV<5:0> + TDCO<6:0> from register
00 = Disable

Note 1: This register can only be modified in Configuration mode (OPMOD<2:0> = 100).

REGISTER 13-4: ADCON2H: ADC CONTROL REGISTER 2 HIGH

R-0, HSC	R-0, HSC	U-0	r-0	r-0	r-0	R/W-0	R/W-0
REFRDY	REFERR	—	—	—	—	SHRSAMC9	SHRSAMC8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SHRSAMC7	SHRSAMC6	SHRSAMC5	SHRSAMC4	SHRSAMC3	SHRSAMC2	SHRSAMC1	SHRSAMC0
bit 7							bit 0

Legend:	r = Reserved bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **REFRDY:** Band Gap and Reference Voltage Ready Flag bit
1 = Band gap is ready
0 = Band gap is not ready

bit 14 **REFERR:** Band Gap or Reference Voltage Error Flag bit
1 = Band gap was removed after the ADC module was enabled (ADON = 1)
0 = No band gap error was detected

bit 13 **Unimplemented:** Read as '0'

bit 12-10 **Reserved:** Maintain as '0'

bit 9-0 **SHRSAMC<9:0>:** Shared ADC Core Sample Time Selection bits
These bits specify the number of shared ADC Core Clock Periods (TADCORE) for the shared ADC core sample time.
1111111111 = 1025 TADCORE
...
0000000001 = 3 TADCORE
0000000000 = 2 TADCORE

REGISTER 13-27: ADTRIGnL/ADTRIGnH: ADC CHANNEL TRIGGER n(x) SELECTION REGISTERS LOW AND HIGH (x = 0 TO 25; n = 0 TO 6) (CONTINUED)

bit 4-0 **TRGSRCx<4:0>:** Common Interrupt Enable for Corresponding Analog Inputs bits (TRGSRC0 to TRGSRC24 – Even)

11111 = ADTRG31 (PPS input)
11110 = PTG
11101 = CLC2
11100 = CLC1
11011 = MCCP9
11010 = SCCP7
11001 = SCCP6
11000 = SCCP5
10111 = SCCP4
10110 = SCCP3
10101 = SCCP2
10100 = SCCP1
10011 = PWM8 Trigger 2
10010 = PWM8 Trigger 1
10001 = PWM7 Trigger 2
10000 = PWM7 Trigger 1
01111 = PWM6 Trigger 2
01110 = PWM6 Trigger 1
01101 = PWM5 Trigger 2
01100 = PWM5 Trigger 1
01011 = PWM4 Trigger 2
01010 = PWM4 Trigger 1
01001 = PWM3 Trigger 2
01000 = PWM3 Trigger 1
00111 = PWM2 Trigger 2
00110 = PWM2 Trigger 1
00101 = PWM1 Trigger 2
00100 = PWM1 Trigger 1
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

14.2 Features Overview

- Three Rail-to-Rail Analog Comparators
- Up to Four Selectable Input Sources per Comparator
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Interrupt Generation Capability
- Dedicated Pulse Density Modulation DAC for each Analog Comparator:
  - PDM unit followed by a digitally controlled multimode multipole RC filter
- Multimode Multipole RC Output Filter:
  - Transition mode: Provides the fastest response
  - Fast mode: For tracking DAC slopes
  - Steady-State mode: Provides 12-bit resolution
- Slope Compensation along with each DAC:
  - Slope Generation mode
  - Hysteretic Control mode
  - Triangle Wave mode
- Functional Support for the High-Speed PWM module which Includes:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

14.3 Control Registers

The DACCTRL1L and DACCTRL2H/L registers are common configuration registers for DAC modules.

The DACxCON, DACxDAT, SLPxCON and SLPxDAT registers specify the operation of individual modules.

Table 15-1 shows the truth table that describes how the Quadrature signals are decoded.

TABLE 15-1: TRUTH TABLE FOR QUADRATURE ENCODER

Current Quadrature State		Previous Quadrature State		Action
QEA	QEB	QEA	QEB	
1	1	1	1	No count or direction change
1	1	1	0	Count up
1	1	0	1	Count down
1	1	0	0	Invalid state change; ignore
1	0	1	1	Count down
1	0	1	0	No count or direction change
1	0	0	1	Invalid state change; ignore
1	0	0	0	Count up
0	1	1	1	Count up
0	1	1	0	Invalid state change; ignore
0	1	0	1	No count or direction change
0	1	0	0	Count down
0	0	1	1	Invalid state change; ignore
0	0	1	0	Count down
0	0	0	1	Count up
0	0	0	0	No count or direction change

Figure 15-2 illustrates the simplified block diagram of the QEI module. The QEI module consists of decoder logic to interpret the Phase A (QEAx) and Phase B (QEBx) signals, and an up/down counter to accumulate the count. The counter pulses are generated when the Quadrature state changes. The count direction information must be maintained in a register until a direction change is detected. The module also includes digital noise filters, which condition the input signal.

The QEI module consists of the following major features:

- Four Input Pins: Two Phase Signals, an Index Pulse and a Home Pulse
- Programmable Digital Noise Filters on Inputs
- Quadrature Decoder providing Counter Pulses and Count Direction
- Count Direction Status
- 4x Count Resolution
- Index (INDXx) Pulse to Reset the Position Counter
- General Purpose 32-Bit Timer/Counter mode
- Interrupts generated by QEI or Counter Events
- 32-Bit Velocity Counter
- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 32-Bit Position Initialization/Capture Register
- 32-Bit Compare Less Than and Greater Than Registers
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Interval Timer mode

15.1 QEI Control and Status Registers

REGISTER 15-1: QEIxCON: QEIx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIEN	—	QEISIDL	PIMOD2(1,5)	PIMOD1(1,5)	PIMOD0(1,5)	IMV1(2)	IMV0(2)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2(3)	INTDIV1(3)	INTDIV0(3)	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **QEIEN:** Quadrature Encoder Interface Module Enable bit
1 = Module counters are enabled
0 = Module counters are disabled, but SFRs can be read or written

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** QEI Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits(1,5)
111 = Modulo Count mode for position counter and every Index event resets the position counter(4)
110 = Modulo Count mode for position counter
101 = Resets the position counter when the position counter equals the QEIxGEC register
100 = Second Index event after Home event initializes position counter with contents of QEIxIC register
011 = First Index event after Home event initializes position counter with contents of QEIxIC register
010 = Next Index input event initializes the position counter with contents of QEIxIC register
001 = Every Index input event resets the position counter
000 = Index input event does not affect the position counter

bit 9-8 **IMV<1:0>:** Index Match Value bits(2)
11 = Index match occurs when QEBx = 1 and QEAx = 1
10 = Index match occurs when QEBx = 1 and QEAx = 0
01 = Index match occurs when QEBx = 0 and QEAx = 1
00 = Index match occurs when QEBx = 0 and QEAx = 0

bit 7 **Unimplemented:** Read as '0'

Note 1: When CCMx = 10 or CCMx = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCMx = 00, and QEAx and QEBx values match the Index Match Value (IMV), the POSxCNTH and POSxCNTL registers are reset.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

4: Not all devices support this mode.

5: The QCAPEN and HCAPEN bits must be cleared during PIMODx Modes 2 through 7 to ensure proper functionality. Not all devices support HCAPEN.

REGISTER 17-2: SPIxCON1H: SPIx CONTROL REGISTER 1 HIGH (CONTINUED)

bit 6 **FRMSYNC:** Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (Slave)
0 = Frame Sync pulse output (Master)

bit 5 **FRMPOL:** Frame Sync/Slave Select Polarity bit
1 = Frame Sync pulse/Slave select is active-high
0 = Frame Sync pulse/Slave select is active-low

bit 4 **MSSEN:** Master Mode Slave Select Enable bit
1 = SPIx Slave select support is enabled with polarity determined by FRMPOL ($\overline{SSx}$ pin is automatically driven during transmission in Master mode)
0 = Slave select SPIx support is disabled ($\overline{SSx}$ pin will be controlled by port I/O)

bit 3 **FRMSYPW:** Frame Sync Pulse-Width bit
1 = Frame Sync pulse is one serial word length wide (as defined by MODE<32,16>/WLENGTH<4:0>)
0 = Frame Sync pulse is one clock (SCKx) wide

bit 2-0 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits
Controls the number of serial words transmitted per Sync pulse.
111 = Reserved
110 = Reserved
101 = Generates a Frame Sync pulse on every 32 serial words
100 = Generates a Frame Sync pulse on every 16 serial words
011 = Generates a Frame Sync pulse on every 8 serial words
010 = Generates a Frame Sync pulse on every 4 serial words
001 = Generates a Frame Sync pulse on every 2 serial words (value used by audio protocols)
000 = Generates a Frame Sync pulse on each serial word

Note 1: AUDEN can only be written when the SPIEN bit = 0.
2: AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3: URDTEN is only valid when IGNTUR = 1.
4: AUDMOD<1:0> can only be written when the SPIEN bit = 0 and is only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER (CONTINUED)

bit 0 **SYNCTXEN:** SENTx Synchronization Period Status/Transmit Enable bit(1)

Module in Receive Mode (RCVEN = 1):

1 = A valid synchronization period was detected; the module is receiving nibble data

0 = No synchronization period has been detected; the module is not receiving nibble data

Module in Asynchronous Transmit Mode (RCVEN = 0, TXM = 0):

The bit always reads as '1' when the module is enabled, indicating the module transmits SENTx data frames continuously. The bit reads '0' when the module is disabled.

Module in Synchronous Transmit Mode (RCVEN = 0, TXM = 1):

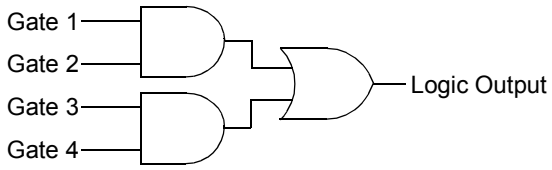
1 = The module is transmitting a SENTx data frame

0 = The module is not transmitting a data frame, user software may set SYNCTXEN to start another data frame transmission

Note 1: In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

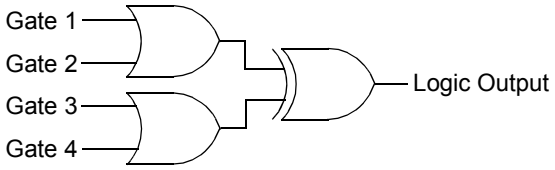
FIGURE 23-2: CLCx LOGIC FUNCTION COMBINATORIAL OPTIONS

AND – OR



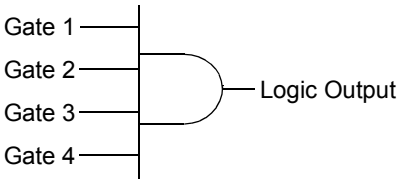
MODE<2:0> = 000

OR – XOR



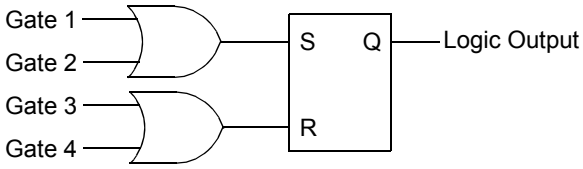
MODE<2:0> = 001

4-Input AND



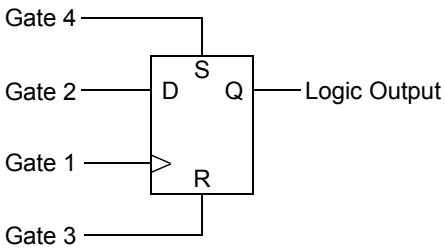
MODE<2:0> = 010

S-R Latch



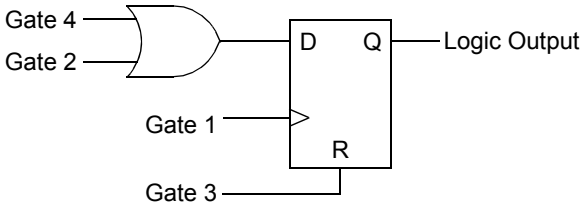
MODE<2:0> = 011

1-Input D Flip-Flop with S and R



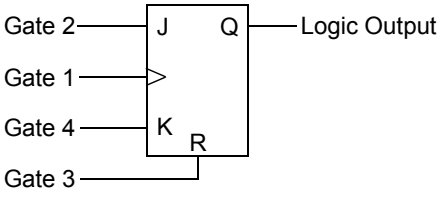
MODE<2:0> = 100

2-Input D Flip-Flop with R



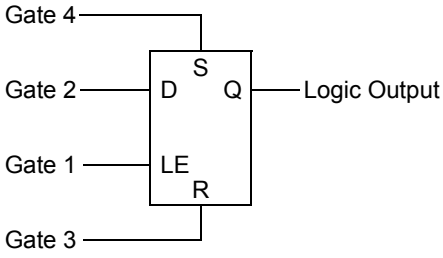
MODE<2:0> = 101

J-K Flip-Flop with R



MODE<2:0> = 110

1-Input Transparent Latch with S and R



MODE<2:0> = 111

REGISTER 23-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = Data Source 2 signal is enabled for Gate 1
0 = Data Source 2 signal is disabled for Gate 1

bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 1
0 = Data Source 2 inverted signal is disabled for Gate 1

bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = Data Source 1 signal is enabled for Gate 1
0 = Data Source 1 signal is disabled for Gate 1

bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 1
0 = Data Source 1 inverted signal is disabled for Gate 1

27.1 Operational Amplifier Control Registers

REGISTER 27-1: AMPCON1L: OP AMP CONTROL REGISTER LOW

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
AMPON	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	AMPEN3	AMPEN2	AMPEN1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AMPON:** Op Amp Enable/On bit
1 = Enables op amp modules if their respective AMPENx bits are also asserted
0 = Disables all op amp modules

bit 14-3 **Unimplemented:** Read as '0'

bit 2 **AMPEN3:** Op Amp #3 Enable bit
1 = Enables Op Amp #3 if the AMPON bit is also asserted
0 = Disables Op Amp #3

bit 1 **AMPEN2:** Op Amp #2 Enable bit
1 = Enables Op Amp #2 if the AMPON bit is also asserted
0 = Disables Op Amp #2

bit 0 **AMPEN1:** Op Amp #1 Enable bit
1 = Enables Op Amp #1 if the AMPON bit is also asserted
0 = Disables Op Amp #1

REGISTER 29-6: PMD7: PERIPHERAL MODULE DISABLE 7 CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	PTGMD	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMP3MD:** Comparator 3 Module Disable bit
1 = Comparator 3 module is disabled
0 = Comparator 3 module is enabled

bit 9 **CMP2MD:** Comparator 2 Module Disable bit
1 = Comparator 2 module is disabled
0 = Comparator 2 module is enabled

bit 8 **CMP1MD:** Comparator 1 Module Disable bit
1 = Comparator 1 module is disabled
0 = Comparator 1 module is enabled

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **PTGMD**: PTG Module Disable bit
1 = PTG module is disabled
0 = PTG module is enabled

bit 2-0 **Unimplemented:** Read as '0'

TABLE 30-4: DEVICE IDs FOR THE dsPIC33CK256MP508 FAMILY

Device	DEVID
Device IDs for dsPIC33CK256MP508 Family with CAN FD	
dsPIC33CK256MP508	0x7C74
dsPIC33CK256MP506	0x7C73
dsPIC33CK256MP505	0x7C72
dsPIC33CK256MP503	0x7C71
dsPIC33CK256MP502	0x7C70
dsPIC33CK128MP508	0x7C64
dsPIC33CK128MP506	0x7C63
dsPIC33CK128MP505	0x7C62
dsPIC33CK128MP503	0x7C61
dsPIC33CK128MP502	0x7C60
dsPIC33CK64MP508	0x7C54
dsPIC33CK64MP506	0x7C53
dsPIC33CK64MP505	0x7C52
dsPIC33CK64MP503	0x7C51
dsPIC33CK64MP502	0x7C50
dsPIC33CK32MP506	0x7C43
dsPIC33CK32MP505	0x7C42
dsPIC33CK32MP503	0x7C41
dsPIC33CK32MP502	0x7C40
Device IDs for dsPIC33CK256MP508 Family without CAN FD	
dsPIC33CK256MP208	0x7C34
dsPIC33CK256MP206	0x7C33
dsPIC33CK256MP205	0x7C32
dsPIC33CK256MP203	0x7C31
dsPIC33CK256MP202	0x7C30
dsPIC33CK128MP208	0x7C24
dsPIC33CK128MP206	0x7C23
dsPIC33CK128MP205	0x7C22
dsPIC33CK128MP203	0x7C21
dsPIC33CK128MP202	0x7C20
dsPIC33CK64MP208	0x7C14
dsPIC33CK64MP206	0x7C13
dsPIC33CK64MP205	0x7C12
dsPIC33CK64MP203	0x7C11
dsPIC33CK64MP202	0x7C10
dsPIC33CK32MP206	0x7C03
dsPIC33CK32MP205	0x7C02
dsPIC33CK32MP203	0x7C01
dsPIC33CK32MP202	0x7C00

D

E

F

