Microchip Technology - DSPIC33CK64MP508T-I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT
Number of I/O	69
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ck64mp508t-i-pt

4.4.2.3 Move and Accumulator Instructions

Move instructions, and the DSP accumulator class of instructions, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.4.2.4 MAC Instructions

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.4.2.5 Other Instructions

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

REGISTER 5-2: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Lower Write Address bits
Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

REGISTER 5-3: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADRU<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADRU<23:16>:** Nonvolatile Memory Upper Write Address bits
Selects the upper eight bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

REGISTER 8-4: LATx: OUTPUT DATA FOR PORTx REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
LATx<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
LATx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **LATx<15:0>:** PORTx Data Output Value bits

REGISTER 8-5: ODCx: OPEN-DRAIN ENABLE FOR PORTx REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ODCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ODCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **ODCx<15:0>:** PORTx Open-Drain Enable bits
1 = Open-drain is enabled on the PORTx pin
0 = Open-drain is disabled on the PORTx pin

TABLE 8-4: REMAPPABLE PIN INPUTS

RPINRx<15:8> or RPINRx<7:0>	Function	Available on Ports
0	Vss	Internal
1	Comparator 1	Internal
2	Comparator 2	Internal
3	Comparator 3	Internal
4-5	RP4-RP5	Reserved
6	PTG Trigger 26	Internal
7	PTG Trigger 27	Internal
8-10	RP8-RP10	Reserved
11	PWM Event Out C	Internal
12	PWM Event Out D	Internal
13	PWM Event Out E	Internal
14-31	RP14-RP31	Reserved
32	RP32	Port Pin RB0
33	RP33	Port Pin RB1
34	RP34	Port Pin RB2
35	RP35	Port Pin RB3
36	RP36	Port Pin RB4
37	RP37	Port Pin RB5
38	RP38	Port Pin RB6
39	RP39	Port Pin RB7
40	RP40	Port Pin RB8
41	RP41	Port Pin RB9
42	RP42	Port Pin RB10
43	RP43	Port Pin RB11
44	RP44	Port Pin RB12
45	RP45	Port Pin RB13
46	RP46	Port Pin RB14
47	RP47	Port Pin RB15
48	RP48	Port Pin RC0
49	RP49	Port Pin RC1
50	RP50	Port Pin RC2
51	RP51	Port Pin RC3
52	RP52	Port Pin RC4
53	RP53	Port Pin RC5
54	RP54	Port Pin RC6
55	RP55	Port Pin RC7
56	RP56	Port Pin RC8
57	RP57	Port Pin RC9
58	RP58	Port Pin RC10
59	RP59	Port Pin RC11
60	RP60	Port Pin RC12
61	RP61	Port Pin RC13
62	RP62	Port Pin RC14

TABLE 8-6: REMAPPABLE OUTPUT PIN REGISTERS

Register	RP Pin	I/O Port
RPOR0<5:0>	RP32	Port Pin RB0
RPOR0<13:8>	RP33	Port Pin RB1
RPOR1<5:0>	RP34	Port Pin RB2
RPOR1<13:8>	RP35	Port Pin RB3
RPOR2<5:0>	RP36	Port Pin RB4
RPOR2<13:8>	RP37	Port Pin RB5
RPOR3<5:0>	RP38	Port Pin RB6
RPOR3<13:8>	RP39	Port Pin RB7
RPOR4<5:0>	RP40	Port Pin RB8
RPOR4<13:8>	RP41	Port Pin RB9
RPOR5<5:0>	RP42	Port Pin RB10
RPOR5<13:8>	RP43	Port Pin RB11
RPOR6<5:0>	RP44	Port Pin RB12
RPOR6<13:8>	RP45	Port Pin RB13
RPOR7<5:0>	RP46	Port Pin RB14
RPOR7<13:8>	RP47	Port Pin RB15
RPOR8<5:0>	RP48	Port Pin RC0
RPOR8<13:8>	RP49	Port Pin RC1
RPOR9<5:0>	RP50	Port Pin RC2
RPOR9<13:8>	RP51	Port Pin RC3
RPOR10<5:0>	RP52	Port Pin RC4
RPOR10<13:8>	RP53	Port Pin RC5
RPOR11<5:0>	RP54	Port Pin RC6
RPOR11<13:8>	RP55	Port Pin RC7
RPOR12<5:0>	RP56	Port Pin RC8
RPOR12<13:8>	RP57	Port Pin RC9
RPOR13<5:0>	RP58	Port Pin RC10
RPOR13<13:8>	RP59	Port Pin RC11
RPOR14<5:0>	RP60	Port Pin RC12
RPOR14<13:8>	RP61	Port Pin RC13
RPOR15<5:0>	RP62	Port Pin RC14
RPOR15<13:8>	RP63	Port Pin RC15
RPOR16<5:0>	RP64	Port Pin RD0
RPOR16<13:8>	RP65	Port Pin RD1
RPOR17<5:0>	RP66	Port Pin RD2
RPOR17<13:8>	RP67	Port Pin RD3
RPOR18<5:0>	RP68	Port Pin RD4
RPOR18<13:8>	RP69	Port Pin RD5
RPOR19<5:0>	RP70	Port Pin RD6
RPOR19<13:8>	RP71	Port Pin RD7
RPOR20<5:0>	RP72	Port Pin RD8
RPOR20<13:8>	RP73	Port Pin RD9
RPOR21<5:0>	RP74	Port Pin D10
RPOR21<13:8>	RP75	Port Pin RD11
RPOR22<5:0>	RP76	Port Pin RD12
RPOR22<13:8>	RP77	Port Pin RD13

REGISTER 8-15: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT3R7	INT3R6	INT3R5	INT3R4	INT3R3	INT3R2	INT3R1	INT3R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT2R7	INT2R6	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **INT3R<7:0>:** Assign External Interrupt 3 (INT3) to the Corresponding RPn Pin bits
See Table 8-4.

bit 7-0 **INT2R<7:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits
See Table 8-4.

REGISTER 8-16: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1CKR7	T1CKR6	T1CKR5	T1CKR4	T1CKR3	T1CKR2	T1CKR1	T1CKR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **T1CKR<7:0>:** Assign Timer1 External Clock (T1CK) to the Corresponding RPn Pin bits
See Table 8-4.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 10-1: DMACON: DMA ENGINE CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DMAEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PRSSEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DMAEN:** DMA Module Enable bit
1 = Enables module
0 = Disables module and terminates all active DMA operation(s)

bit 14-1 **Unimplemented:** Read as '0'

bit 0 **PRSSEL:** Channel Priority Scheme Selection bit
1 = Round robin scheme
0 = Fixed priority scheme

REGISTER 11-16: C1INTL: CAN INTERRUPT REGISTER LOW

HS/C-0	HS/C-0	HS/C-0	HS/C-0	R-0	R-0	U-0	U-0
IVMIF(1)	WAKIF(1)	CERRIF(1)	SERRIF(1)	RXOVIF	TXATIF	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0	HS/C-0	HS/C-0	R-0	R-0
—	—	—	TEFIF	MODIF(1)	TBCIF(1)	RXIF	TXIF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IVMIF:** Invalid Message Interrupt Flag bit(1)
1 = Invalid message interrupt occurred
0 = No invalid message interrupt occurred

bit 14 **WAKIF:** Bus Wake-up Activity Interrupt Flag bit(1)
1 = Wake-up activity interrupt occurred
0 = No wake-up activity interrupt occurred

bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit(1)
1 = CAN bus error interrupt occurred
0 = No CAN bus error interrupt occurred

bit 12 **SERRIF:** System Error Interrupt Flag bit(1)
1 = System error interrupt occurred
0 = No system error interrupt occurred

bit 11 **RXOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = Receive buffer overflow interrupt occurred
0 = No receive buffer overflow interrupt occurred

bit 10 **TXATIF:** Transmit Attempt Interrupt Flag bit
1 = Transmit attempt interrupt occurred
0 = No transmit attempt Interrupt occurred

bit 9-5 **Unimplemented:** Read as '0'

bit 4 **TEFIF:** Transmit Event FIFO Interrupt Flag bit
1 = Transmit event FIFO interrupt occurred
0 = No transmit event FIFO interrupt occurred

bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit(1)
1 = CAN module mode change occurred (OPMOD<2:0> have changed to reflect REQOP<2:0>)
0 = No mode change occurred

bit 2 **TBCIF:** CAN Timer Overflow Interrupt Flag bit(1)
1 = TBC has overflowed
0 = TBC has not overflowed

bit 1 **RXIF:** Receive Object Interrupt Flag bit
1 = Receive object interrupt is pending
0 = No receive object interrupts are pending

bit 0 **TXIF:** Transmit Object Interrupt Flag bit
1 = Transmit object interrupt is pending
0 = No transmit object interrupts are pending

Note 1: C1INTL: Flags are set by hardware and cleared by application.

REGISTER 11-27: C1FIFOBAH: CAN MESSAGE MEMORY BASE ADDRESS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIFOBA<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIFOBA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOBA<31:16>:** Message Memory Base Address bits
Defines the base address for the transmit event FIFO followed by the message objects.

REGISTER 11-28: C1FIFOBAL: CAN MESSAGE MEMORY BASE ADDRESS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIFOBA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
FIFOBA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FIFOBA<15:0>:** Message Memory Base Address bits
Defines the base address for the transmit event FIFO followed by the message objects.

REGISTER 11-34: C1FIFOSTAx: CAN FIFO STATUS REGISTER x (x = 1 TO 7)

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FIFOCI4(1)	FIFOCI3(1)	FIFOCI2(1)	FIFOCI1(1)	FIFOCI0(1)
bit 15							bit 8

R-0	R-0	R-0	C/HS-0	C/HS-0	R-0	R-0	R-0
TXABT(3)	TXLARB(2)	TXERR(2)	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FIFOCI<4:0>:** FIFO Message Index bits(1)

TXEN = 1 (FIFO configured as a transmit buffer):
A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0 (FIFO configured as a receive buffer):
A read of this register will return an index to the message that the FIFO will use to save the next message.

bit 7 **TXABT:** Message Aborted Status bit(3)

1 = Message was aborted
0 = Message completed successfully

bit 6 **TXLARB:** Message Lost Arbitration Status bit(2)

1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 5 **TXERR:** Error Detected During Transmission bit(2)

1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 4 **TXATIF:** Transmit Attempts Exhausted Interrupt Pending bit

TXEN = 1 (FIFO configured as a transmit buffer):
1 = Interrupt is pending
0 = Interrupt is not pending

TXEN = 0 (FIFO configured as a receive buffer):
Unused, read as '0'.

bit 3 **RXOVIF:** Receive FIFO Overflow Interrupt Flag bit

TXEN = 1 (FIFO configured as a transmit buffer):
Unused, read as '0'.

TXEN = 0 (FIFO configured as a receive buffer):
1 = Overflow event has occurred
0 = No overflow event has occurred

Note 1: FIFOCI<4:0> gives a zero-indexed value to the message in the FIFO. If the FIFO is 4 messages deep (FSIZE<4:0> = 3), FIFOCIx will take on a value of 0 to 3, depending on the state of the FIFO.

2: These bits are updated when a message completes (or aborts) or when the FIFO is reset.

3: This bit is reset on any read of this register or when the TXQ is reset. The bits are cleared when TXREQ is set or using an SPI write.

REGISTER 13-25: ADSTATL: ADC DATA READY STATUS REGISTER LOW

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
AN<15:8>RDY							
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
AN<7:0>RDY							
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **AN<15:0>RDY:** Common Interrupt Enable for Corresponding Analog Inputs bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

REGISTER 13-26: ADSTATH: ADC DATA READY STATUS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
—	—	—	—	—	—	AN<25:24>RDY	
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
AN<23:16>RDY							
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AN<25:16>RDY:** Common Interrupt Enable for Corresponding Analog Inputs bits
1 = Channel conversion result is ready in the corresponding ADCBUFx register
0 = Channel conversion result is not ready

REGISTER 19-5: PMDOUT1: PARALLEL MASTER PORT DATA OUTPUT LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DATAOUT<15:0>:** Output Data Port bits
These bits are for 8-bit read operations in Slave mode and write operations for Dual Buffer Master mode.

REGISTER 19-6: PMDOUT2: PARALLEL MASTER PORT DATA OUTPUT HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DATAOUT<31:16>:** Output Data Port bits
These bits are for 8-bit write operations in Slave mode.

20.0 SINGLE-EDGE NIBBLE TRANSMISSION (SENT)

Note 1: This data sheet summarizes the features of this group of dsPIC33CK256MP508 family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Single-Edge Nibble Transmission (SENT) Module"** (DS70005145) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The Single-Edge Nibble Transmission (SENT) module is based on the SAE J2716, *"SENT – Single-Edge Nibble Transmission for Automotive Applications"*. The SENT protocol is a one-way, single wire time modulated serial communication, based on successive falling edges. It is intended for use in applications where high-resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU).

The SENTx module has the following major features:

- Selectable Transmit or Receive mode
- Synchronous or Asynchronous Transmit modes
- Automatic Data Rate Synchronization
- Optional Automatic Detection of CRC Errors in Receive mode
- Optional Hardware Calculation of CRC in Transmit mode
- Support for Optional Pause Pulse Period
- Data Buffering for One Message Frame
- Selectable Data Length for Transmit/Receive from 3 to 6 Nibbles
- Automatic Detection of Framing Errors

SENT protocol timing is based on a predetermined time unit, TTICK. Both the transmitter and receiver must be preconfigured for TTICK, which can vary from 3 to 90 µs. A SENT message frame starts with a Sync pulse. The purpose of the Sync pulse is to allow the receiver to calculate the data rate of the message encoded by the transmitter. The SENT specification allows messages to be validated with up to a 20% variation in TTICK. This allows for the transmitter and receiver to run from different clocks that may be inaccurate, and drift with time and temperature. The data nibbles are 4 bits in length and are encoded as the data value + 12 ticks. This yields a 0 value of 12 ticks and the maximum value, 0xF, of 27 ticks.

A SENT message consists of the following:

- A synchronization/calibration period of 56 tick times
- A status nibble of 12-27 tick times
- Up to six data nibbles of 12-27 tick times
- A CRC nibble of 12-27 tick times
- An optional pause pulse period of 12-768 tick times

Figure 20-1 shows a block diagram of the SENTx module.

Figure 20-2 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of tick times for each section.

20.2 Receive Mode

The module can be configured for receive operation by setting the RCVEN (SENTxCON1<11>) bit. The time between each falling edge is compared to SYNCMIN<15:0> (SENTxCON3<15:0>) and SYNCMAX<15:0> (SENTxCON2<15:0>), and if the measured time lies between the minimum and maximum limits, the module begins to receive data. The validated Sync time is captured in the SENTxSYNC register and the tick time is calculated. Subsequent falling edges are verified to be within the valid data width and the data is stored in the SENTxDATL/H registers. An interrupt event is generated at the completion of the message and the user software should read the SENTx Data registers before the reception of the next nibble. The equation for SYNCMIN<15:0> and SYNCMAX<15:0> is shown in Equation 20-3.

EQUATION 20-3: SYNCMIN<15:0> AND SYNCMAX<15:0> CALCULATIONS

$$T_{TICK} = T_{CLK} \bullet (TICKTIME\langle 15:0\rangle + 1)$$

$$FRAMETIME\langle 15:0\rangle = T_{TICK}/T_{FRAME}$$

$$SyncCount = 8 \times F_{RCV} \times T_{TICK}$$

$$SYNCMIN\langle 15:0\rangle = 0.8 \times SyncCount$$

$$SYNCMAX\langle 15:0\rangle = 1.2 \times SyncCount$$

$$FRAMETIME\langle 15:0\rangle \geq 122 + 27N$$

$$FRAMETIME\langle 15:0\rangle \geq 848 + 12N$$

Where:

T_{FRAME} = Total time of the message from ms

N = The number of data nibbles in message, 1-6

F_{RCV} = FCY x Prescaler

T_{CLK} = FCY/Prescaler

For TTICK = 3.0 μs and FCLK = 4 MHz, SYNCMIN<15:0> = 76.

Note: To ensure a Sync period can be identified, the value written to SYNCMIN<15:0> must be less than the value written to SYNCMAX<15:0>.

20.2.1 RECEIVE MODE CONFIGURATION

20.2.1.1 Initializing the SENTx Module

Perform the following steps to initialize the module:

1. Write RCVEN (SENTxCON1<11>) = 1 for Receive mode.
2. Write NIBCNT<2:0> (SENTxCON1<2:0>) for the desired data frame length.
3. Write CRCEN (SENTxCON1<8>) for hardware or software CRC validation.
4. Write PPP (SENTxCON1<7>) = 1 if pause pulse is present.
5. Write SENTxCON2 with the value of SYNCMAXx (Nominal Sync Period + 20%).
6. Write SENTxCON3 with the value of SYNCMINx (Nominal Sync Period – 20%).
7. Enable interrupts and set interrupt priority.
8. Set the SNTEN (SENTxCON1<15>) bit to enable the module.

The data should be read from the SENTxDATL/H registers after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt trigger.

REGISTER 22-1: CCPxCON1L: CCPx CONTROL 1 LOW REGISTERS (CONTINUED)

bit 3-0 **MOD<3:0>:** CCPx Mode Select bits

For CCSEL = 1 (Input Capture modes):

1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)

For CCSEL = 0 (Output Compare/Timer modes):

1111 = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Reserved
0110 = Reserved
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode, output functions are disabled

REGISTER 23-5: CLCxGLSH: CLCx GATE LOGIC INPUT SELECT HIGH REGISTER (CONTINUED)

bit 3 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = Data Source 2 signal is enabled for Gate 3
0 = Data Source 2 signal is disabled for Gate 3

bit 2 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 3
0 = Data Source 2 inverted signal is disabled for Gate 3

bit 1 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = Data Source 1 signal is enabled for Gate 3
0 = Data Source 1 signal is disabled for Gate 3

bit 0 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 3
0 = Data Source 1 inverted signal is disabled for Gate 3

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE LOW REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGBTE<15:0>:** PTG Broadcast Trigger Enable bits
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

Note 1: These bits are read-only when the module is executing Step commands.

REGISTER 24-4: PTGBTEH: PTG BROADCAST TRIGGER ENABLE HIGH REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGBTE<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGBTE<31:16>:** PTG Broadcast Trigger Enable bits
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

Note 1: These bits are read-only when the module is executing Step commands.

30.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33CK256MP508 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The dsPIC33CK256MP508 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

30.1 Configuration Bits

In dsPIC33CK256MP508 family devices, the Configuration Words are implemented as volatile memory. This means that configuration data will get loaded to volatile memory (from the Flash Configuration Words) each time the device is powered up. Configuration data is stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 30-1. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets. The BSEQx bits (FBTSEQ<11:0>) determine which panel is the Active Partition at start-up and the Configuration Words from that panel are loaded into the Configuration Shadow registers.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

TABLE 30-1: dsPIC33CKXXXMPX0X CONFIGURATION ADDRESSES

Register Name	Single Partition		Dual Partition, Active		Dual Partition, Inactive	
	256k	128k	256k	128k	256k	128k
FSEC(2)	0x02BF00	0x015F00	0x015F00	0x00AF00	0x415F00	0x40AF00
FBSLIM(2)	0x02BF10	0x015F10	0x015F10	0x00AF10	0x415F10	0x40AF10
FSIGN(2)	0x02BF14	0x015F14	0x015F14	0x00AF14	0x415F14	0x40AF14
FOSCSEL	0x02BF18	0x015F18	0x015F18	0x00AF18	0x415F18	0x40AF18
FOSC	0x02BF1C	0x015F1C	0x015F1C	0x00AF1C	0x415F1C	0x40AF1C
FWDT	0x02BF20	0x015F20	0x015F20	0x00AF20	0x415F20	0x40AF20
FPOR	0x02BF24	0x015F24	0x015F24	0x00AF24	0x415F24	0x40AF24
FICD	0x02BF28	0x015F28	0x015F28	0x00AF28	0x415F28	0x40AF28
FDMTIVTL	0x02BF2C	0x015F2C	0x015F2C	0x00AF2C	0x415F2C	0x40AF2C
FDMTIVTH	0x02BF30	0x015F30	0x015F30	0x00AF30	0x415F30	0x40AF30
FDMTCNTL	0x02BF34	0x015F34	0x015F34	0x00AF34	0x415F34	0x40AF34
FDMTCNTH	0x02BF38	0x015F38	0x015F38	0x00AF38	0x415F38	0x40AF38
FDMT	0x02BF3C	0x015F3C	0x015F3C	0x00AF3C	0x415F3C	0x40AF3C
FDEVOPT1	0x02BF40	0x015F40	0x015F40	0x00AF40	0x415F40	0x40AF40
FALTREG	0x02BF44	0x015F44	0x015F44	0x00AF44	0x415F44	0x40AF44
FBTSEQ	0x02BFFC	0x015FFC	0x015FFC	0x00AFFC	0x415FFC	0x40AFFC
FBOOT(1)	0x801800					

Note 1: FBOOT resides in calibration memory space.

2: Changes to the Inactive Partition Configuration Words affect how the Active Partition accesses the Inactive Partition.

TABLE 30-2: dsPIC33CKXXMPX0X CONFIGURATION ADDRESSES

Register Name	Single Partition		Dual Partition, Active		Dual Partition, Inactive	
	64k	32k	64k	32k	64k	32k
FSEC(2)	0x00AF00	0x005F00	0x005F00	0x002F00	0x405F00	0x402F00
FBSLIM(2)	0x00AF10	0x005F10	0x005F10	0x002F10	0x405F10	0x402F10
FSIGN(2)	0x00AF14	0x005F14	0x005F14	0x002F14	0x405F14	0x402F14
FOSCSEL	0x00AF18	0x005F18	0x005F18	0x002F18	0x405F18	0x402F18
FOSC	0x00AF1C	0x005F1C	0x005F1C	0x002F1C	0x405F1C	0x402F1C
FWDT	0x00AF20	0x005F20	0x005F20	0x002F20	0x405F20	0x402F20
FPOR	0x00AF24	0x005F24	0x005F24	0x002F24	0x405F24	0x402F24
FICD	0x00AF28	0x005F28	0x005F28	0x002F28	0x405F28	0x402F28
FDMTIVTL	0x00AF2C	0x005F2C	0x005F2C	0x002F2C	0x405F2C	0x402F2C
FDMTIVTH	0x00AF30	0x005F30	0x005F30	0x002F30	0x405F30	0x402F30
FDMTCNTL	0x00AF34	0x005F34	0x005F34	0x002F34	0x405F34	0x402F34
FDMTCNTH	0x00AF38	0x005F38	0x005F38	0x002F38	0x405F38	0x402F38
FDMT	0x00AF3C	0x005F3C	0x005F3C	0x002F3C	0x405F3C	0x402F3C
FDEVOPT1	0x00AF40	0x005F40	0x005F40	0x002F40	0x405F40	0x402F40
FALTREG	0x00AF44	0x005F44	0x005F44	0x002F44	0x405F44	0x402F44
FBTSEQ	0x00AFFC	0x005FFC	0x005FFC	0x002FFC	0x405FFC	0x402FFC
FBOOT(1)	0x801800					

Note 1: FBOOT resides in calibration memory space.

2: Changes to the Inactive Partition Configuration Words affect how the Active Partition accesses the Inactive Partition.

TABLE 30-4: DEVICE IDs FOR THE dsPIC33CK256MP508 FAMILY

Device	DEVID
Device IDs for dsPIC33CK256MP508 Family with CAN FD	
dsPIC33CK256MP508	0x7C74
dsPIC33CK256MP506	0x7C73
dsPIC33CK256MP505	0x7C72
dsPIC33CK256MP503	0x7C71
dsPIC33CK256MP502	0x7C70
dsPIC33CK128MP508	0x7C64
dsPIC33CK128MP506	0x7C63
dsPIC33CK128MP505	0x7C62
dsPIC33CK128MP503	0x7C61
dsPIC33CK128MP502	0x7C60
dsPIC33CK64MP508	0x7C54
dsPIC33CK64MP506	0x7C53
dsPIC33CK64MP505	0x7C52
dsPIC33CK64MP503	0x7C51
dsPIC33CK64MP502	0x7C50
dsPIC33CK32MP506	0x7C43
dsPIC33CK32MP505	0x7C42
dsPIC33CK32MP503	0x7C41
dsPIC33CK32MP502	0x7C40
Device IDs for dsPIC33CK256MP508 Family without CAN FD	
dsPIC33CK256MP208	0x7C34
dsPIC33CK256MP206	0x7C33
dsPIC33CK256MP205	0x7C32
dsPIC33CK256MP203	0x7C31
dsPIC33CK256MP202	0x7C30
dsPIC33CK128MP208	0x7C24
dsPIC33CK128MP206	0x7C23
dsPIC33CK128MP205	0x7C22
dsPIC33CK128MP203	0x7C21
dsPIC33CK128MP202	0x7C20
dsPIC33CK64MP208	0x7C14
dsPIC33CK64MP206	0x7C13
dsPIC33CK64MP205	0x7C12
dsPIC33CK64MP203	0x7C11
dsPIC33CK64MP202	0x7C10
dsPIC33CK32MP206	0x7C03
dsPIC33CK32MP205	0x7C02
dsPIC33CK32MP203	0x7C01
dsPIC33CK32MP202	0x7C00