



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4/M4F
Core Size	32-Bit Dual-Core
Speed	120MHz
Connectivity	EBI/EMI, I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	106
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	304K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4c32ea-au

4.2 144-lead LQFP Package and Pinout

4.2.1 144-lead LQFP Package Outline

The 144-lead LQFP package has a 0.5 mm ball pitch and respects Green Standards.

Figure 4-2 shows the orientation of the 144-lead LQFP package. Refer to Figure 47-2 “144-lead LQFP Package Mechanical Drawing”.

Figure 4-2. Orientation of the 144-lead LQFP Package

144

1

12.6.11.1 VABS

Floating-point Absolute.

Syntax

`VABS{cond}.F32 Sd, Sm`

where:

cond is an optional condition code, see “Conditional Execution”.

Sd, Sm are the destination floating-point value and the operand floating-point value.

Operation

This instruction:

1. Takes the absolute value of the operand floating-point register.
2. Places the results in the destination floating-point register.

Restrictions

There are no restrictions.

Condition Flags

The floating-point instruction clears the sign bit.

Examples

`VABS.F32 S4, S6`

12.6.11.26 VSQRT

Floating-point Square Root.

Syntax

`VSQRT{cond}.F32 Sd, Sm`

where:

cond is an optional condition code, see “Conditional Execution”.

Sd is the destination floating-point value.

Sm is the operand floating-point value.

Operation

This instruction:

- Calculates the square root of the value in a floating-point register.
- Writes the result to another floating-point register.

Restrictions

There are no restrictions.

Condition Flags

These instructions do not change the flags.

- **SIZE: Size of the MPU Protection Region**

The minimum permitted value is 3 (b00010).

The SIZE field defines the size of the MPU memory region specified by the MPU_RNR. as follows:

$$(\text{Region size in bytes}) = 2^{(\text{SIZE}+1)}$$

The smallest permitted region size is 32B, corresponding to a SIZE value of 4. The table below gives an example of SIZE values, with the corresponding region size and value of N in the MPU_RBAR.

SIZE Value	Region Size	Value of N ⁽¹⁾	Note
b00100 (4)	32 B	5	Minimum permitted size
b01001 (9)	1 KB	10	–
b10011 (19)	1 MB	20	–
b11101 (29)	1 GB	30	–
b11111 (31)	4 GB	b01100	Maximum possible size

Note: 1. In the MPU_RBAR; see “MPU Region Base Address Register”

- **ENABLE: Region Enable**

Note: For information about access permission, see “MPU Access Permission Attributes”.

15.5.3 Reset Controller Mode Register

Name: RSTC_MR

Address: 0x400E1408

Access: Read/Write

31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	ERSTL			
7	6	5	4	3	2	1	0
–	–	–	URSTIEN	–	–	–	URSTEN

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_WPMR).

- **URSTEN: User Reset Enable**

0: The detection of a low level on the NRST pin does not generate a user reset.

1: The detection of a low level on the NRST pin triggers a user reset.

- **URSTIEN: User Reset Interrupt Enable**

0: USRTS bit in RSTC_SR at 1 has no effect on rstc_irq.

1: USRTS bit in RSTC_SR at 1 asserts rstc_irq if URSTEN = 0.

- **ERSTL: External Reset Length**

This field defines the external reset length. The external reset is asserted during a time of $2^{(ERSTL+1)}$ slow clock cycles. This allows assertion duration to be programmed between 60 μ s and 2 seconds. Note that synchronization cycles must also be considered when calculating the actual reset length as previously described.

- **KEY: Write Access Password**

Value	Name	Description
0xA5	PASSWD	Writing any other value in this field aborts the write operation. Always reads as 0.

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
CPKEY				–	–	CPBMCK	CPCK
15	14	13	12	11	10	9	8
–	–	–	–	–	PCK2	PCK1	PCK0
7	6	5	4	3	2	1	0
UHDP	–	–	–	–	–	–	–

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

- **UHDP: USB Host/Device Port Clock Disable**

0: No effect.

1: Disables the 48 MHz clock (UHDPCK) of the USB Host/Device Port.

- **PCKx: Programmable Clock x Output Disable**

0: No effect.

1: Disables the corresponding Programmable Clock output.

- **CPCK: Coprocessor Clocks Disable**

0: No effect.

1: Enables the corresponding Coprocessor Clocks (CPHCLK, CPFCLK, CPSYSTICK) if CPKEY = 0xA.

- **CPBMCK: Coprocessor Bus Master Clocks Disable**

0: No effect.

1: Disables the corresponding Coprocessor Bus Master Clock (CPBMCK, CPFCLK) if CPKEY = 0xA.

Note: Disabling CPBMCK must not be performed if CPCK is 1 in PMC_SCSR.

- **CPKEY: Coprocessor Clocks Disable Key**

Value	Name	Description
0xA	PASSWD	This field must be written to 0xA in order to validate CPCK field.

33.8.9 SPI Chip Select Register

Name: SPI_CSRx[x=0..3]

Address: 0x40008030 (0), 0x48000030 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
DLYBCT							
23	22	21	20	19	18	17	16
DLYBS							
15	14	13	12	11	10	9	8
SCBR							
7	6	5	4	3	2	1	0
BITS				CSAAT	CSNAAT	NCPHA	CPOL

This register can only be written if the WPEN bit is cleared in the SPI Write Protection Mode Register.

Note: SPI_CSRx registers must be written even if the user wants to use the default reset values. The BITS field is not updated with the translated value unless the register is written.

- **CPOL: Clock Polarity**

0: The inactive state value of SPCK is logic level zero.

1: The inactive state value of SPCK is logic level one.

CPOL is used to determine the inactive state value of the serial clock (SPCK). It is used with NCPHA to produce the required clock/data relationship between master and slave devices.

- **NCPHA: Clock Phase**

0: Data is changed on the leading edge of SPCK and captured on the following edge of SPCK.

1: Data is captured on the leading edge of SPCK and changed on the following edge of SPCK.

NCPHA determines which edge of SPCK causes data to change and which edge causes data to be captured. NCPHA is used with CPOL to produce the required clock/data relationship between master and slave devices.

- **CSNAAT: Chip Select Not Active After Transfer (Ignored if CSAAT = 1)**

0: The Peripheral Chip Select does not rise between two transfers if the SPI_TDR is reloaded before the end of the first transfer and if the two transfers occur on the same Chip Select.

1: The Peripheral Chip Select rises systematically after each transfer performed on the same slave. It remains inactive after the end of transfer for a minimal duration of:

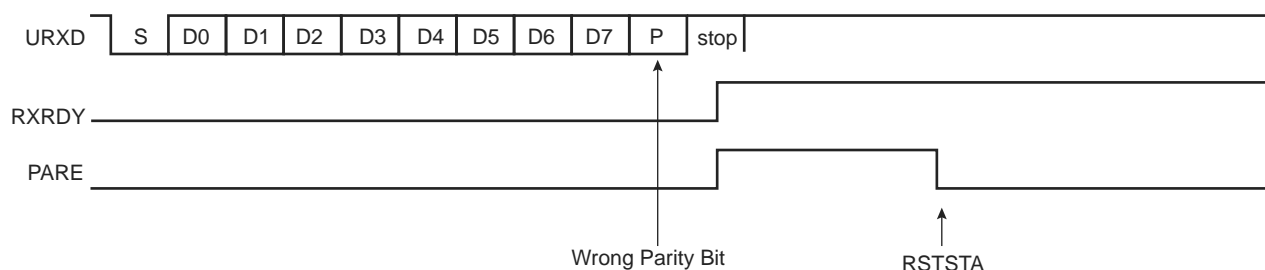
$$\frac{DLYBCS}{f_{\text{peripheral clock}}} \quad (\text{If field DLYBCS is lower than 6, a minimum of six periods is introduced.})$$

- **CSAAT: Chip Select Active After Transfer**

0: The Peripheral Chip Select Line rises as soon as the last transfer is achieved.

1: The Peripheral Chip Select does not rise after the last transfer is achieved. It remains active until a new transfer is requested on a different chip select.

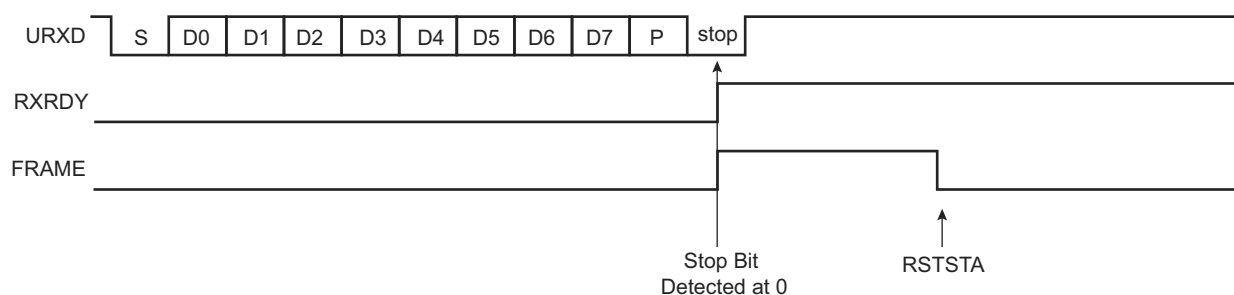
Figure 35-7. Parity Error



35.5.2.6 Receiver Framing Error

When a start bit is detected, it generates a character reception when all the data bits have been sampled. The stop bit is also sampled and when it is detected at 0, the FRAME (Framing Error) bit in UART_SR is set at the same time the RXRDY bit is set. The FRAME bit remains high until the Control Register (UART_CR) is written with the bit RSTSTA at 1.

Figure 35-8. Receiver Framing Error



35.5.2.7 Receiver Digital Filter

The UART embeds a digital filter on the receive line. It is disabled by default and can be enabled by writing a logical 1 in the FILTER bit of UART_MR. When enabled, the receive line is sampled using the 16x bit clock and a three-sample filter (majority 2 over 3) determines the value of the line.

35.5.3 Transmitter

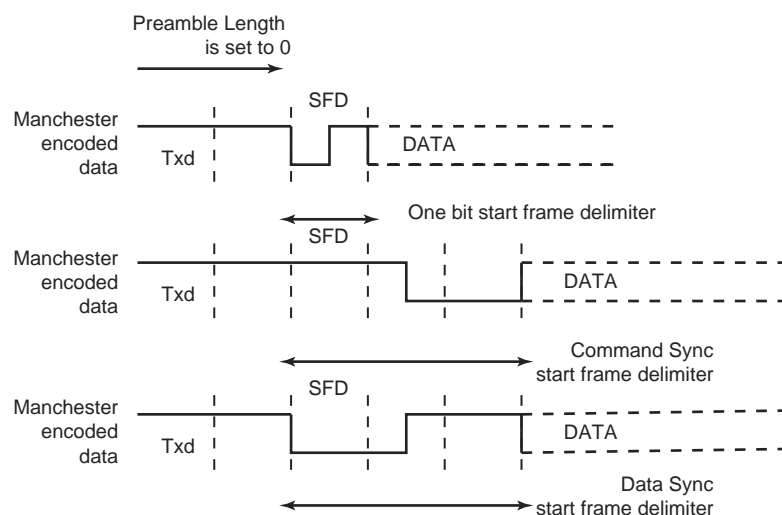
35.5.3.1 Transmitter Reset, Enable and Disable

After device reset, the UART transmitter is disabled and must be enabled before being used. The transmitter is enabled by writing UART_CR with the bit TXEN at 1. From this command, the transmitter waits for a character to be written in the Transmit Holding Register (UART_THR) before actually starting the transmission.

The programmer can disable the transmitter by writing UART_CR with the bit TXDIS at 1. If the transmitter is not operating, it is immediately stopped. However, if a character is being processed into the internal shift register and/or a character has been written in the UART_THR, the characters are completed before the transmitter is actually stopped.

The programmer can also put the transmitter in its reset state by writing the UART_CR with the bit RSTTX at 1. This immediately stops the transmitter, whether or not it is processing characters.

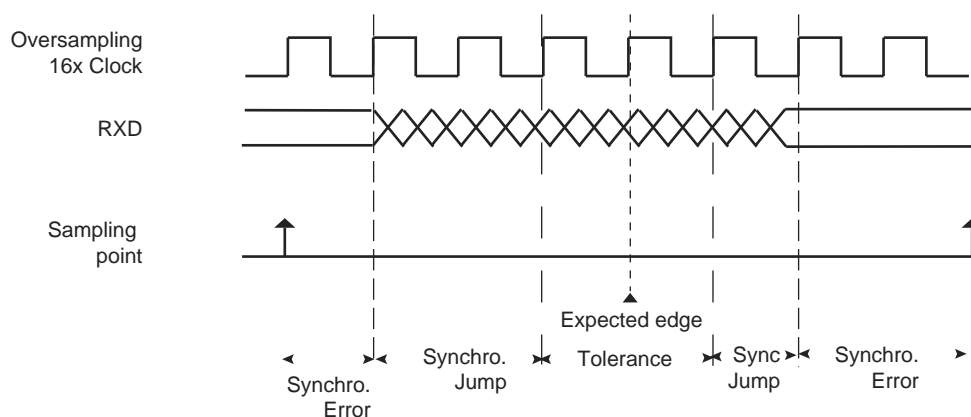
Figure 36-9. Start Frame Delimiter



Drift Compensation

Drift compensation is available only in 16X oversampling mode. An hardware recovery system allows a larger clock drift. To enable the hardware system, the bit in the USART_MAN register must be set. If the RXD edge is one 16X clock cycle from the expected edge, this is considered as normal jitter and no corrective actions is taken. If the RXD event is between 4 and 2 clock cycles before the expected edge, then the current period is shortened by one clock cycle. If the RXD event is between 2 and 3 clock cycles after the expected edge, then the current period is lengthened by one clock cycle. These intervals are considered to be drift and so corrective actions are automatically taken.

Figure 36-10. Bit Resynchronization

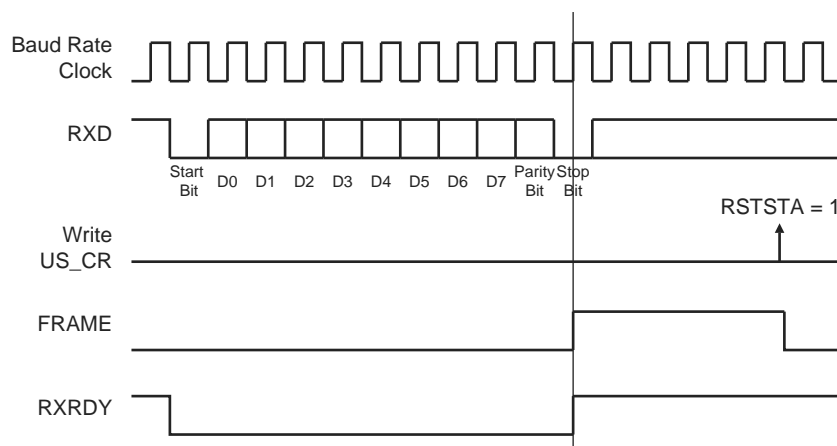


36.6.3.3 Asynchronous Receiver

If the USART is programmed in Asynchronous operating mode (SYNC = 0), the receiver oversamples the RXD input line. The oversampling is either 16 or 8 times the baud rate clock, depending on the OVER bit in the US_MR. The receiver samples the RXD line. If the line is sampled during one half of a bit time to 0, a start bit is detected and data, parity and stop bits are successively sampled on the bit rate clock.

If the oversampling is 16 (OVER = 0), a start is detected at the eighth sample to 0. Data bits, parity bit and stop bit are assumed to have a duration corresponding to 16 oversampling clock cycles. If the oversampling is 8 (OVER = 1), a start bit is detected at the fourth sample to 0. Data bits, parity bit and stop bit are assumed to have a duration corresponding to 8 oversampling clock cycles.

Figure 36-24. Framing Error Status



36.6.3.13 Transmit Break

The user can request the transmitter to generate a break condition on the TXD line. A break condition drives the TXD line low during at least one complete character. It appears the same as a 0x00 character sent with the parity and the stop bits at 0. However, the transmitter holds the TXD line at least during one character until the user requests the break condition to be removed.

A break is transmitted by writing a 1 to the STTBK bit in the US_CR. This can be performed at any time, either while the transmitter is empty (no character in either the Shift register or in US_THR) or when a character is being transmitted. If a break is requested while a character is being shifted out, the character is first completed before the TXD line is held low.

Once STTBK command is requested further STTBK commands are ignored until the end of the break is completed.

The break condition is removed by writing a 1 to the STPBK bit in the US_CR. If the STPBK is requested before the end of the minimum break duration (one character, including start, data, parity and stop bits), the transmitter ensures that the break condition completes.

The transmitter considers the break as though it is a character, i.e., the STTBK and STPBK commands are processed only if the TXRDY bit in US_CSR is to 1 and the start of the break condition clears the TXRDY and TXEMPTY bits as if a character is processed.

Writing US_CR with both STTBK and STPBK bits to 1 can lead to an unpredictable result. All STPBK commands requested without a previous STTBK command are ignored. A byte written into the Transmit Holding register while a break is pending, but not started, is ignored.

After the break condition, the transmitter returns the TXD line to 1 for a minimum of 12 bit times. Thus, the transmitter ensures that the remote receiver detects correctly the end of break and the start of the next character. If the timeguard is programmed with a value higher than 12, the TXD line is held high for the timeguard period.

After holding the TXD line for this period, the transmitter resumes normal operations.

Figure 36-25 illustrates the effect of both the Start Break (STTBK) and Stop Break (STPBK) commands on the TXD line.

The following triggers are common to both modes:

- Software Trigger: Each channel has a software trigger, available by setting SWTRG in TC_CCR.
- SYNC: Each channel has a synchronization signal SYNC. When asserted, this signal has the same effect as a software trigger. The SYNC signals of all channels are asserted simultaneously by writing TC_BCR (Block Control) with SYNC set.
- Compare RC Trigger: RC is implemented in each channel and can provide a trigger when the counter value matches the RC value if CPCTRG is set in the TC_CMR.

The channel can also be configured to have an external trigger. In Capture mode, the external trigger signal can be selected between TIOA and TIOB. In Waveform mode, an external event can be programmed on one of the following signals: TIOB, XC0, XC1 or XC2. This external event can then be programmed to perform a trigger by setting bit ENETRIG in the TC_CMR.

If an external trigger is used, the duration of the pulses must be longer than the peripheral clock period in order to be detected.

37.6.7 Capture Mode

Capture mode is entered by clearing the WAVE bit in the TC_CMR.

Capture mode allows the TC channel to perform measurements such as pulse timing, frequency, period, duty cycle and phase on TIOA and TIOB signals which are considered as inputs.

Figure 37-5 shows the configuration of the TC channel when programmed in Capture mode.

37.6.8 Capture Registers A and B

Registers A and B (RA and RB) are used as capture registers. They can be loaded with the counter value when a programmable event occurs on the signal TIOA.

The LDRA field in the TC_CMR defines the TIOA selected edge for the loading of register A, and the LDRB field defines the TIOA selected edge for the loading of Register B.

RA is loaded only if it has not been loaded since the last trigger or if RB has been loaded since the last loading of RA.

RB is loaded only if RA has been loaded since the last trigger or the last loading of RB.

Loading RA or RB before the read of the last value loaded sets the Overrun Error Flag (LOVRS bit) in the TC_SR. In this case, the old value is overwritten.

37.6.9 Trigger Conditions

In addition to the SYNC signal, the software trigger and the RC compare trigger, an external trigger can be defined.

The ABETRIG bit in the TC_CMR selects TIOA or TIOB input signal as an external trigger. The External Trigger Edge Selection parameter (ETRGEDG field in TC_CMR) defines the edge (rising, falling, or both) detected to generate an external trigger. If ETRGEDG = 0 (none), the external trigger is disabled.

39. Segment Liquid Crystal Display Controller (SLCDC)

39.1 Description

The Segment Liquid Crystal Display Controller (SLCDC) can drive a monochrome passive liquid crystal display (LCD) with up to 6 common terminals and up to 50 segment terminals.

An LCD consists of several segments (pixels or complete symbols) which can be visible or invisible. A segment has two electrodes with liquid crystal between them. When a voltage above a threshold voltage is applied across the liquid crystal, the segment becomes visible.

The voltage must alternate to avoid an electrophoresis effect in the liquid crystal, which degrades the display. Hence the waveform across a segment must not have a DC component.

The SLCDC is programmable to support many different requirements such as:

- Adjusting the driving time of the LCD pads in order to save power and increase the controllability of the DC offset
- Driving smaller LCD (down to 1 common by 1 segment)
- Adjusting the SLCDC frequency in order to obtain the best compromise between frequency and consumption and adapt it to the LCD driver
- Assigning the segments in a user defined pattern to simplify the use of the digital functions multiplexed on these pins

Table 39-1. List of Terms

Term	Description
LCD	A passive display panel with terminals leading directly to a segment
Segment	The least viewing element (pixel) which can be on or off
Common(s)	Denotes how many segments are connected to a segment terminal
Duty	$1/(\text{Number of common terminals on a current LCD display})$
Bias	$1/(\text{Number of voltage levels used driving an LCD display} - 1)$
Frame Rate	Number of times the LCD segments are energized per second

39.2 Embedded Characteristics

The SLCDC provides the following capabilities:

- Display Capacity: Up to 50 Segments and 6 Common Terminals
- Support from Static to 1/6 Duty
- Supports: Static and 1/2 and 1/3 Bias
- Two LCD Supply Sources:
 - Internal (On-chip LCD Power Supply)
 - External
- LCD Output Voltage Software Selectable from 2.4V to VDDIN in 16 Steps (Control Embedded in the Supply Controller)
- Flexible Selection of Frame Frequency
- Two Interrupt Sources: End Of Frame and Disable
- Versatile Display Modes
- Equal Source and Sink Capability to Maximize LCD Life Time
- Segment and Common Pins not Needed for Driving the Display Can be Used as Ordinary I/O Pins

39.8.7 SLCDC Interrupt Disable Register

Name: SLCDC_IDR

Address: 0x4003C024

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	DIS	–	ENDFRAME

- **ENDFRAME: End of Frame Interrupt Disable**

0: No effect.

1: Disables the corresponding interrupt.

- **DIS: SLCDC Disable Completion Interrupt Disable**

0: No effect.

1: Disables the corresponding interrupt.

40.5 Product Dependencies

40.5.1 Power Management

The ADC Controller is not continuously clocked. The programmer must first enable the ADC Controller peripheral clock in the Power Management Controller (PMC) before using the ADC Controller. However, if the application does not require ADC operations, the ADC Controller clock can be stopped when not needed and restarted when necessary. Configuring the ADC Controller does not require the ADC Controller clock to be enabled.

40.5.2 Interrupt Sources

The ADC interrupt line is connected on one of the internal sources of the Interrupt Controller. Using the ADC interrupt requires the interrupt controller to be programmed first.

Table 40-2. Peripheral IDs

Instance	ID
ADC	29

40.5.3 Analog Inputs

The analog input pins can be multiplexed with PIO lines. In this case, the assignment of the ADC input is automatically done as soon as the corresponding channel is enabled by writing the Channel Enable register (ADC_CHER). By default, after reset, the PIO line is configured as a digital input with its pull-up enabled, and the ADC input is connected to the GND.

40.5.4 Temperature Sensor

The temperature sensor is internally connected to channel index 7 of the ADC.

The temperature sensor provides an output voltage V_T that is proportional to the absolute temperature (PTAT). To activate the temperature sensor, the TEMPON bit in the Temperature Sensor Mode register (ADC_TEMPMR) must be set. After setting the bit, the startup time of the temperature sensor must be achieved prior to initiating any measurement.

40.5.5 I/O Lines

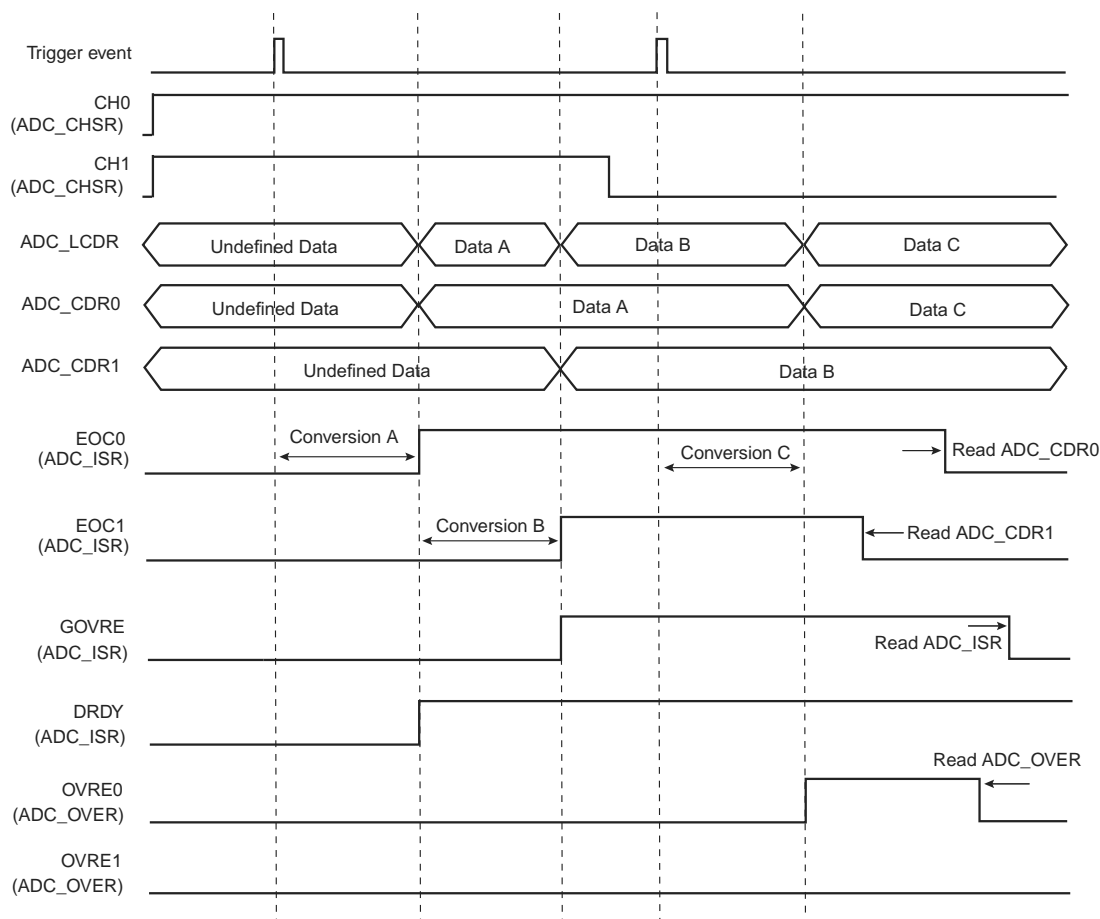
The digital input ADTRG is multiplexed with digital functions on the I/O line and the selection of ADTRG is made using the PIO controller by configuring the I/O Input mode.

The analog inputs ADx are multiplexed with digital functions on the I/O lines. ADx inputs are selected as inputs of the ADCC when writing a one in the corresponding CHx bit of ADC_CHER and the digital functions are not selected.

Table 40-3. I/O Lines

Instance	Signal	I/O Line	Peripheral
ADC	ADTRG	PB23	A
ADC	COM4/AD1	PA4	X1
ADC	COM5/AD2	PA5	X1
ADC	SEG6/AD0	PA12	X1
ADC	SEG31/AD3	PB13	X1
ADC	SEG41/AD4	PB23	X1
ADC	SEG49/AD5	PB31	X1

Figure 40-4. EOCx, GOVRE and OVREx Flag Behavior



Warning: If the corresponding channel is disabled during a conversion or if it is disabled and then reenabled during a conversion, the associated data and the corresponding EOCx and GOVRE flags in ADC_ISR and OVREx flags in ADC_OVER are unpredictable.

40.6.5 Conversion Triggers

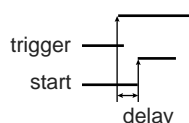
Conversions of the active analog channels are started with a software or hardware trigger. The software trigger is provided by writing the Control register (ADC_CR) with the START bit at 1.

The hardware trigger can be one of the TIOA outputs of the Timer Counter channels or the external trigger input of the ADC (ADTRG). The hardware trigger is selected with the TRGSEL field in ADC_MR. The selected hardware trigger is enabled with the TRGEN bit in ADC_MR.

The minimum time between two consecutive trigger events must be strictly greater than the duration time of the longest conversion sequence as configured in ADC_MR, ADC_CHSR and ADC_SEQR1.

If a hardware trigger is selected, the start of a conversion is triggered after a delay which starts at each rising edge of the selected signal. Due to asynchronous handling, the delay may vary in a range of two peripheral clock periods to one ADC clock period.

Figure 40-5. Hardware Trigger Delay



40.7.3 ADC Channel Sequence 1 Register

Name: ADC_SEQR1

Address: 0x40038008

Access: Read/Write

31	30	29	28	27	26	25	24
USCH8				USCH7			
23	22	21	20	19	18	17	16
USCH6				USCH5			
15	14	13	12	11	10	9	8
USCH4				USCH3			
7	6	5	4	3	2	1	0
USCH2				USCH1			

This register can only be written if the WPEN bit is cleared in “ADC Write Protection Mode Register” .

- **USCHx: User Sequence Number x**

The sequence number x (USCHx) can be programmed by the channel number CHy where y is the value written in this field. The allowed range is 0 up to 7. So it is only possible to use the sequencer from CH0 to CH7.

This register activates only if ADC_MR(USEQ) field is set to 1.

Any USCHx field is taken into account only if ADC_CHSR(CHx) register field reads logical 1; else any value written in USCHx does not add the corresponding channel in the conversion sequence.

Configuring the same value in different fields leads to multiple samples of the same channel during the conversion sequence. This can be done consecutively, or not, depending on user needs.

43. Classical Public Key Cryptography Controller (CPKCC)

43.1 Description

The Classical Public Key Cryptography Controller (CPKCC) is an Atmel macrocell that processes public key cryptography algorithm calculus in both $GF(p)$ and $GF(2^n)$ fields. The ROMed CPKCL, the Classical Public Key Cryptography Library, is the library built on the top of the CPKCC.

The Classical Public Key Cryptography Library includes complete implementation of the following public key cryptography algorithms:

- RSA, DSA:
 - Modular Exponentiation with CRT up to 6144 bits
 - Modular Exponentiation without CRT up to 5408 bits
 - Prime generation
 - Utilities: GCD/modular Inverse, Divide, Modular reduction, Multiply, ...
- Elliptic Curves:
 - ECDSA up to 1504 bits
 - Point Multiply,
 - Point Add/Doubling
 - Elliptic Curves in $GF(p)$ or $GF(2^n)$
 - Choice of the curves parameters so compatibility with NIST Curves or others.
- Deterministic Random Number Generation (DRNG ANSI X9.31) for DSA

- **UPRSM: Upstream Resume Interrupt**

0: Cleared when the USBFS_DEVICR.UPRSMC bit is written to one to acknowledge the interrupt (USBFS clock inputs must be enabled before).

1: Set when the USBFS sends a resume signal called “Upstream Resume”. This triggers a USB interrupt if USBFS_DEVIMR.UPRSME = 1.

- **PEP_x: Endpoint x Interrupt**

0: Cleared when the interrupt source is serviced.

1: Set when an interrupt is triggered by the endpoint x (USBFS_DEVEPTISR_x, USBFS_DEVEPTIMR_x). This triggers a USB interrupt if USBFS_DEVIMR.PEP_x = 1.

- **DMA_x: DMA Channel x Interrupt**

0: Cleared when the USBFS_DEVDMASTATUS_x interrupt source is cleared.

1: Set when an interrupt is triggered by the DMA channel x. This triggers a USB interrupt if DMA_x = 1.

45.6.10 Device Global Interrupt Disable Register

Name: USBFS_DEVIDR

Address: 0x40020014

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	DMA_4	DMA_3	DMA_2	DMA_1	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	PEP_4
15	14	13	12	11	10	9	8
PEP_3	PEP_2	PEP_1	PEP_0	–	–	–	–
7	6	5	4	3	2	1	0
–	UPRSMEC	EORSMEC	WAKEUPEC	EORSTEC	SOFEC	–	SUSPEC

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Clears the corresponding bit in USBFS_DEVIMR

- **SUSPEC: Suspend Interrupt Disable**
- **SOFEC: Start of Frame Interrupt Disable**
- **EORSTEC: End of Reset Interrupt Disable**
- **WAKEUPEC: Wake-Up Interrupt Disable**
- **EORSMEC: End of Resume Interrupt Disable**
- **UPRSMEC: Upstream Resume Interrupt Disable**
- **PEP_x: Endpoint x Interrupt Disable**
- **DMA_x: DMA Channel x Interrupt Disable**

Table 53-3. SAM4C Datasheet Rev. 11102E Revision History (Continued)

Doc. Rev. 11102E	Changes
06-Oct-14	Section 49. "Ordering Information" Updated Table 49-1 "Ordering Codes for SAM4C Devices".
	Section 50. "SAM4C16/8 Errata Revision A (MRL A) Parts" Removed erratum on SUPC: LCD End of Frame Disable Does Not Work.
	Added Section 50.5.2 "RSWDT Windowing Mode", Section 50.7.1 "Unpredictable Software Behavior When Entering Sleep Mode", Section 50.8.1 "CORE 1 SysTick Counter Erratic Behavior" and Section 50.9.1 "SRCB Bit in CKGR_PLLB Register".
	Added Section 51. "SAM4C16/8 Errata Revision B (MRL B) Parts".
	Added Section 52. "SAM4C32 Errata Revision A (MRL A) Parts".

Table 53-4. SAM4C Datasheet Rev. 11102D Revision History

Doc. Rev. 11102D	Changes
14-Apr-14	Section 46. "Electrical Characteristics" Table 46-1 "Absolute Maximum Ratings*": removed junction temperature. Table 46-21 "VDDIO Supply Monitor": modified min and max values for parameter ACC. Table 46-26 "4/8/12 MHz RC Oscillators Characteristics": modified conditions for ACC4, ACC8 and ACC12. Modified max values for ACC8 and ACC12. Figure 45-18 "Measurement Setup for Configuration C and D": added note below figure.
	Table 46-49 "SAM4C16/8 Typical Current Consumption Values for Backup Mode Configurations C and D": modified 'Conditions' column to VDDIO.
	Table 46-59 "SAM4C8/16 Test Setup 3 Current Consumption": modified values for 128-bit Flash Access, Cache Enabled columns.
	Section 50. "SAM4C16/8 Errata Revision A (MRL A) Parts" Added erratum on Flash Memory: "Flash: Incorrect Flash Read May Occur Depending on VDDIO Voltage and Flash Wait State"

Table 53-5. SAM4C Datasheet Rev. 11102C Revision History

Doc. Rev. 11102C	Changes
16-Jan-14	Table 5-2 "Low-power Mode Configuration Summary": modified notes ⁽⁴⁾ and ⁽⁵⁾ .
	Section 46. "Electrical Characteristics" Removed section 45.5.17.2 '10-bit ADC with Averager'.
	Table 46-65 "Power Consumption on VDDCORE(1)": all consumption values modified except AES.
	Removed section 45.7.6 'Low-power Mode Wake-up Time'.