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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, Serial Port
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e532a40dl

Timers

The W79E(L)532 has three 16-bit timers that are functionally similar to the timers of the 8052 family. When used as timers, they can be set to run at either 4 clocks or 12 clocks per count, thus providing the user with the option of operating in a mode that emulates the timing of the original 8052. The W79E(L)532 has an additional feature, the watchdog timer. This timer is used as a System Monitor or as a very long time period timer.

Interrupts

The Interrupt structure in the W79E(L)532 is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W79E(L)532 provides 7 interrupt resources with two priority level, including 2 external interrupt sources, timer interrupts, serial I/O interrupts.

Power Management

Like the standard 80C52, the W79E(L)532 also has IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU core is stopped while the timers, serial port and interrupts clock continue to operate. In the POWER DOWN mode, all the clock are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

On-chip Data SRAM

The W79E(L)532 has 1K Bytes of data space SRAM which is read/write accessible and is memory mapped. This on-chip MOVX SRAM is reached by the MOVX instruction. It is not used for executable program memory. There is no conflict or overlap among the 256 bytes Scratchpad RAM and the 1K Bytes MOVX SRAM as they use different addressing modes and separate instructions. The on-chip MOVX SRAM is enabled by setting the DME0 bit in the PMR register. After a reset, the DME0 bit is cleared such that the on-chip MOVX SRAM is disabled, and all data memory spaces 0000H – FFFFH access to the external memory.

PD: Setting this bit causes the W79E(L)532 to go into the POWER DOWN mode. In this mode all the
clocks are stopped and program execution is frozen.

IDL: Setting this bit causes the W79E(L)532 to go into the IDLE mode. In this mode the clocks to the
CPU are stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

TF1: Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.

TR1: Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.

TF0: Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.

TR0: Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.

IE1: Interrupt 1 edge detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.

IT1: Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

IE0: Interrupt 0 edge detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.

IT0: Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C / $\overline{T}$	M1	M0	GATE	C / $\overline{T}$	M1	M0
			TIMER1				TIMER0	

Mnemonic: TMOD Address: 89h

GATE: Gating control: When this bit is set, Timer/counter x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.

REN: Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.

TB8: This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.

RB8: In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.

TI: Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

RI: Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

SBUF.7-0: Serial data on the serial port 0 is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

P4.2 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P42AL Address: 9Ah

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P42AH Address: 9Bh

P4.3 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P43AL Address: 9Ch

P4.3 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P43AH Address: 9Dh

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST/HWB	-	LDAP	-	-	-	LDSEL	ENP

Mnemonic: CHPCON Address: 9Fh

SWRST/HWB: Set this bit to launch a whole device reset that is same as asserting high to RST pin, micro controller will be back to initial state and clear this bit automatically. To read this bit, its alternate function to indicate the ISP hardware reboot mode is invoking when read it in high.

LDAP: This bit is Read Only. High: device is executing the program in LDFlash. Low: device is executing the program in APFlashs.

LDSEL: Loader program residence selection. Set to high to route the device fetching code from LDFlash.

ENP: In System Programming Mode Enable. Set this be to launch the ISP mode. Device will operate ISP procedures, such as Erase, Program and Read operations, according to correlative SFRs settings. During ISP mode, device achieves ISP operations by the way of IDLE state. In the other words, device is not indeed in IDLE mode is set bit PCON.1 while ISP is enabled. Clear this bit to disable ISP mode, device get back to normal operation including IDLE state.

Software Reset

Set CHPCON = 0X83, timer and enter IDLE mode. CPU will reset and restart from APFlash after time out.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

Port 4 Chip-select Polarity

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P42INV	P40INV	-	-	-	P0UP

Mnemonic: P4CSIN Address: A2h

P4xINV: The active polarity of P4.x when set it as chip-select signal. High = Active High. Low = Active Low.

P0UP: Enable Port 0 weak pull up.

Timer 2 Capture LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L: This register is used to capture the TL2 value when a timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 Capture MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H: This register is used to capture the TH2 value when a timer 2 is configured in capture mode.
RCAP2H is also used as the MSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2: Timer 2 LSB

Timer 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TH2: Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

CY: Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.

AC: Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.

F0: User flag 0: General purpose flag that can be set or cleared by the user.

7. INSTRUCTION

The W79E(L)532 executes all the instructions of the standard 8032 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W79E(L)532, each machine cycle consists of 4 clock periods, while in the standard 8032 it consists of 12 clock periods. Also, in the W79E(L)532 there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8032 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the W79E(L)532 has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W79E(L)532 reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8032.

7.1 Instruction Timing

The instruction timing for the W79E(L)532 is an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the W79E(L)532 and the standard 8032. In the W79E(L)532 each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2 C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the W79E(L)532 does one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the W79E(L)532 are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8032, the MOVX instruction is always two machine cycles long. However in the W79E(L)532, the user has a facility to stretch the duration of this instruction from 2 machine cycles to 9 machine cycles. The $\overline{RD}$ and $\overline{WR}$ strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. The rest of the instructions are either three, four or five machine cycle instructions. Note that in the W79E(L)532, based on the number of machine cycles, there are five different types, while in the standard 8032 there are only three. However, in the W79E(L)532 each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8032. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8032 in terms of clock periods.

Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have FFh written into them which puts the port pins in a high state. Port 0 floats as it does not have on-chip pull-ups.

Table 6. SFR Reset Value

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111b	IE	00000000b
SP	00000111b	SADDR	00000000b
DPL	00000000b	P3	11111111b
DPH	00000000b	IP	x0000000b
PMR	010xx0x0b	SADEN	00000000b
STATUS	000x0000b	T2CON	00000000b
PC	00000000b	T2MOD	00000x00b
PCON	00xx0000b	RCAP2L	00000000b
TCON	00000000b	RCAP2H	00000000b
TMOD	00000000b	TL2	00000000b
TL0	00000000b	TH2	00000000b
TL1	00000000b	TA	11111111b
TH0	00000000b	PSW	00000000b
TH1	00000000b	WDCON	0x0x0xx0b
CKCON	00000001b	ACC	00000000b
P1	11111111b	EIE	xxx00000b
P4CONA	00000000b	P4CONB	00000000b
P40AL	00000000b	P40AH	00000000b
P41AL	00000000b	P41AH	00000000b
P42AL	00000000b	P42AH	00000000b
P43Al	00000000b	P43AH	00000000b
CHPCON	00000000b	P4CSIN	00000000b
ROMCON	00000111b	SFRAL	00000000b
SFRAH	00000000b	SFRFD	00000000b

10. PROGRAMMABLE TIMERS/COUNTERS

The W79E(L)532 has three 16-bit programmable timer/counters and one programmable Watchdog timer. The Watchdog timer is operationally quite different from the other two timers.

10.1 Timer/Counters 0 & 1

The W79E(L)532 has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

Time-Base Selection

The W79E(L)532 gives the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the W79E(L)532 and the standard 8051 can be matched. This is the default mode of operation of the W79E(L)532 timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bits in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

Mode 0

In Mode 0, the timer/counters act as a 8 bit counter with a 5 bit, divide by 32 pre-scale. In this mode we have a 13 bit timer/counter. The 13 bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock increments the count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When the count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. When $C/\overline{T}$ is set to 0, then it will count clock cycles,

and if C / $\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P3.4) for timer 0 and T1 (P3.5) for timer 1. When the 13 bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur. Note that when used as a timer, the time-base may be either clock cycles/12 or clock cycles/4 as selected by the bits TxM of the CKCON SFR.

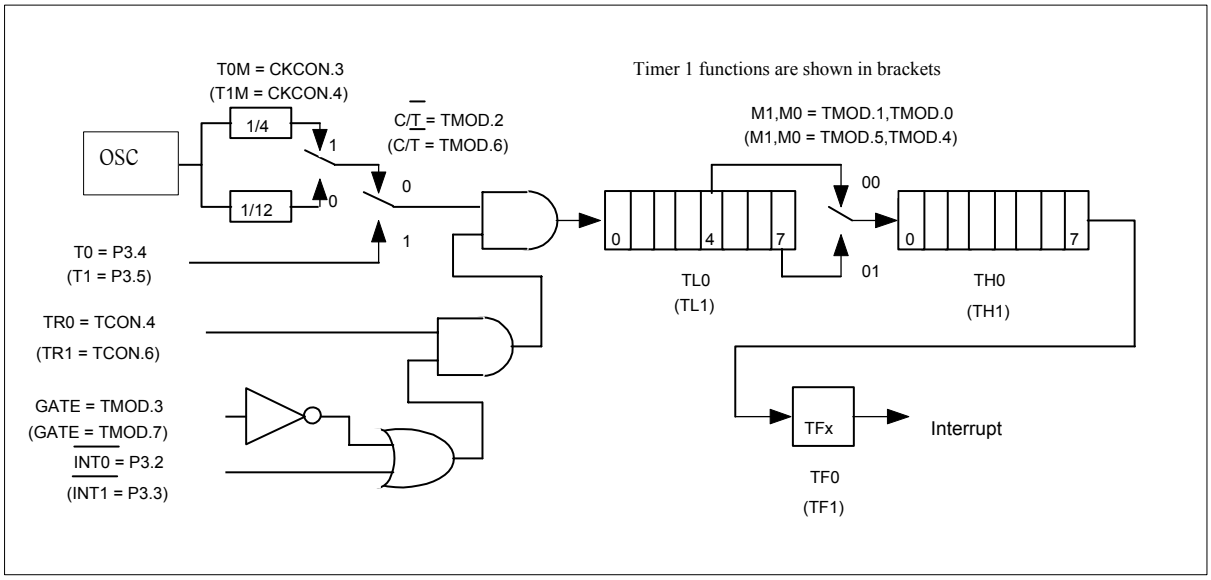


Figure 11. Timer/Counter Mode 0 & Mode 1

Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16 bit counter, rather than a 13 bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

Auto-reload Mode, Counting Up/Down

Timer/Counter 2 will be in auto-reload mode as an up/down counter if CP / $\overline{RL2}$ bit in T2CON is cleared and the DCEN bit in T2MOD is set. In this mode, Timer/Counter 2 is an up/down counter whose direction is controlled by the T2EX pin. A 1 on this pin cause the counter to count up. An overflow while counting up will cause the counter to be reloaded with the contents of the capture registers. The next down count following the case where the contents of Timer/Counter equal the capture registers will load an FFFFh into Timer/Counter 2. In either event a reload will set the TF2 bit. A reload will also toggle the EXF2 bit. However, the EXF2 bit can not generate an interrupt while in this mode.

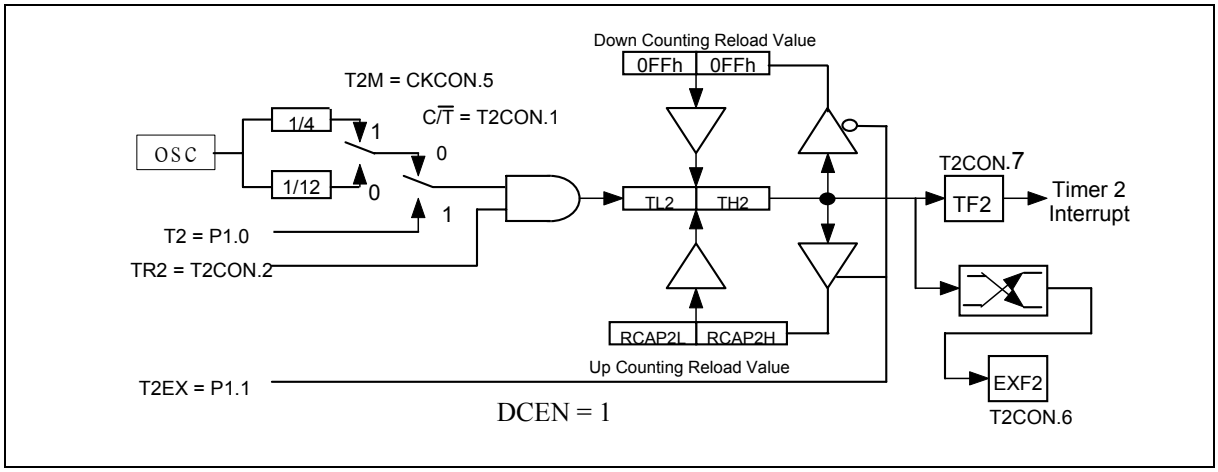


Figure 16. 16-Bit Auto-reload Up/Down Counter

Baud Rate Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.

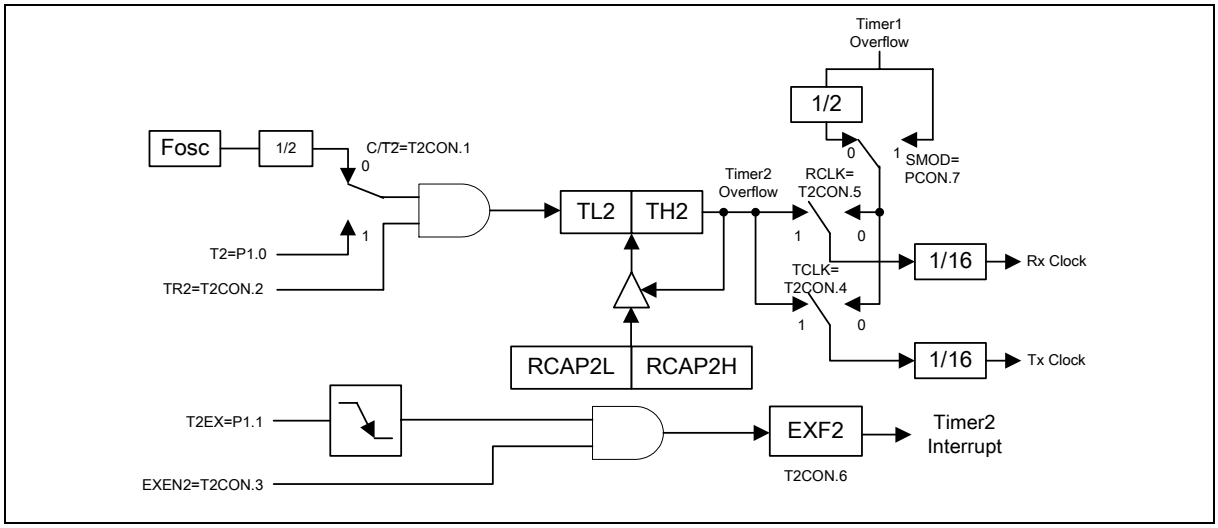


Figure 17. Baud Rate Generator Mode

PWM2 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM2 Address: DDH

PWM Control 1 Register

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENWPM0

Mnemonic: PWMCON1 Address: DCH

PWM3OE: Output enable for PWM3
PWM2OE: Output enable for PWM2
ENPWM3: Enable PWM3
ENPWM2: Enable PWM2
PWM1OE: Output enable for PWM1
PWM0OE: Output enable for PWM0
ENPWM1: Enable PWM1
ENPWM0: Enable PWM0

PWM1 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM1 Address: DBH

PWM0 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM0 Address: DAH

PWMP Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWMP Address: D9H

PWM4 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM4 Address: CFH

PWM Control 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM5OE-	PWM4OE	ENWPM5	ENWPM4

Mnemonic: PWMCON2 Address: CEH

PWM5OE: Output enable for PWM5

PWM4OE: Output enable for PWM4

ENPWM5: Enable for PWM5

ENPWM4: Enable for PWM4

PWM5 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM5 Address: C3H

10.4 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the users software.

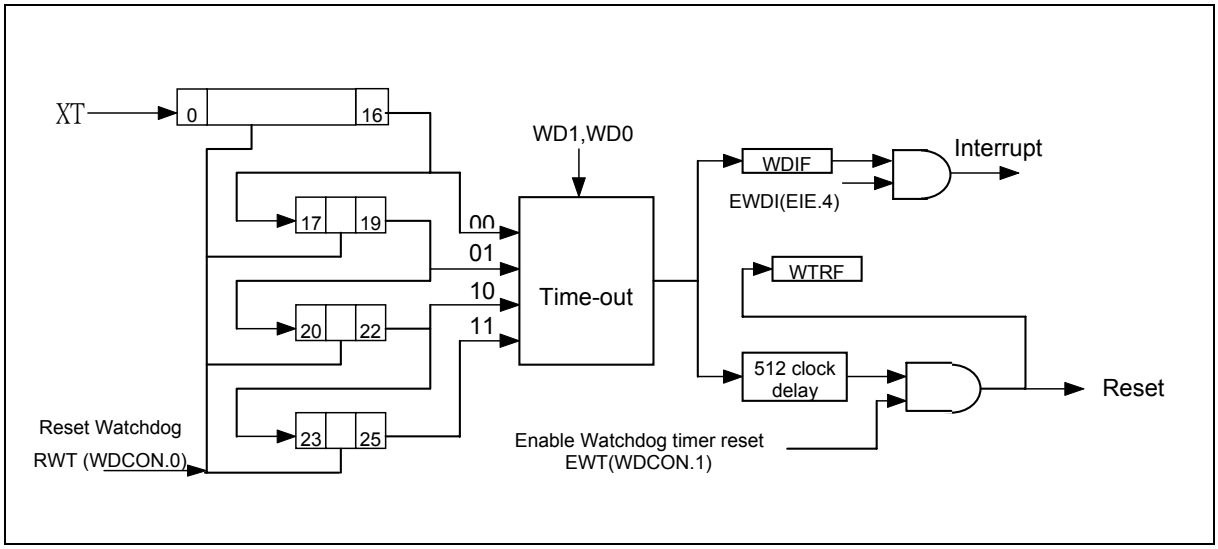


Figure 19. Watchdog Timer

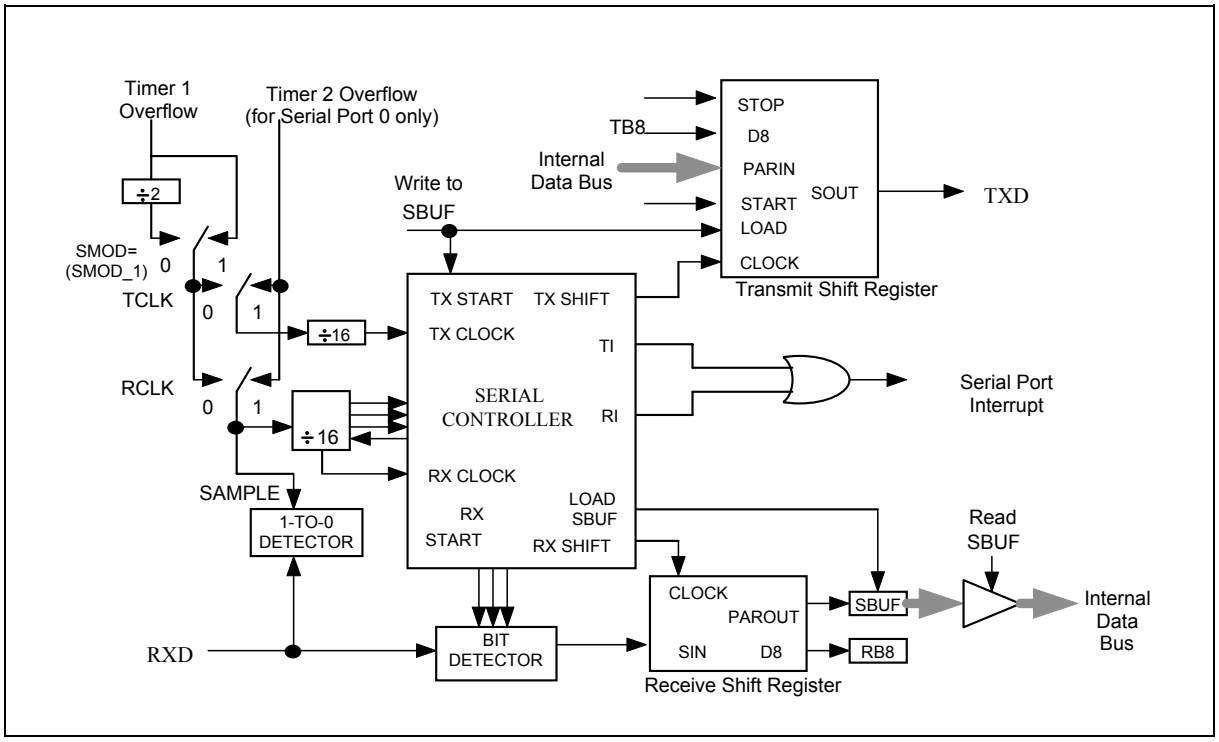


Figure 23. Serial Port Mode 3

Table 10. Serial Ports Modes

SM1	SM0	MODE	TYPE	BAUD CLOCK	FRAME SIZE	STAR T BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

11.1 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W79E(L)532 has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE(FE_1) bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W79E(L)532 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

11.2 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the W79E(L)532, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

12. TIMED ACCESS PROTECTION

The W79E(L)532 has several new features, like the Watchdog timer, on-chip ROM size adjustment, wait state control signal and Power on/fail reset flag, which are crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E(L)532 has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access(TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG    0C7h          ;define new register TA, located at 0C7h
MOV     TA, #0AAh
MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
MOV     TA, #0AAh       3 M/C          Note: M/C = Machine Cycles
MOV     TA, #055h       3 M/C
MOV     WDCON, #00h     3 M/C
```

Example 2: Valid access

```
MOV     TA, #0AAh       3 M/C
MOV     TA, #055h       3 M/C
NOP                     1 M/C
SETB    EWT             2 M/C
```

Example 3: Valid access

```
MOV     TA, #0Aah       3 M/C
MOV     TA, #055h       3 M/C
ORL     WDCON, #00000010B  3M/C
```

Example 4: Invalid access

```
MOV   TA, #0AAh    3 M/C
MOV   TA, #055h    3 M/C
NOP                1 M/C
NOP                1 M/C
CLR   POR          2 M/C
```

Example 5: Invalid Access

```
MOV   TA, #0AAh    3 M/C
NOP                1 M/C
MOV   TA, #055h    3 M/C
SETB  EWT          2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycle window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window in not opened at all, and the write to the protected bit fails.

14. IN-SYSTEM PROGRAMMING

14.1 The Loader Program Locates at LDFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #03H value before CPU has entered idle state. CPU will switch to LDFlash memory and execute a reset action. H/W reboot mode will switch to LDFlash memory, too. Set SFRCN register where it locates at user's loader program to update APFlash bank 0 or bank 1 memory. Set a SWRESET (CHPCON.7) to switch back APFlash after CPU has updated APFlash program. CPU will restart to run program from reset state.

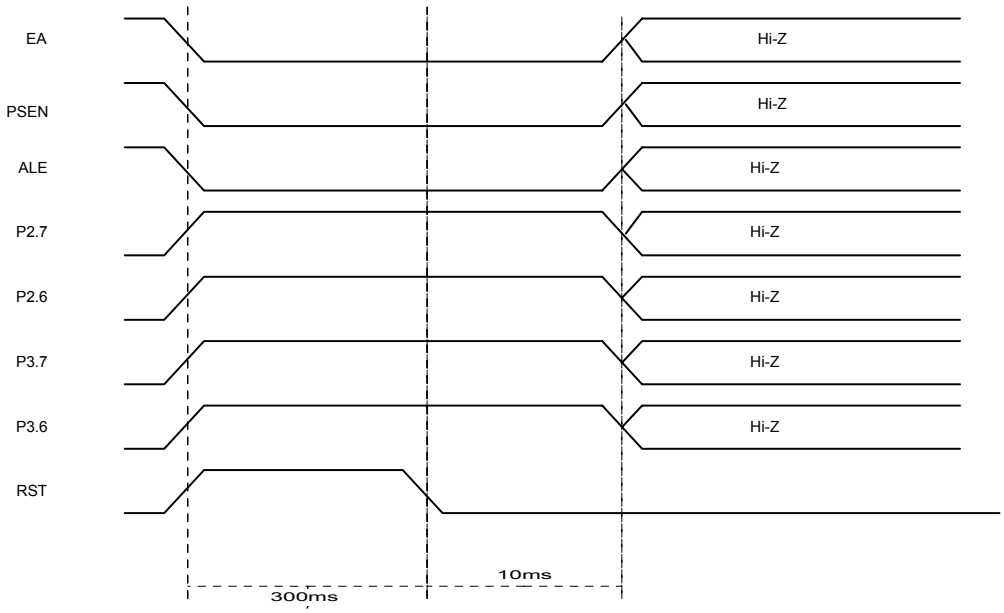
14.2 The Loader Program Locates at APFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #01H value before CPU has entered idle state. Set SFRCN register to update LDFlash or another bank of APFlash program. CPU will continue to run user's APFlash program after CPU has updated program. Please refer demonstrative code to understand other detail description.

15. H/W WRITER MODE

This mode is for the writer to write / read Flash EPROM operation. A general user may not enter this mode.

The Timing For Entering Flash EPROM Mode on the Programmer



16. SECURITY BITS

1. Using device programmer, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below. The W79E(L)532 has Special Setting Register which can be accessed by device programmer. The register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. If you needn't have ISP function, please don't fill "FF" code on LD memory. The writer always writes AP and LD flashs every time.

B7	B6	B5	B4	B3	B2	B1	B0

Security Bits

B7 : 1 -> XT > 24M hz, 0: XT < 24M hz.
B5 : 0 -> Eable H/W reboot with P4.3
B4 : 0 -> Enable H/W reboot with P2.6, P2.7
B1 : 0 -> MOVC Inhibited
B0 : 0 -> Data out lock
Default 1 for each bit.

Option Bits

B0: Lock bit

This bit is used to protect the customer's program code in the W79E(L)532. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

B1: MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

B4: H/W Reboot with P2.6 and P2.7

If this bit is set to logic 0, enable to reboot 4k LDFlash mode while RST =H, P2.6 = L and P2.7 = L state. CPU will start from LDFlash to update the user's program.

B5: H/W Reboot with P4.3

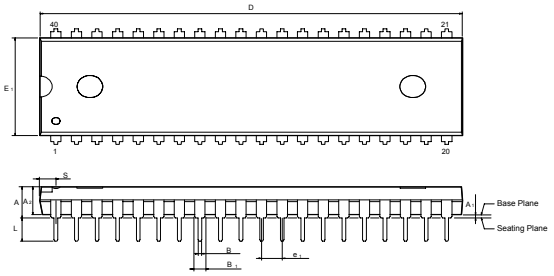
If this bit is set to logic 0, enable to reboot 4k LDFlash mode while RST =H and P4.3 = L state. CPU will start from LDFlash to update the user's program

B7: Select clock freqency.

If clock freqency is over 24M hz, then set this bit is H. If clock frequency is less than 24M hz, then clear this bit.

19. PACKAGE DIMENSIONS

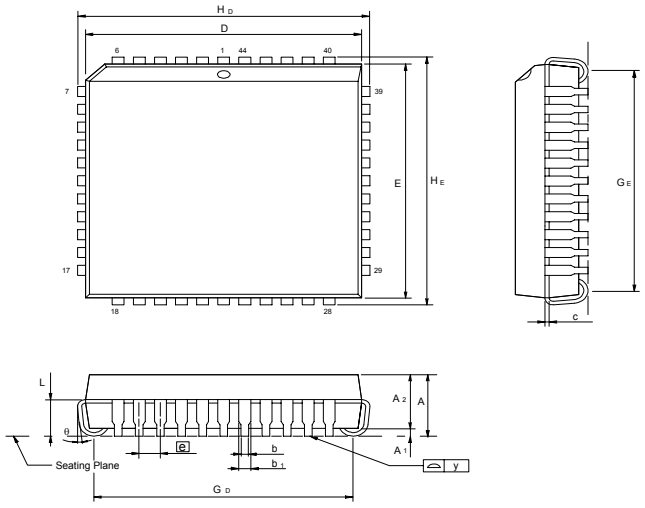
40-pin DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

```
;*******************************************************************************
; * VERIFY 64KB APFLASH BANK
;*******************************************************************************
        MOV  R4,#03H            ; ERROR COUNTER
        MOV  R6,#FDH            ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV  R7,#FFH
        MOV  TL0,R6
        MOV  TH0,R7
        MOV  DPTR,#0H           ; The start address of sample code
        MOV  R2,#0H             ; Target  low byte address
        MOV  R1,#0H             ; Target  high byte address
        MOV  SFRAH,R1           ; SFRAH, Target high address
        MOV  SFRCN,#00H         ; SFRCN = 00H, Read APFlash0
                                ; SFRCN = 80H , Read APFlash1

READ_VERIFY_64K:
        MOV  SFRAL,R2           ; SFRAL = LOW ADDRESS
        MOV  TCON,#10H          ; TCON = 10H, TR0 = 1,GO
        MOV  PCON,#01H
        INC  R2
        MOVX  A,@DPTR
        INC  DPTR
        CJNE  A,SFRFD,ERROR_64K
        CJNE  R2,#0H,READ_VERIFY_64K
        INC  R1
        MOV  SFRAH,R1
        CJNE  R1,#0H,READ_VERIFY_64K

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
        MOV  TA,#AAH
        MOV  TA,#55H
        MOV  CHPCON,#83H        ; SOFTWARE RESET. CPU will restart from APFlash0

ERROR_64K:
        DJNZ  R4,UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
.                               ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
                        .
                        .
                        .
```