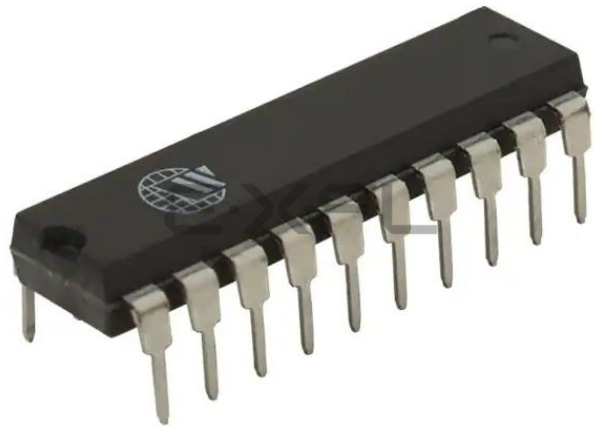

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## What is "Embedded - Microcontrollers"?

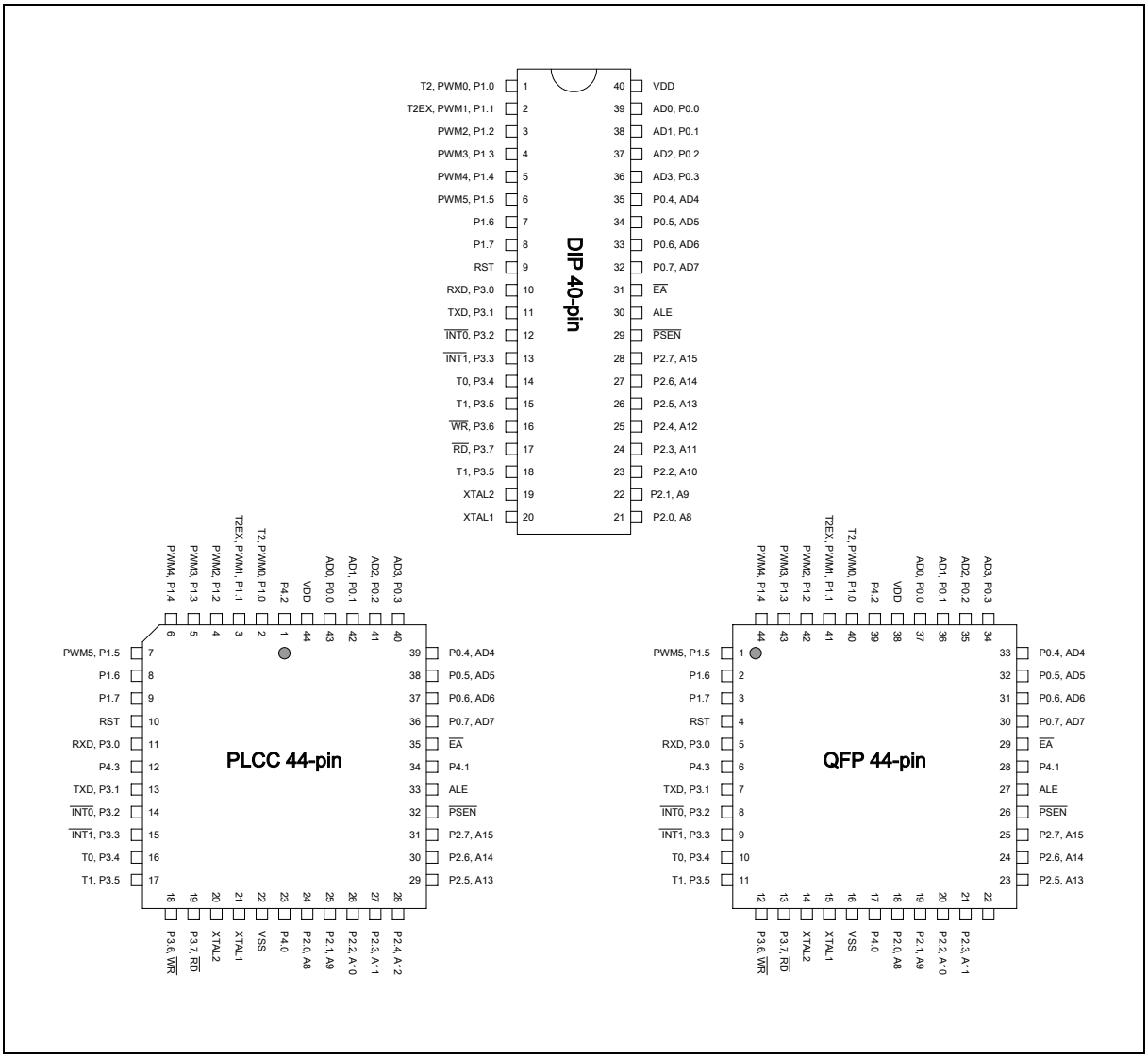
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8052 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | EBI/EMI, Serial Port |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79l532a25dl |

| DEVICE | OPERATING FREQUENCY | OPERATING VOLTAGE | PACKAGE |
|---|---|---|---|
| | | | LEAD FREE(RoHS) |
| W79E532 | up to 40MHz | 4.5V ~ 5.5V | DIP44, PLCC44, QFP44 |
| W79L532 | up to 20MHz | 3.0V ~ 5.5V | DIP44, PLCC44, QFP44 |

## 3. PIN CONFIGURATIONS



### Timers

The W79E(L)532 has three 16-bit timers that are functionally similar to the timers of the 8052 family. When used as timers, they can be set to run at either 4 clocks or 12 clocks per count, thus providing the user with the option of operating in a mode that emulates the timing of the original 8052. The W79E(L)532 has an additional feature, the watchdog timer. This timer is used as a System Monitor or as a very long time period timer.

### Interrupts

The Interrupt structure in the W79E(L)532 is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W79E(L)532 provides 7 interrupt resources with two priority level, including 2 external interrupt sources, timer interrupts, serial I/O interrupts.

### Power Management

Like the standard 80C52, the W79E(L)532 also has IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU core is stopped while the timers, serial port and interrupts clock continue to operate. In the POWER DOWN mode, all the clock are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

### On-chip Data SRAM

The W79E(L)532 has 1K Bytes of data space SRAM which is read/write accessible and is memory mapped. This on-chip MOVX SRAM is reached by the MOVX instruction. It is not used for executable program memory. There is no conflict or overlap among the 256 bytes Scratchpad RAM and the 1K Bytes MOVX SRAM as they use different addressing modes and separate instructions. The on-chip MOVX SRAM is enabled by setting the DME0 bit in the PMR register. After a reset, the DME0 bit is cleared such that the on-chip MOVX SRAM is disabled, and all data memory spaces 0000H – FFFFH access to the external memory.

| A16 | P1.0 | P1.1 | P1.2 | P1.3 | P1.4 | P1.5 | P1.6 | P1.7 |
|---|---|---|---|---|---|---|---|---|
| DCP12 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| DCP11 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| DCP10 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

**ISP Address Low Byte**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

Mnemonic: SFRAL Address: ACh

Low byte destination address for In System Programming operation. SFRAH and SFRAL address a specific ROM byte for erasure, programming or read.

**ISP Address High Byte**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |

Mnemonic: SFRAH Address: ADh

High byte destination address for In System Programming operation. SFRAH and SFRAL address a specific ROM byte for erasure, programming or read.

**ISP Data Buffer**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Mnemonic: SFRFD Address: AEh

In ISP mode, read/write a specific byte ROM content must go through SFRFD register.

**ISP Operation Modes**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | BANK | WFWIN | NOE | NCE | CTRL3 | CTRL2 | CTRL1 | CTRL0 |

Mnemonic: SFRCN Address: AFh

BANK: Select APFlash banks for ISP. Set it 1 access to APFlash1, clear it to APFlash0.

WFWIN: Destination ROM bank for programming, erasure and read. 0 = APFlashx, 1 = LDFlash.

NOE: Flash EPROM output enable.

NCE: Flash EPROM chip enable.

CTRL[3:0]: Mode Selection.

| ISP MODE | BANK | WFWIN | NOE | NCE | CTRL<3:0> | SFRAH, SFRAL | SFRFD |
|---|---|---|---|---|---|---|---|
| Erase 4KB LDFlash | 0 | 1 | 1 | 0 | 0010 | X | X |
| Erase 64K APFlash0 | 0 | 0 | 1 | 0 | 0010 | X | X |
| Erase 64K APFlash1 | 1 | 0 | 1 | 0 | 0010 | X | X |
| Program 4KB LDFlash | 0 | 1 | 1 | 0 | 0001 | Address in | Data in |
| Program 64KB APFlash0 | 0 | 0 | 1 | 0 | 0001 | Address in | Data in |
| Program 64KB APFlash1 | 1 | 0 | 1 | 0 | 0001 | Address in | Data in |
| Read 4KB LDFlash | 0 | 1 | 0 | 0 | 0000 | Address in | Data out |
| Read 64KB APFlash0 | 0 | 0 | 0 | 0 | 0000 | Address in | Data out |
| Read 64KB APFlash1 | 1 | 0 | 0 | 0 | 0000 | Address in | Data out |

**Port 3**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | P3.7 | P3.6 | P3.5 | P3.4 | P3.3 | P3.2 | P3.1 | P3.0 |

Mnemonic: P3 Address: B0h

P3.7-0: General purpose I/O port. Each pin also has an alternate input or output function. The alternate functions are described below.

| | | |
|---|---|---|
| P3.7 | $\overline{RD}$ | Strobe for read from external RAM |
| P3.6 | $\overline{WR}$ | Strobe for write to external RAM |
| P3.5 | T1 | Timer/counter 1 external count input |
| P3.4 | T0 | Timer/counter 0 external count input |
| P3.3 | $\overline{INT1}$ | External interrupt 1 |
| P3.2 | $\overline{INT0}$ | External interrupt 0 |
| P3.1 | TxD | Serial port 0 output |
| P3.0 | RxD | Serial port 0 input |

**Interrupt Priority**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

Mnemonic: IP Address: B8h

IP.7: This bit is un-implemented and will read high.
PT2: This bit defines the Timer 2 interrupt priority. PT2 = 1 sets it to higher priority level.
PS: This bit defines the Serial port 0 interrupt priority. PS = 1 sets it to higher priority level.
PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.
PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.
PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.
PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

# 7. INSTRUCTION

The W79E(L)532 executes all the instructions of the standard 8032 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W79E(L)532, each machine cycle consists of 4 clock periods, while in the standard 8032 it consists of 12 clock periods. Also, in the W79E(L)532 there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8032 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the W79E(L)532 has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W79E(L)532 reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8032.

## 7.1 Instruction Timing

The instruction timing for the W79E(L)532 is an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the W79E(L)532 and the standard 8032. In the W79E(L)532 each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2 C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the W79E(L)532 does one op-code fetch per machine cycle. Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the W79E(L)532 are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8032, the MOVX instruction is always two machine cycles long. However in the W79E(L)532, the user has a facility to stretch the duration of this instruction from 2 machine cycles to 9 machine cycles. The $\overline{RD}$ and $\overline{WR}$ strobe lines are also proportionately elongated. This gives the user flexibility in accessing both fast and slow peripherals without the use of external circuitry and with minimum software overhead. The rest of the instructions are either three, four or five machine cycle instructions. Note that in the W79E(L)532, based on the number of machine cycles, there are five different types, while in the standard 8032 there are only three. However, in the W79E(L)532 each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8032. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8032 in terms of clock periods.

## 8. POWER MANAGEMENT

The W79E(L)532 has several features that help the user to control the power consumption of the device. The power saving features are basically the POWER DOWN mode and the IDLE mode of operation.

### Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the Idle state. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine(ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W79E(L)532 is exiting from an Idle mode with a reset, the instruction following the one which put the device into Idle mode is not executed. So there is no danger of unexpected writes.

### Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and $\overline{\text{PSEN}}$ pins are pulled low. The port pins output the values held by their respective SFRs.

The W79E(L)532 will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detect. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W79E(L)532 can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the low level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after the one which put the device into Power Down mode and continues from there.

## 9. INTERRUPTS

The W79E(L)532 has a two priority level interrupt structure with 11 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

### Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts.

### Priority Level Structure

There are three priority levels for the interrupts, highest, high and low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

**Table 7. Priority structure of interrupts**

| SOURCE | FLAG | VECTOR ADDRESS | PRIORITY LEVEL |
|---|---|---|---|
| External Interrupt 0 | IE0 | 0003h | 1(highest) |
| Timer 0 Overflow | TF0 | 000Bh | 2 |
| External Interrupt 1 | IE1 | 0013h | 3 |
| Timer 1 Overflow | TF1 | 001Bh | 4 |
| Serial Port | RI + TI | 0023h | 5 |
| Timer 2 Overflow | TF2 + EXF2 | 002Bh | 6 |
| Watchdog Timer | WDIF | 0063h | 7 (lowest) |

## 10.2 Timer/Counter 2

Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/T2 = 1) or the crystal oscillator, which is divided by 12 or 4 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

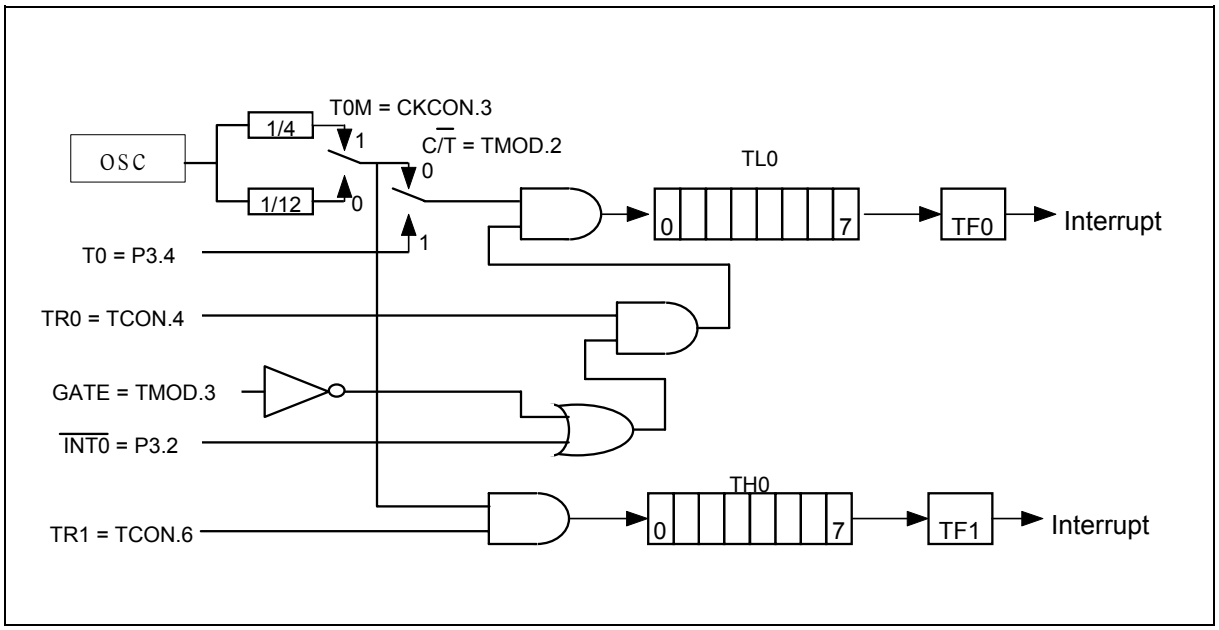



Figure 13. Timer/Counter 0 Mode 3

### Capture Mode

The capture mode is enabled by setting the CP / $\overline{RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will also generate an interrupt. Setting the T2CR bit (T2MOD.3), the W79E(L)532 allows hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured.

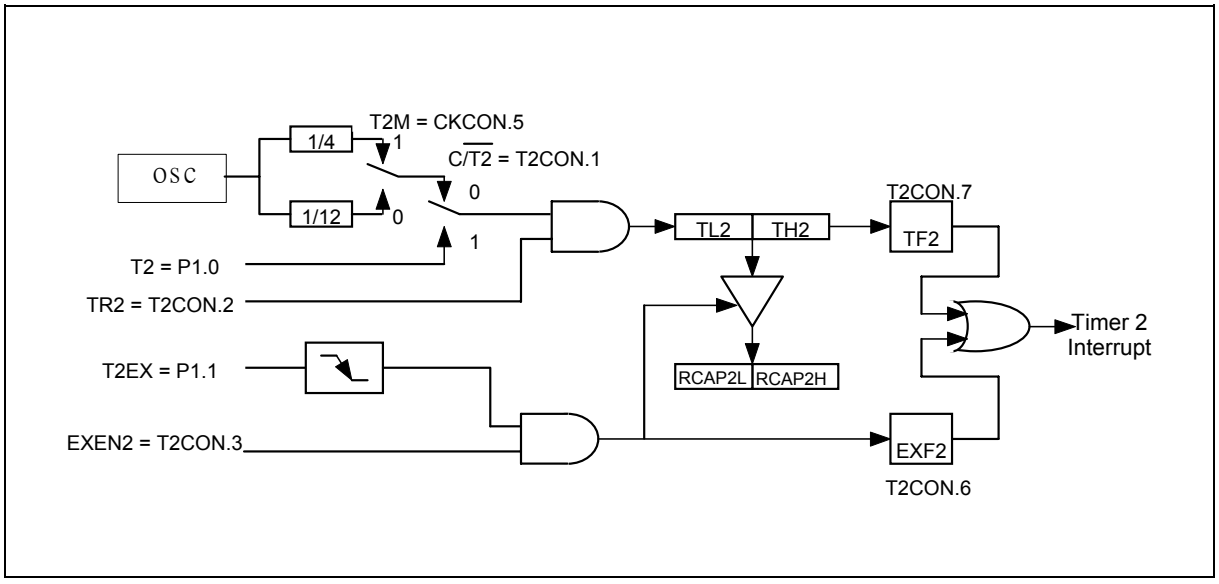



Figure 14. 16-Bit Capture Mode

### Auto-reload Mode, Counting up

The auto-reload mode as an up counter is enabled by clearing the CP / $\overline{RL2}$ bit in the T2CON register and clearing the DCEN bit in T2MOD register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

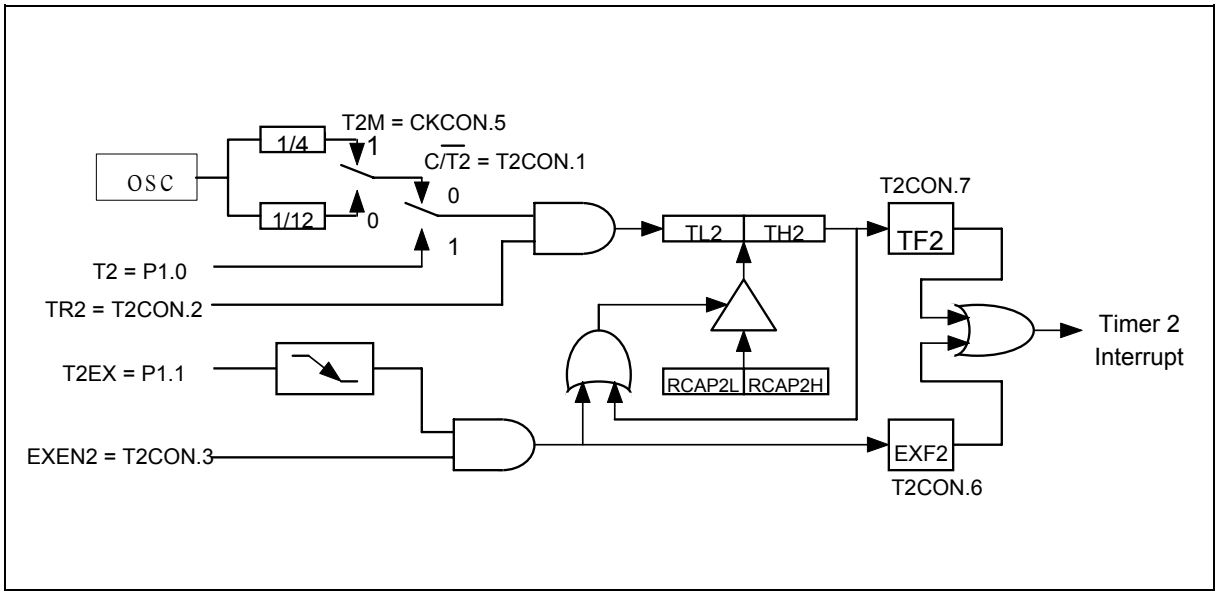



Figure 15. 16-Bit Auto-reload Mode, Counting Up

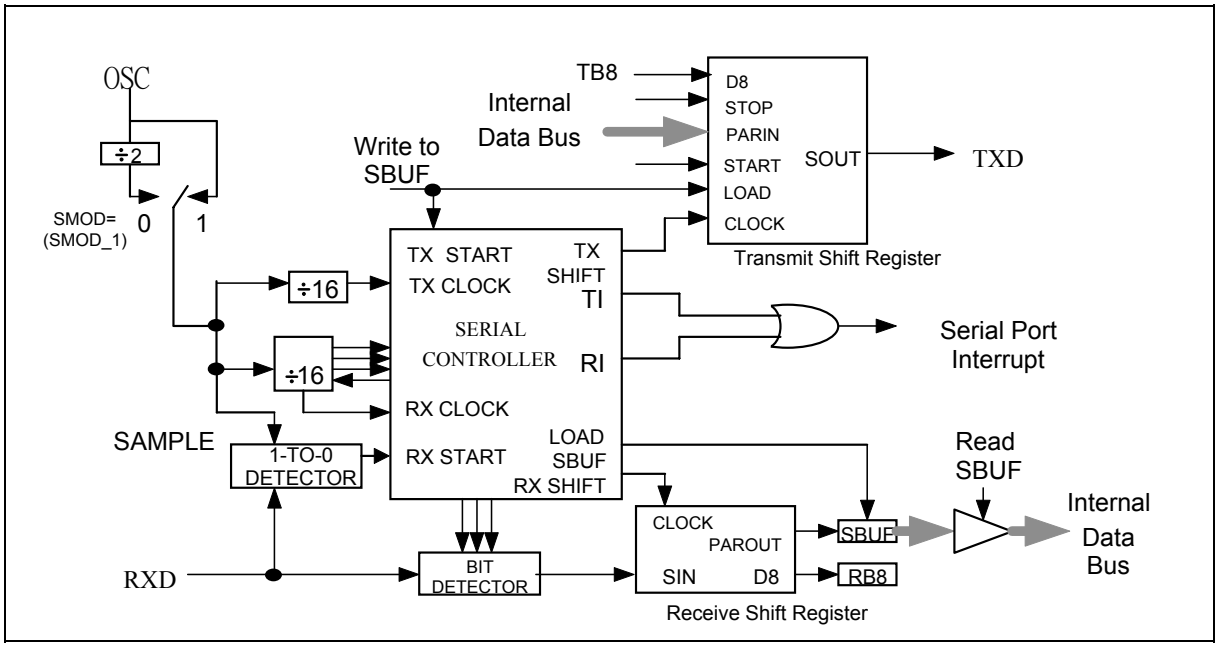



Figure 22. Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

**Mode 3**

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

## 11.1 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W79E(L)532 has the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE(FE_1) bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W79E(L)532 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

## 11.2 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the W79E(L)532, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100
SADEN 1111 1010
Given 1010 0x0x

Slave 2:

SADDR 1010 0111
SADEN 1111 1001
Given 1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical ORing of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

## 12. TIMED ACCESS PROTECTION

The W79E(L)532 has several new features, like the Watchdog timer, on-chip ROM size adjustment, wait state control signal and Power on/fail reset flag, which are crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E(L)532 has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access(TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG    0C7h          ;define new register TA, located at 0C7h
MOV     TA, #0AAh
MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

**Examples of Timed Assessing are shown below.**

Example 1: Valid access

```
MOV     TA, #0AAh       3 M/C          Note: M/C = Machine Cycles
MOV     TA, #055h       3 M/C
MOV     WDCON, #00h     3 M/C
```

Example 2: Valid access

```
MOV     TA, #0AAh       3 M/C
MOV     TA, #055h       3 M/C
NOP                     1 M/C
SETB    EWT             2 M/C
```

Example 3: Valid access

```
MOV     TA, #0Aah       3 M/C
MOV     TA, #055h       3 M/C
ORL     WDCON, #00000010B  3M/C
```

## 14. IN-SYSTEM PROGRAMMING

### 14.1 The Loader Program Locates at LDFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #03H value before CPU has entered idle state. CPU will switch to LDFlash memory and execute a reset action. H/W reboot mode will switch to LDFlash memory, too. Set SFRCN register where it locates at user's loader program to update APFlash bank 0 or bank 1 memory. Set a SWRESET (CHPCON.7) to switch back APFlash after CPU has updated APFlash program. CPU will restart to run program from reset state.

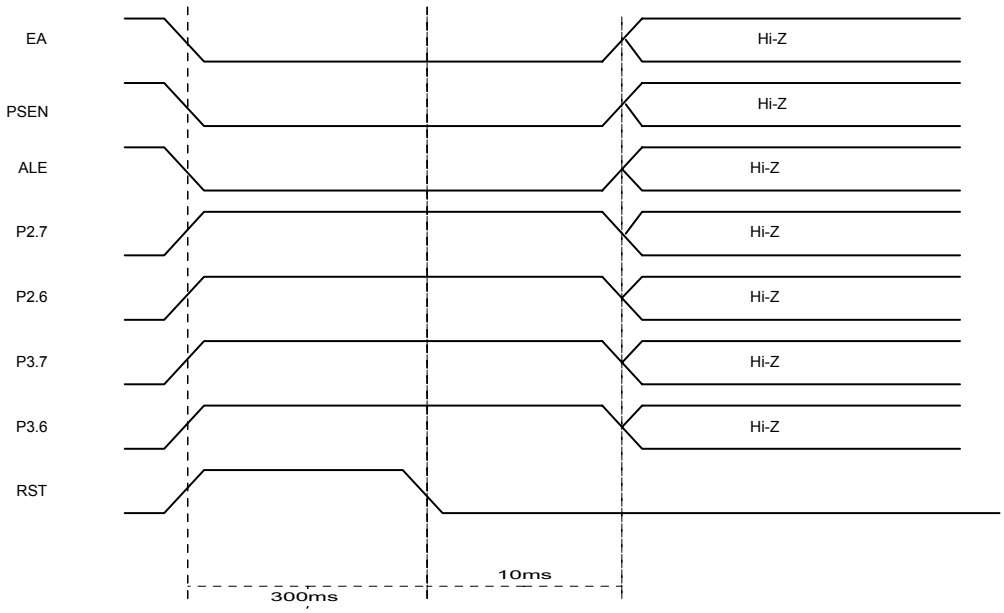
### 14.2 The Loader Program Locates at APFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #01H value before CPU has entered idle state. Set SFRCN register to update LDFlash or another bank of APFlash program. CPU will continue to run user's APFlash program after CPU has updated program. Please refer demonstrative code to understand other detail description.

## 15. H/W WRITER MODE

This mode is for the writer to write / read Flash EPROM operation. A general user may not enter this mode.

**The Timing For Entering Flash EPROM Mode on the Programmer**



# 17. ELECTRICAL CHARACTERISTICS

## 17.1 Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITION | RATING | UNIT |
|---|---|---|---|---|
| DC Power Supply | $V_{DD} - V_{SS}$ | -0.3 | +7.0 | V |
| Input Voltage | $V_{IN}$ | $V_{SS}$ -0.3 | $V_{DD}$ +0.3 | V |
| Operating Temperature | $T_A$ | 0 | +70 | °C |
| Storage Temperature | Tst | -55 | +150 | °C |

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 17.2 DC Characteristics

($T_A$ = 25°C, unless otherwise specified.)

| PARAMETER | SYM. | SPECIFICATION | | | TEST CONDITIONS |
|---|---|---|---|---|---|
| | | MIN. | MAX. | UNIT | |
| Operating Voltage | $V_{DD}$ | 3.0 | 5.5 | V | $V_{DD}$ >4.5V→Fosc < = 40 MHz<br>$V_{DD}$ >3.0V→Fosc < = 20 MHz |
| Operating Current | $I_{DD}$ | - | 30 | mA | $V_{DD}$ = 5.5V, Fosc = 20 MHz |
| | | | 10 | mA | $V_{DD}$ = 3.3V, Fosc = 12 MHz |
| Idle Current | $I_{IDLE}$ | - | 13 | mA | $V_{DD}$ = 5.5V, Fosc=20 MHz |
| | | | 5 | mA | $V_{DD}$ = 3.3V, Fosc=12 MHz |
| Power Down Current | $I_{PWDN}$ | - | 10 | µA | $V_{DD}$ = 3.3 ~ 5.5V |
| Input Current P1, P2, P3 | $I_{IN1}$ | -50 | +10 | µA | $V_{DD}$ = 3.3 ~ 5.5V<br>$V_{IN}$ = 0V or $V_{DD}$ |
| Input Current RST[*1] | $I_{IN2}$ | - | 900 | µA | $V_{DD}$ = 5.5V, 0<$V_{IN}$<$V_{DD}$ |
| | | - | 500 | µA | $V_{DD}$ = 3.3V, 0<$V_{IN}$<$V_{DD}$ |
| Input Leakage Current P0, $\overline{EA}$ | $I_{LK}$ | -10 | +10 | µA | $V_{DD}$ = 3.3 ~ 5.5V<br>0V<$V_{IN}$<$V_{DD}$ |
| Logic 1 to 0 Transition Current P1, P2, P3 | $I_{TL}$[*4] | -500 | -200 | µA | $V_{DD}$ = 5.5V $V_{IN}$ = 2.0V |
| | | -250 | -50 | µA | $V_{DD}$ = 3.3V $V_{IN}$ = 1.0V |
| Input Low Voltage P0, P1, P2, P3, $\overline{EA}$ | $V_{IL1}$ | 0 | 0.8 | V | $V_{DD}$ = 4.5V |
| | | 0 | 0.5 | V | $V_{DD}$ =3.3V |
| Input Low Voltage RST[*1] | $V_{IL2}$ | 0 | 0.8 | V | $V_{DD}$ = 4.5V |
| | | 0 | 0.5 | V | $V_{DD}$ = 3.3V |
| Input Low Voltage XTAL1[*3] | $V_{IL3}$ | 0 | 0.8 | V | $V_{DD}$ = 4.5V |
| | | 0 | 0.5 | V | $V_{DD}$ = 3.3V |

DC Characteristics, continued

| PARAMETER | SYM. | SPECIFICATION | | | TEST CONDITIONS |
|---|---|---|---|---|---|
| | | MIN. | MAX. | UNIT | |
| Input High Voltage P0, P1, P2, P3, $\overline{EA}$ | $V_{IH1}$ | 2.4 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| | | 1.8 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 3.3V |
| Input High Voltage RST | $V_{IH2}$ | 3.0 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| | | 2.0 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 3.3V |
| Input High Voltage XTAL1[*3] | $V_{IH3}$ | 3.5 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 5.5V |
| | | 2.0 | $V_{DD}$ +0.2 | V | $V_{DD}$ = 3.3V |
| Sink current P1, P3 | Isk1 | 6 | 9 | mA | $V_{DD}$ = 4.5V, $V_{OL}$ = 0.45 |
| | | 3.8 | 7 | mA | $V_{DD}$ = 3.3V, $V_{OL}$ = 0.4 |
| Sink current P0,P2, ALE, $\overline{PSEN}$ | Isk2 | 10 | 14 | mA | $V_{DD}$ = 4.5V , $V_{OL}$ = 0.45V |
| | | 6.5 | 9.5 | mA | $V_{DD}$ = 3.3V, $V_{OL}$=0.4 |
| Source current P1, P2 (I/O), P3 | Isr1 | -200 | -360 | uA | $V_{DD}$ = 4.5V, $V_{OL}$ = 2.4V |
| | | -100 | -220 | uA | $V_{DD}$ = 3.3V, $V_{OL}$ = 1.4V |
| Source current P0,P2 (address), ALE, $\overline{PSEN}$ | Isr2 | -10 | -14 | mA | $V_{DD}$ = 4.5V, $V_{OL}$ = 2.4V |
| | | -6 | -9 | mA | $V_{DD}$ = 3.3V, $V_{OL}$ = 1.4V |
| Output Low Voltage P1, P2 (I/O), P3 | $V_{OL1}$ | - | 0.45 | V | $V_{DD}$ = 4.5V, $I_{OL}$ = +6 mA |
| | | - | 0.4 | V | $V_{DD}$ = 3.3V, $I_{OL}$ = +3.8 mA |
| Output Low Voltage P0, P2(address), ALE, $\overline{PSEN}$ [*2] | $V_{OL2}$ | - | 0.45 | V | $V_{DD}$ = 4.5V, $I_{OL}$ = +10 mA |
| | | - | 0.4 | V | $V_{DD}$ = 3.3V, $I_{OL}$ = +6.5 mA |
| Output High Voltage P1, P3 | $V_{OH1}$ | 2.4 | - | V | $V_{DD}$ = 4.5V, $I_{OH}$ = -200 μA |
| | | 1.4 | - | V | $V_{DD}$ = 3.3V, $I_{OL}$ = -100 uA |
| Output High Voltage P0, P2, ALE, $\overline{PSEN}$ [*2] | $V_{OH2}$ | 2.4 | - | V | $V_{DD}$ = 4.5V, $I_{OH}$ = -10mA |
| | | 1.4 | - | V | $V_{DD}$ = 3.3V, $I_{OL}$ = -6 mA |

**Notes:**

*1. RST pin is a Schmitt trigger input.

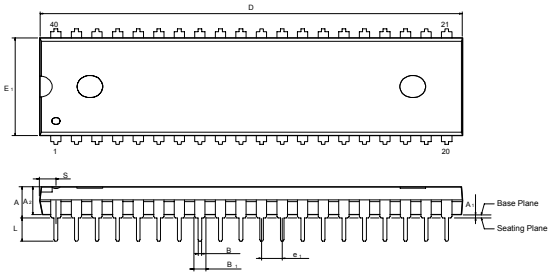
*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN approximates to 2V.

# 19. PACKAGE DIMENSIONS

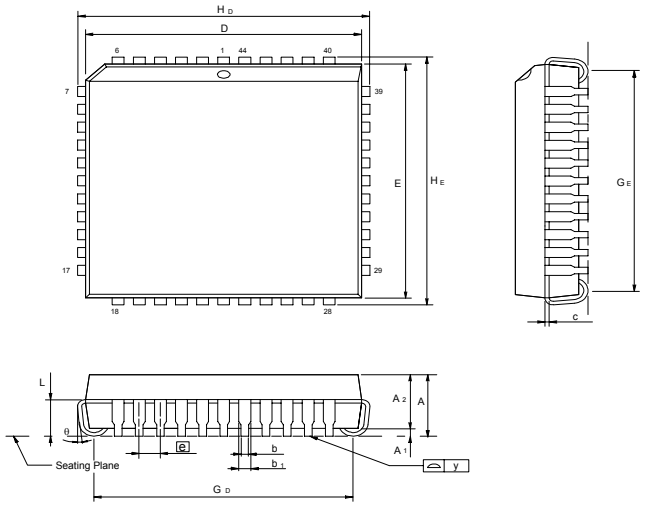
## 40-pin DIP




| Symbol | Dimension in inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.210 | — | — | 5.334 |
| $A_1$ | 0.010 | — | — | 0.254 | — | — |
| $A_2$ | 0.150 | 0.155 | 0.160 | 3.81 | 3.937 | 4.064 |
| B | 0.016 | 0.018 | 0.022 | 0.406 | 0.457 | 0.559 |
| $B_1$ | 0.048 | 0.050 | 0.054 | 1.219 | 1.27 | 1.372 |
| c | 0.008 | 0.010 | 0.014 | 0.203 | 0.254 | 0.356 |
| D | — | 2.055 | 2.070 | — | 52.20 | 52.58 |
| E | 0.590 | 0.600 | 0.610 | 14.986 | 15.24 | 15.494 |
| $E_1$ | 0.540 | 0.545 | 0.550 | 13.72 | 13.84 | 13.97 |
| $e_1$ | 0.090 | 0.100 | 0.110 | 2.286 | 2.54 | 2.794 |
| L | 0.120 | 0.130 | 0.140 | 3.048 | 3.302 | 3.556 |
| a | 0 | — | 15 | 0 | — | 15 |
| $e_A$ | 0.630 | 0.650 | 0.670 | 16.00 | 16.51 | 17.01 |
| S | — | — | 0.090 | — | — | 2.286 |

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

## 44-pin PLCC




| Symbol | Dimension in inches | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.185 | — | — | 4.699 |
| $A_1$ | 0.020 | — | — | 0.508 | — | — |
| $A_2$ | 0.145 | 0.150 | 0.155 | 3.683 | 3.81 | 3.937 |
| $b_1$ | 0.026 | 0.028 | 0.032 | 0.66 | 0.711 | 0.813 |
| b | 0.016 | 0.018 | 0.022 | 0.406 | 0.457 | 0.559 |
| c | 0.008 | 0.010 | 0.014 | 0.203 | 0.254 | 0.356 |
| D | 0.648 | 0.653 | 0.658 | 16.46 | 16.59 | 16.71 |
| E | 0.648 | 0.653 | 0.658 | 16.46 | 16.59 | 16.71 |
| e | 0.050 BSC | | | 1.27 BSC | | |
| $G_D$ | 0.590 | 0.610 | 0.630 | 14.99 | 15.49 | 16.00 |
| $G_E$ | 0.590 | 0.610 | 0.630 | 14.99 | 15.49 | 16.00 |
| $H_D$ | 0.680 | 0.690 | 0.700 | 17.27 | 17.53 | 17.78 |
| $H_E$ | 0.680 | 0.690 | 0.700 | 17.27 | 17.53 | 17.78 |
| L | 0.090 | 0.100 | 0.110 | 2.296 | 2.54 | 2.794 |
| y | — | — | 0.004 | — | — | 0.10 |

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

## 21. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A1 | June 24, 2004 | - | Initial Issued |
| A2 | Sep 14, 2004 | 6 | Modify block diagram. |
| | | 8 | Remove economy mode. |
| | | 68 | Modify Figure A. |
| A3 | April 19, 2005 | 76 | Add Important Notice |
| A4 | Aug 11, 2005 | 2, 5, 12 | Add Port 0 pull-up resisters information |
| | | 62 | Remove encrypt function of Security bits B2 description |
| | | 2, 3 | Add Lead Free package. |
| A5 | November 21, 2005 | - | Add wide voltage device (W79L532) |
| | | 3 | Add device list. |
| | | 42 | Revise the diagram of timer2 baud rate generator mode. |
| | | 44 | Revise the diagram of PWM |
| | | 53 | Revise the diagram of serial port mode 2. |
| | | 56 | Modify the explanation to the TA protection example. |
| | | 61 | Modify DC characteristic. |
| | | 68 | Modify application circuit |
| A6 | November 6, 2006 | - | Remove block diagram. |
| | | 2 | Remove all Leaded package parts. |
| | | 3, 62 | Revise Operating speed to 20MHz on W79L532 |
| A7 | January 03, 2007 | 64,65 | Add test condition in AC specification. |
| | | | |
| | | | |

## Important Notice

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**Headquarters**
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

**Taipei Office**
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

**Winbond Electronics Corporation America**
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

**Winbond Electronics Corporation Japan**
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

**Winbond Electronics (Shanghai) Ltd.**
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

**Winbond Electronics (H.K.) Ltd.**
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064