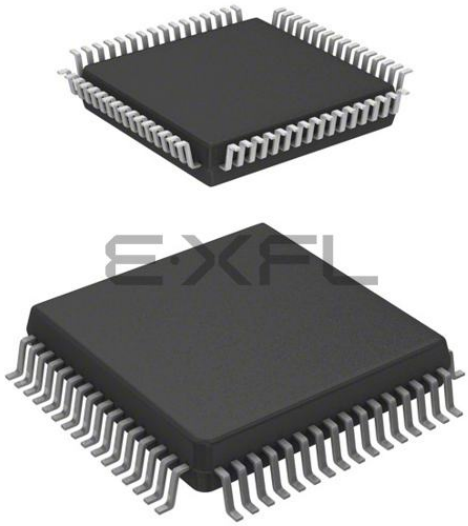

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Number of I/O	24
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Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	528 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
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LIST OF FIGURES

If a second word is to be erased, it is important that the E1LAT bit be reset before restarting the erasing sequence, otherwise any write to a new address will have no effect. This condition provides a higher degree of security for the stored data.

User programs must be running from the RAM or ROM as the EEPROM will have its address and data buses latched.

3.5.4 EEPROM programming operation

To program a byte of EEPROM, the following steps should be taken:

1. Set the E1LAT bit.
2. Write address/data to the EEPROM address to be programmed.
3. Set the E1PGM bit.
4. Wait for time t_{PROG1}.
5. Reset the E1LAT bit (to logic zero).

While a programming operation is being performed, any access of the EEPROM array will not be successful.

Warning: To program a byte correctly, it has to have been previously erased.

If a second word is to be programmed, it is important that the E1LAT bit be reset before restarting the programming sequence otherwise any write to a new address will have no effect. This condition provides a higher degree of security for the stored data.

User programs must be running from the RAM or ROM as the EEPROM will have its address and data buses latched.

Note: 224 bytes of EEPROM (address $0120 to $01FF) can be program and erase protected under the control of bit 1 of the OPTR register detailed in Section 3.5.5.

3.5.5 Options register (OPTR)

This register (OPTR), located at $0100, contains the secure and protect functions for the EEPROM and allows the user to select options in a non-volatile manner. The contents of the OPTR register are loaded into data latches with each power-on or external reset.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$0100							EE1P	SEC	Not affected

(1) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

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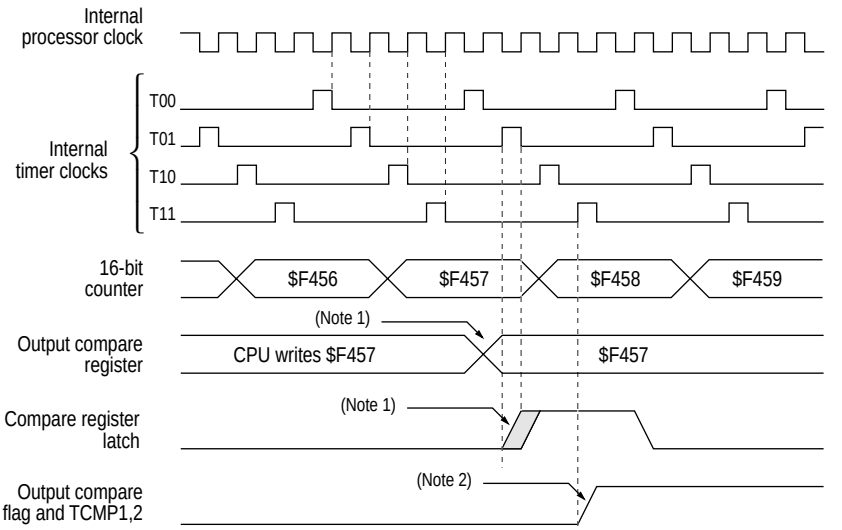
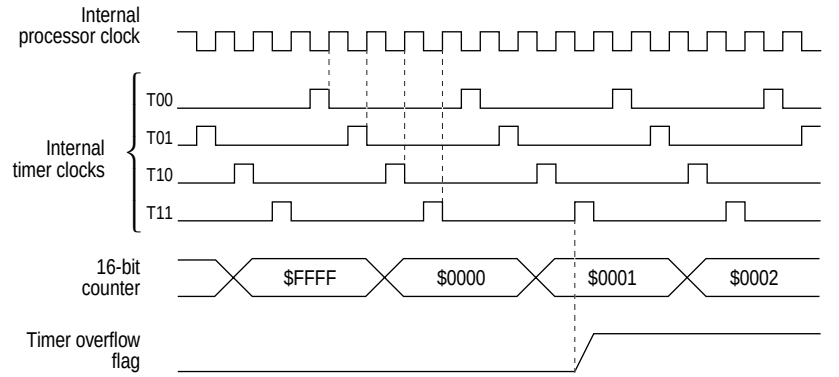


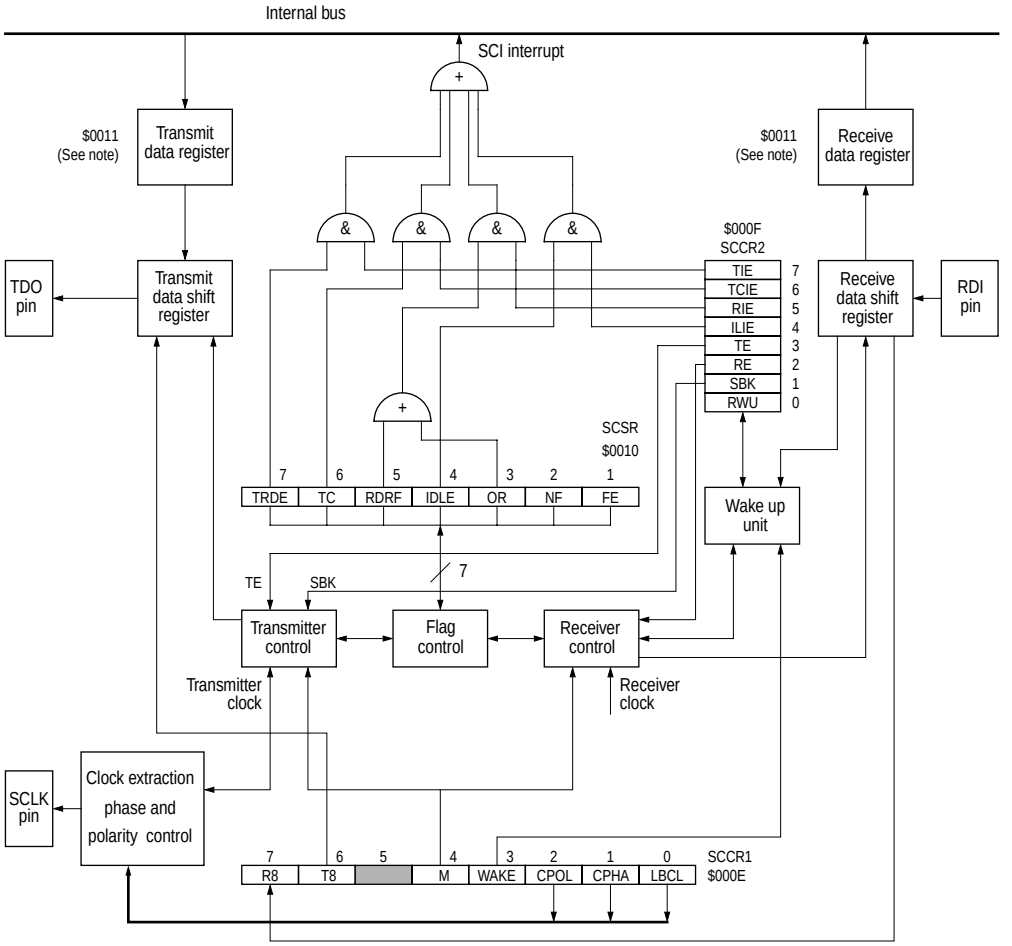
Note: The CPU write to the compare registers may take place at any time, but a compare only occurs at timer state T01. Thus a four cycle difference may exist between the write to the compare register and the actual compare.

Figure 6-4 Timer state timing diagram for output compare



Note: The timer overflow flag is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by a read of the timer status register during the internal processor clock high time, followed by a read of the counter low register.

Figure 6-5 Timer state timing diagram for timer overflow



Note: The serial communications data register (SCI SCDR) is controlled by the internal R/$\overline{W}$ signal. It is the transmit data register when written to and the receive data register when read.

Figure 7-1 Serial communications interface block diagram

7.10 SCI synchronous transmission

The SCI transmitter allows the user to control a one way synchronous serial transmission. The SCLK pin is the clock output of the SCI transmitter. No clocks are sent to that pin during start bit and stop bit. Depending on the state of the LBCL bit (bit 0 of SCCR1), clocks will or will not be activated during the last valid data bit (address mark). The CPOL bit (bit 2 of SCCR1) allows the user to select the clock polarity, and the CPHA bit (bit 1 of SCCR1) allows the user to select the phase of the external clock (see Figure 7-8, Figure 7-9 and Figure 7-10).

During idle, preamble and send break, the external SCLK clock is not activated.

These options allow the user to serially control peripherals which consist of shift registers, without losing any functions of the SCI transmitter which can still talk to other SCI receivers. These options do not affect the SCI receiver which is independent of the transmitter.

The SCLK pin works in conjunction with the TDO pin. When the SCI transmitter is disabled (TE = 0), the SCLK and TDO pins go to the high impedance state.

Note: The LBCL, CPOL and CPHA bits have to be selected before enabling the transmitter to ensure that the clocks function correctly. These bits should not be changed while the transmitter is enabled.

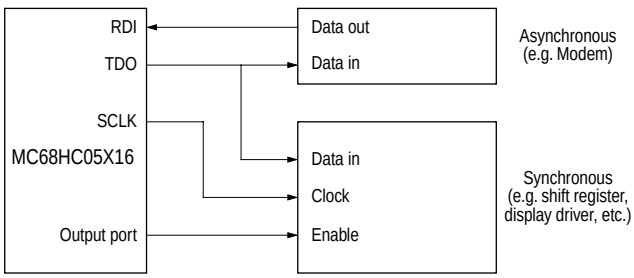


Figure 7-8 SCI example of synchronous and asynchronous transmission

7.11.3 Serial communications control register 2 (SCCR2)

The SCI control register 2 (SCCR2) provides the control bits that enable/disable individual SCI functions.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
SCI control (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000

TIE — Transmit interrupt enable

1 (set) – TDRE interrupts enabled.

0 (clear) – TDRE interrupts disabled.

TCIE — Transmit complete interrupt enable

1 (set) – TC interrupts enabled.

0 (clear) – TC interrupts disabled.

RIE — Receiver interrupt enable

1 (set) – RDRF and OR interrupts enabled.

0 (clear) – RDRF and OR interrupts disabled.

ILIE — Idle line interrupt enable

1 (set) – IDLE interrupts enabled.

0 (clear) – IDLE interrupts disabled.

TE — Transmitter enable

When the transmit enable bit is set, the transmit shift register output is applied to the TDO line and the corresponding clocks are applied to the SCLK pin. Depending on the state of control bit M (SCCR1), a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted when software sets the TE bit from a cleared state.

If a transmission is in progress and a zero is written to TE, the transmitter will wait until after the present byte has been transmitted before placing the TDO and the SCLK pin in the idle, high impedance state.

If the TE bit has been written to a zero and then set to a one before the current byte is transmitted, the transmitter will wait for that byte to be transmitted and will then initiate transmission of a new preamble. After this latest transmission, and provided the TDRE bit is set (no new data to transmit), the line remains idle (driven high while TE = 1); otherwise, normal transmission occurs. This function allows the user to neatly terminate a transmission sequence.

Table 7-9 SCI transmit baud rate output for a given prescaler output

SCT/SCR bits			Divide by	Representative highest prescaler baud rate output				
Bit 2	Bit 1	Bit 0		131072	32768	38400	19200	9600
0	0	0	1	131072	32768	38400	19200	9600
0	0	1	2	65536	16384	19200	9600	4800
0	1	0	4	32768	8192	9600	4800	2400
0	1	1	8	16384	4096	4800	2400	1200
1	0	0	16	8192	2048	2400	1200	600
1	0	1	32	4096	1024	1200	600	300
1	1	0	64	2048	512	600	300	150
1	1	1	128	1024	256	300	150	75

Note: The examples shown in Table 7-6, Table 7-7, Table 7-8 and Table 7-9 do not apply when the part is operating in slow mode (see Section 2.2.3).
For the receiver, the internal clock frequency is 16 times higher than the selected baud rate.

7.13 SCI during STOP mode

When the MCU enters STOP mode, the baud rate generator driving the receiver and transmitter is shut down. This stops all SCI activity. Both the receiver and the transmitter are unable to operate.

If the STOP instruction is executed during a transmitter transfer, that transfer is halted. When STOP mode is exited as a result of an external interrupt, that particular transmission resumes.

If the receiver is receiving data when the STOP instruction is executed, received data sampling is stopped (baud generator stops) and the rest of the data is lost.

Warning: For the above reasons, all SCI transactions should be in the idle state when the STOP instruction is executed.

7.14 SCI during WAIT mode

The SCI system is not affected by WAIT mode and continues normal operation. Any valid SCI interrupt will wake-up the system. If required, the SCI system can be disabled prior to entering WAIT mode by writing a zero to the transmitter and receiver enable bits in the serial communication control register 2 at $000F. This action will result in a reduction of power consumption during WAIT mode.

The A/D reference input (AN0–AN7) is applied to a precision internal D/A converter. Control logic drives this D/A converter and the analog output is successively compared with the analog input sampled at the beginning of the conversion. The conversion is monotonic with no missing codes.

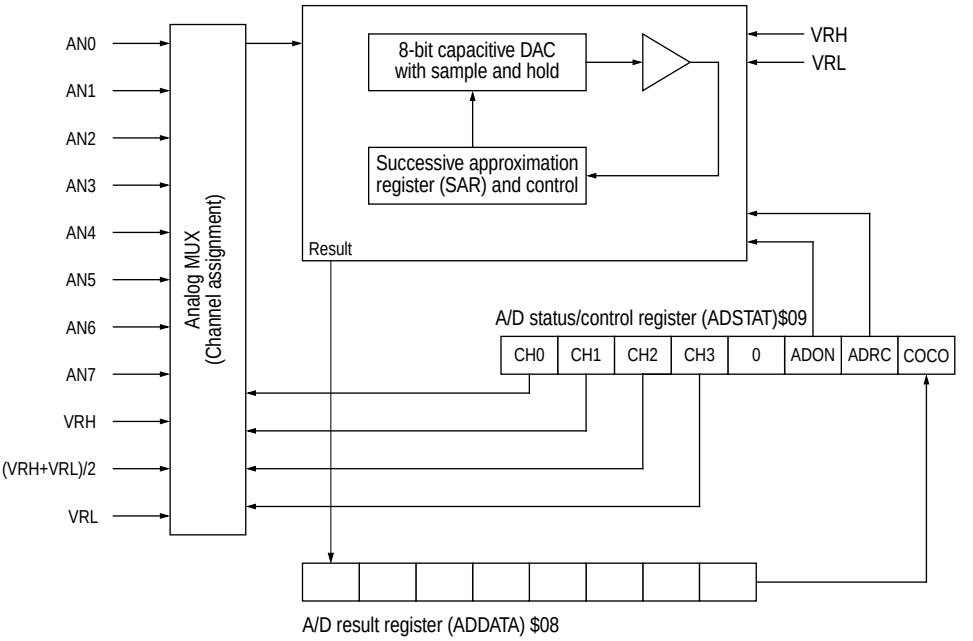


Figure 9-1 A/D converter block diagram

The result of each successive comparison is stored in the SAR and, when the conversion is complete, the contents of the SAR are transferred to the read-only result data register ($08), and the conversion complete flag, COCO, is set in the A/D status/control register ($09).

Warning: Any write to the A/D status/control register will abort the current conversion, reset the conversion complete flag and start a new conversion on the selected channel.

At power-on or external reset, both the ADRC and ADON bits are cleared; thus the A/D is disabled.

9.2.3 A/D status/control register (ADSTAT)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000

COCO — Conversion complete flag

1 (set) – COCO is set each time a conversion is complete, allowing the new result to be read from the A/D result data register ($08). The converter then starts a new conversion.

0 (clear) – COCO is cleared by reading the result data register or writing to the status/control register.

Reset clears the COCO flag.

ADRC — A/D RC oscillator control

The ADRC bit allows the user to control the A/D RC oscillator, which is used to provide a sufficiently high clock rate to the A/D to ensure accuracy when the chip is running at low speeds.

1 (set) – When the ADRC bit is set, the A/D RC oscillator is turned on and, if ADON is set, the A/D runs from the RC oscillator clock. See Table 9-1.

0 (clear) – When the ADRC bit is cleared, the A/D RC oscillator is turned-off and, if ADON is set, the A/D runs from the CPU clock.

When the A/D RC oscillator is turned on, it takes a time t_{ADRC} to stabilize (see Table 12-3). During this time A/D conversion results may be inaccurate.

Note: If the MCU bus clock falls below 1MHz, the A/D RC oscillator should be switched on.

Power-on or external reset clears the ADRC bit.

Table 9-1 A/D clock selection

ADRC	ADON	RC oscillator	A/D converter	Comments
0	0	OFF	OFF	A/D switched off.
0	1	OFF	ON	A/D using CPU clock.
1	0	ON	OFF	Allows the RC oscillator to stabilize.
1	1	ON	ON	A/D using RC oscillator clock.

10.2.1 Interrupt priorities

Each potential interrupt source is assigned a priority level, which means that if more than one interrupt is pending at the same time, the processor will service the one with the highest priority first. For example, if both an external interrupt and a timer interrupt are pending after an instruction execution, the external interrupt is serviced first.

Table 10-2 shows the relative priority of all the possible interrupt sources. Figure 10-4 shows the interrupt processing flow.

Table 10-2 Interrupt priorities

Source	Register	Flags	Vector address	Priority
Reset	—	—	$3FFE, $3FFF	highest
Software interrupt (SWI)	—	—	$3FFC, $3FFD	
External interrupt ($\overline{IRQ}$) or WOI	—	—	$3FFA, $3FFB	
Timer input captures	TSR	ICF1, ICF2	$3FF8, $3FF9	
Timer output compares	TSR	OCF1, OCF2	$3FF6, $3FF7	
Timer overflow	TSR	TOF	$3FF4, $3FF5	
Serial communications interface (SCI)	SCSR	TDRE, TC, OR, RDRF, IDLE	$3FF2, $3FF3	
MCAN	CINT	WIF,OIF,EIF, TIF, RIF	$3FF0, $3FF1	lowest

10.2.2 Nonmaskable software interrupt (SWI)

The software interrupt (SWI) is an executable instruction and a nonmaskable interrupt: it is executed regardless of the state of the I-bit in the CCR. If the I-bit is zero (interrupts enabled), SWI is executed after interrupts that were pending when the SWI was fetched, but before interrupts generated after the SWI was fetched. The SWI interrupt service routine address is specified by the contents of memory locations $3FFC and $3FFD.

10.2.3 Maskable hardware interrupts

If the interrupt mask bit in the CCR is set, all maskable interrupts (internal and external) are masked. Clearing the I-bit allows interrupt processing to occur.

Note: The internal interrupt latch is cleared in the first part of the interrupt service routine; therefore, one external interrupt pulse could be latched and serviced as soon as the I-bit is cleared.

Note: If the external interrupt function is disabled by the INTE bit and an external interrupt is sensed by the edge detector circuitry, then the interrupt request is latched and the interrupt stays pending until the INTE bit is set. The internal latch of the external interrupt is cleared in the first part of the service routine (except for the low level interrupt which is not latched); therefore, only one external interrupt pulse can be latched during t_{ILIL} and serviced as soon as the I-bit is cleared.

10.2.3.2 External interrupts

$\overline{\text{IRQ}}$ interrupt

If the interrupt mask in the condition code register has been cleared and the interrupt enable bit (INTE) is set and the signal on the external interrupt pin ($\overline{\text{IRQ}}$) satisfies the condition selected by the option control bits (INTP and INTN), then the external interrupt is recognized. INTE, INTP and INTN are all bits contained in the miscellaneous register at $000C. When the interrupt is recognized, the current state of the CPU is pushed onto the stack and the I-bit is set. This masks further interrupts until the present one is serviced. The external interrupt service routine address is specified by the content of memory locations $3FFA and $3FFB.

Wired-OR interrupt (WOI)

An external WOI capability is provided on all port B I/O pins when they are programmed as inputs, and on the NWOI pin. A WOI is activated only if WOIE in the EEPROM control register is set and if wired-OR interrupts have been chosen as an option on the device (see Section 1.2). If wired-OR interrupts are enabled on a given input pin (NWOI pin or port B pins; refer to Section 2.3.19 and Section 4.2), an external interrupt is requested when this pin is pulled high. The request is serviced by the interrupt routine whose start address is contained in memory locations $3FFA and $3FFB. External and power-on reset clear the WOIE bit. A WOI interrupt will cause the MCU to exit STOP mode.

The interrupt enable bit (INTE) in the miscellaneous register enables both wired-OR interrupts and the $\overline{\text{IRQ}}$ interrupt. $\overline{\text{IRQ}}$ and WOI are internally OR-ed before interrupt sensitivity selection (see Section 10.2.3.1).

10.2.3.3 MCAN interrupt (CIRQ)

Several sources can trigger a CIRQ. The MCAN interrupt register at $0023 is used to identify the source. Each CIRQ source can be individually enabled (except the wake-up interrupt, which is always enabled) by different bits of the MCAN control register at $0020.

The CIRQ sources are (also see Section 5.3.4):

Receive IRQ: this signals successful reception of a complete message.

Transmit IRQ: this signals successful transmission of a complete message.

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12.4 Control timing

Table 12-4 Control timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Oscillator frequency	f_{OSC}	0	22	MHz
MCAN module clock frequency	f_{CAN}	0	11	MHz
MCU bus frequency	f_{MCU}	0	2.2	MHz
Cycle time (see Figure 10-1)	t_{CYC}	455	—	ns
Crystal oscillator start-up time (see Figure 10-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width (mask option)				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time	t_{ERA}	10	10	ms
EEPROM byte program time(1)	t_{PROG}	10	10	ms
Timer (see Figure 12-1)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns
Write/erase endurance(5)(6)	—	10000		cycles
Data retention(5)(6)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

(5) At a temperature of 85°C.

(6) Refer to Reliability Monitor Report (currrent quarterly issue) for current failure rate information.

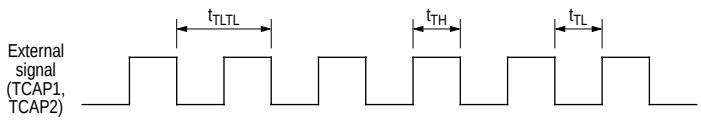

Figure 12-1 Timer relationship

A.3.3 A/D converter characteristics

Table A-4 A/D characteristics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°**C** to +125°**C**)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics (V_{RH} = V_{DD} and V_{RL} = 0V)	—	± 0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	± 0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	± 1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
ΔV_R(1)	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when V_{IN} = V_{RL}	00	—	Hex
Full scale reading	Conversion result when V_{IN} = V_{RH}	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(2)	 — —	 12 12	 t_{CYC} µs
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(3)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Performance verified down to 2.5V ΔVR, but accuracy is tested and guaranteed at ΔVR = 5V±10%.

(2) Source impedances greater than 10kΩ will adversely affect internal charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 9-2).

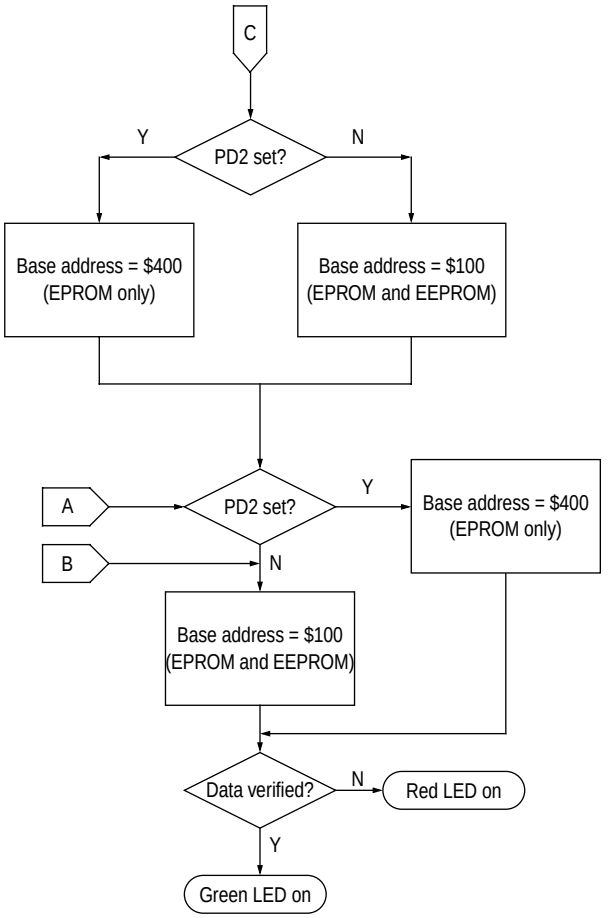

Figure B-3 Modes of operation flow chart (Continued)

B.9.5 A/D converter characteristics

Table B-11 A/D characteristics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics (V_{RH} = V_{DD} and V_{RL} = 0V)	—	± 0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	± 0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	± 1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
ΔV_R(1)	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when V_{IN} = V_{RL}	00	—	Hex
Full scale reading	Conversion result when V_{IN} = V_{RH}	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(2)	 — —	 12 12	 t_{CYC} µs
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(3)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Performance verified down to 2.5V ΔVR, but accuracy is tested and guaranteed at ΔVR = 5V±10%.

(2) Source impedances greater than 10kΩ will adversely affect internal charging time during input sampling.

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