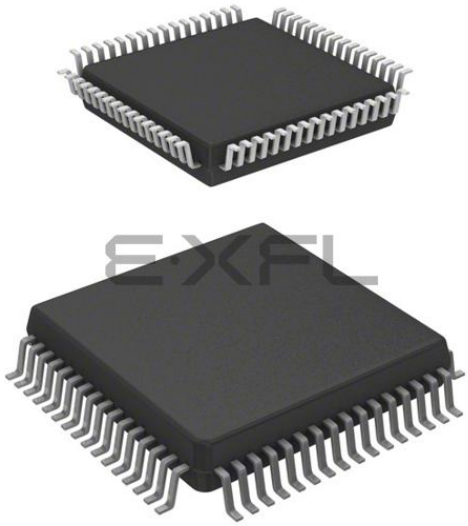

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	CANbus, SCI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	528 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705x32mfue4

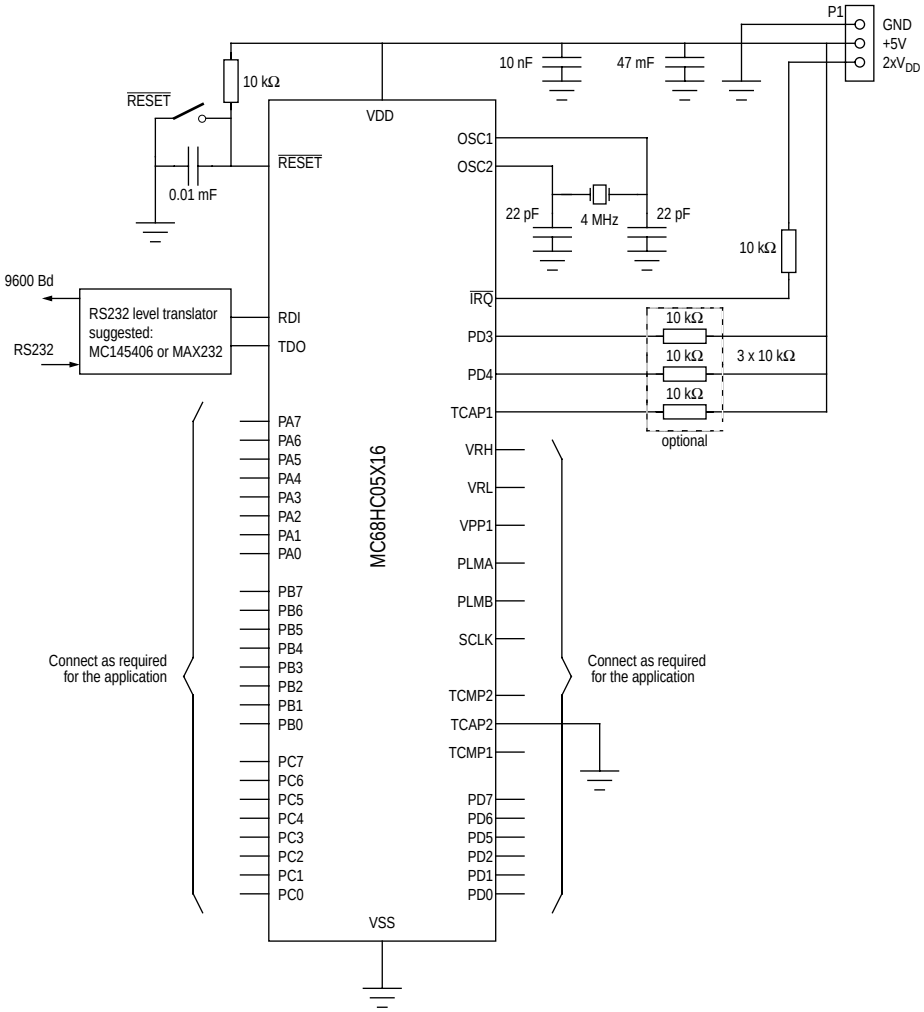
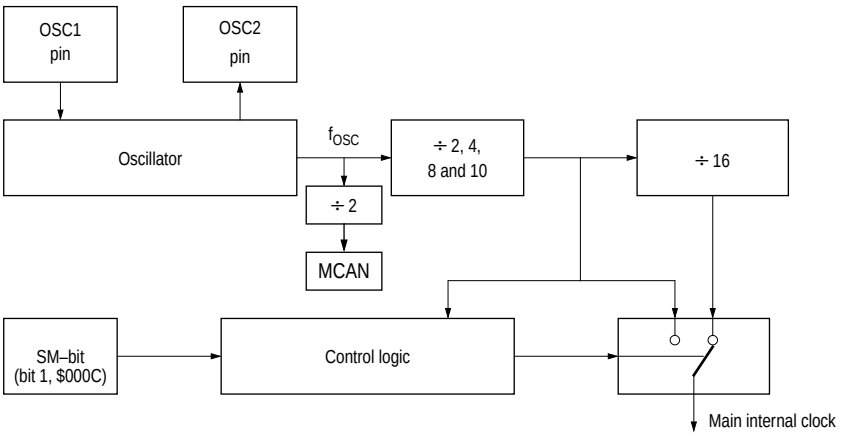


Figure 2-3 MC68HC05X16 'load program in RAM and execute' schematic diagram



Note: The MCAN module clock is unaffected during SLOW mode.

Figure 2-5 Slow mode divider block diagram

2.2.3.1 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG	u001 000u

SM — Slow mode

1 (set) – The system runs at a bus speed 16 times lower than normal (f_{OSC}/32, /64, /128 or /160). SLOW mode affects all sections of the device (including SCI, A/D and timer) except for the MCAN module.

0 (clear) – The system runs at normal bus speed (f_{OSC}/2, /4, /8 or /10).

The SM bit is cleared by external or power-on reset. The SM bit is automatically cleared when entering STOP mode.

Note: The bits shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

2.3.21 VDD1

This pin is the power input for the input comparator of the MCAN module.

2.3.22 VSS1

This pin is the ground connection for the input comparator of the MCAN bus.

2.3.23 VDDH

This pin provides the high voltage reference output for the MCAN bus. The output voltage is equal to VDD÷2.

2.3.24 RX0/RX1

These input pins connect the physical bus lines to the input comparator (receive). When the MCAN is in SLEEP mode, a dominant level on these pins will wake it up.

2.3.25 TX0/TX1

These output pins connect the output drivers of the MCAN bus to the physical bus lines (transmit).

MCAN bus lines. The bus can have one of two complementary values: dominant or recessive. During simultaneous transmission of dominant and recessive bits the resulting bus value will be dominant. For example with a positive logic wired-AND implementation of the bus, the dominant level would correspond to a logic 0 and the recessive level to a logic 1.

3.5 EEPROM

The user EEPROM consists of 256 bytes of memory located from address $0100 to $01FF. 255 bytes are general purpose and 1 byte is used by the option register. The non-volatile EEPROM is byte erasable.

An internal charge pump provides the EEPROM voltage (V_{PP1}), which removes the need to supply a high voltage for erase and programming functions. The charge pump is a capacitor/diode ladder network which will give a very high impedance output of around 20-30 MΩ. The voltage of the charge pump is visible at the VPP1 pin. During normal operation of the device, where programming/erasing of the EEPROM array will occur, VPP1 should never be connected to either VDD or VSS as this could prevent the charge pump reaching the necessary programming voltage. Where it is considered dangerous to leave VPP1 unconnected for reasons of excessive noise in a system, it may be tied to V_{DD}; this will protect the EEPROM data but will also increase power consumption, and therefore it is recommended that the protect bit function is used for regular protection of EEPROM data (see Section 3.5.5).

In order to achieve a higher degree of security for stored data, there is no capability for bulk or row erase operations.

The EEPROM control register ($0007) provides control of the EEPROM programming and erase operations.

Warning: The VPP1 pin should never be connected to VSS, as this could cause permanent damage to the device.

3.5.1 EEPROM control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM/ECLK control	$0007	WOIE	CAF	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

WOIE — Wired-OR interrupt enable

This bit is used to enable wired-OR interrupts on the NWOI pin and on all port B pins which have been programmed as inputs. Wired-OR interrupts can only be enabled if the WOI mask option is selected (see Section 1.2). WOIE is forced to zero if this mask option is not selected. Power-on reset clears the WOIE bit.

1 (set) – Wired-OR interrupts are enabled (provided that wired-OR interrupts have been selected as a mask option).

0 (clear) – Wired-OR interrupts are disabled.

EE1P – EEPROM protect bit

In order to achieve a higher degree of protection, the EEPROM is effectively split into two parts, both working from the VPP1 charge pump. Part 1 of the EEPROM array (32 bytes from $0100 to $011F) cannot be protected; part 2 (224 bytes from $0120 to $01FF) is protected by the EE1P bit of the options register.

1 (set) – Part 2 of the EEPROM array is not protected; all 256 bytes of EEPROM can be accessed for any read, erase or programming operations

0 (clear) – Part 2 of the EEPROM array is protected; any attempt to erase or program a location will be unsuccessful

When this bit is set (erased), the protection will remain until the next power-on or external reset. EE1P can only be written to ‘0’ when the ELAT bit in the EEPROM control register is set.

SEC – Security bit

This high security bit allows the user to secure the EEPROM data from external accesses. When the SEC bit is at ‘0’, the EEPROM contents are secured by preventing any entry to test mode. The only way to erase the SEC bit to ‘1’ externally is to enter bootstrap mode, at which time the entire EEPROM contents will be erased. When the SEC bit is changed, its new value will have no effect until the next external or power-on reset.

3.6 EEPROM during STOP mode

When entering STOP mode, the EEPROM is automatically set to the read mode and the VPP1 high voltage charge pump generator is automatically disabled.

3.7 EEPROM during WAIT mode

The EEPROM is not affected by WAIT mode. Any program/erase operation will continue as in normal operating mode. The charge pump is not affected by WAIT mode, therefore it is possible to wait the t_{ERA1} erase time or t_{PROG1} programming time in WAIT mode.

Under normal operating conditions, the charge pump generator is driven by the internal CPU clocks. When the operating frequency is low, e.g. during slow mode (see Figure 3.8) or during WAIT mode, the clocking should be done by the internal A/D RC oscillator. The RC oscillator is enabled by setting the ADRC bit of the A/D status/control register at $0009.

RX0 — Receive pin 0 (passive) (Refer to Figure 5-6)

1 (set) – VDD/2 will be connected to the input comparator. The RX0 pin is disconnected.

0 (clear) – The RX0 pin will be connected to the input comparator. VDD/2 is disconnected.

RX1 — Receive pin 1 (passive) (Refer to Figure 5-6)

1 (set) – VDD/2 will be connected to the input comparator. The RX1 pin is disconnected.

0 (clear) – The RX1 pin will be connected to the input comparator. VDD/2 is disconnected.

Note: If both RX0 and RX1 are set, or both are clear, then neither of the RX pins will be disconnected.

COMPSEL — Comparator selector

1 (set) – RX0 and RX1 will be compared with VDD/2 during sleep mode (see Figure 5-6).

0 (clear) – RX0 will be compared with RX1 during sleep mode.

SLEEP — Go to sleep

1 (set) – Sleep – The MCAN will go into sleep mode, as long as there are no interrupts pending and there is no activity on the bus. Otherwise the MCAN will issue a wake-up interrupt.

0 (clear) – Wake-up – The MCAN will function normally. If SLEEP is cleared by the CPU then the MCAN will waken up, but will not issue a wake-up interrupt.

Note: If SLEEP is set during the reception or transmission of a message, the MCAN will generate an immediate wake-up interrupt. (This allows for a more orthogonal software implementation on the CPU.) This will have no effect on the transfer layer, i.e. no message will be lost or corrupted.

The CAF flag in the EEPROM control register indicates whether or not sleep mode was entered successfully.

A node that was sleeping and has been awakened by bus activity will not be able to receive any messages until its oscillator has started and it has found a valid end of

TCS — Transmission complete status

This bit is cleared by the MCAN when TR becomes set. When TCS is set it indicates that the last requested transmission was successfully completed. If, after TCS is cleared, but before transmission begins, an abort transmission command is issued then the transmit buffer will be released and TCS will remain clear. TCS will then only be set after a further transmission is both requested and successfully completed.

1 (set) – Complete – Last requested transmission successfully completed.

0 (clear) – Incomplete – Last requested transmission not complete.

TBA — Transmit buffer access

When clear, the transmit buffer is locked and cannot be accessed by the CPU. This indicates that either a message is being transmitted, or is awaiting transmission. If the CPU writes to the transmit buffer while it is locked, then the bytes will be lost without this being signalled.

1 (set) – Released – The transmit buffer may be written to by the CPU.

0 (clear) – Locked – The CPU cannot access the transmit buffer.

DO — Data overrun

This bit is set when both receive buffers are full and there is a further message to be stored. In this case the new message is dropped, but the internal logic maintains the correct protocol. The MCAN does not receive the message, but no warning is sent to the transmitting node. The MCAN clears DO when the CPU sets the COS bit in the CCOM register.

Note that data overrun can also be caused by a transmission, since the MCAN will temporarily store an outgoing frame in a receive buffer in case arbitration is lost during transmission.

1 (set) – Overrun – Both receive buffers were full and there was another message to be stored.

0 (clear) – Normal operation.

RBS — Receive buffer status

This bit is set by the MCAN when a new message is available. When clear this indicates that no message has become available since the last RRB command. The bit is cleared when RRB is set. However, if the second receive buffer already contains a message, then control of that buffer is given to the CPU and RBS is immediately set again. The first receive buffer is then available for the next incoming message from the MCAN.

1 (set) – Full – A new message is available for the CPU to read.

0 (clear) – Empty – No new message is available.

RIF — Receive interrupt flag

The RIF bit is set by the MCAN when a new message is available in the receive buffer, and the RIE bit in CCNTRL is set. At the same time RBS is set. Like all the bits in this register, RIF is cleared by reading the register, or when reset request is set.

1 (set) – A new message is available in the receive buffer.

0 (clear) – No receive interrupt has occurred.

5.3.5 MCAN acceptance code register (CACC)

On reception each message is written into the current receive buffer. The MCU is only signalled to read the message however, if it passes the criteria in the acceptance code and acceptance mask registers (accepted); otherwise, the message will be overwritten by the next message (dropped).

Note: This register can only be accessed when the reset request bit in the CCNTRL register is set.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
MCAN acceptance code (CACC)	$0024	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Undefined

AC7 – AC0 — Acceptance code bits

AC7 – AC0 comprise a user defined sequence of bits with which the 8 most significant bits of the data identifier (ID10 – ID3) are compared. The result of this comparison is then masked with the acceptance mask register. Once a message has passed the acceptance criterion the respective identifier, data length code and data are sequentially stored in a receive buffer, providing there is one free. If there is no free buffer, the data overrun condition will be signalled.

On acceptance the receive buffer status bit is set to full and the receive interrupt bit is set (provided RIE = enabled).

FOLV2 — Force output compare 2

This bit always reads as zero, hence writing a zero to this bit has no effect. Writing a one at this position will force the OLV2 bit to the corresponding output level latch, thus appearing at the TCMP2 pin. Note that this bit does not affect the OCF2 bit of the status register (see Section 6.4.3).

1 (set) – OLV2 bit forced to output level latch.

0 (clear) – No effect.

FOLV1 — Force output compare 1

This bit always reads as zero, hence writing a zero to this bit has no effect. Writing a one at this position will force the OLV1 bit to the corresponding output level latch, thus appearing at the TCMP1 pin. Note that this bit does not affect the OCF1 bit of the status register (see Section 6.4.3).

1 (set) – OLV1 bit forced to output level latch.

0 (clear) – No effect.

OLV2 — Output level 2

When OLV2 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP2 pin. When clear, it will be a low level which will appear on the TCMP2 pin.

1 (set) – A high output level will appear on the TCMP2 pin.

0 (clear) – A low output level will appear on the TCMP2 pin.

IEDG1 — Input edge 1

When IEDG1 is set, a positive-going edge on the TCAP1 pin will trigger a transfer of the free-running counter value to the input capture register 1. When clear, a negative-going edge triggers the transfer.

1 (set) – TCAP1 is positive-going edge sensitive.

0 (clear) – TCAP1 is negative-going edge sensitive.

Note: There is no need for an equivalent bit for the input capture register 2 as TCAP2 is negative-going edge sensitive only.

OLV1 — Output level 1

When OLV1 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP1 pin. When clear, it will be a low level which will appear on the TCMP1 pin.

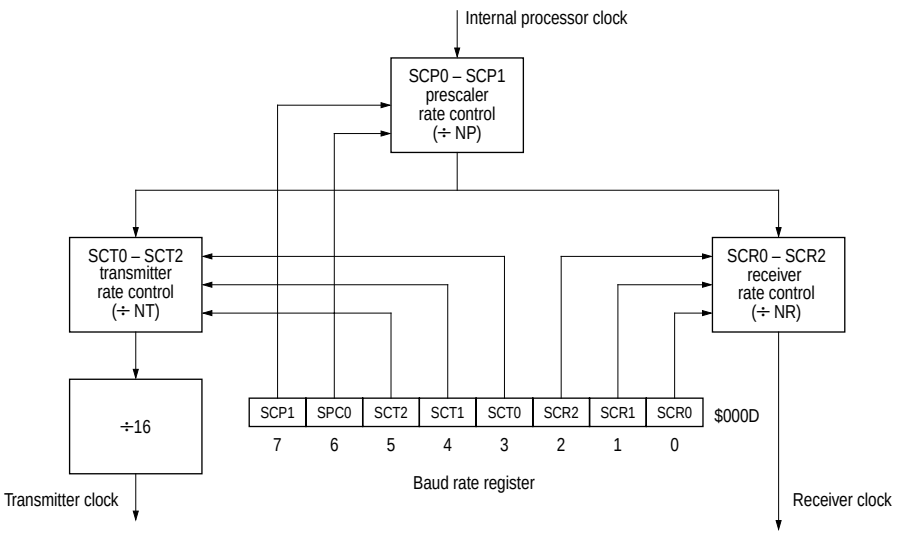
1 (set) – A high output level will appear on the TCMP1 pin.

0 (clear) – A low output level will appear on the TCMP1 pin.

When SCDR is read, it contains the last data byte received, provided that the receiver is enabled. The receive data register full flag bit (RDRF) in the SCSR is set to indicate that a data byte has been transferred from the input serial shift register to the SCDR; this will cause an interrupt if the receiver interrupt is enabled. The data transfer from the input serial shift register to the SCDR is synchronized by the receiver bit rate clock. The OR (overrun), NF (noise), or FE (framing) error flags in the SCSR may be set if data reception errors occurred.

An idle line interrupt is generated if the idle line interrupt is enabled and the IDLE bit (which detects idle line transmission) in SCSR is set. This allows a receiver that is not in the wake-up mode to detect the end of a message or the preamble of a new message, or to resynchronize with the transmitter. A valid character must be received before the idle line condition or the IDLE bit will not be set and idle line interrupt will not be generated.

The SCP0 and SCP1 bits function as a prescaler for SCR0–SCR2 to generate the receiver baud rate and for SCT0–SCT2 to generate the transmitter baud rate. Together, these eight bits provide multiple transmitter/receiver rate combinations for a given crystal frequency (see Figure 7-2). This register should only be written to while both the transmitter and receiver are disabled (TE=0, RE=0).



Note: There is a fixed rate divide-by-16 before the transmitter to compensate for the inherent divide-by-16 of the receiver (sampling). This means that by loading the same value for both the transmitter and receiver baud rate selector, the same baud rates can be obtained.

Figure 7-2 SCI rate generator division

7.5 Data format

Receive data or transmit data is the serial data that is transferred to the internal data bus from the receive data input pin (RDI) or from the internal bus to the transmit data output pin (TDO). The non-return-to-zero (NRZ) data format shown in Figure 7-3 is used and must meet the following criteria:

- The idle line is brought to a logic one state prior to transmission/reception of a character.
- A start bit (logic zero) is used to indicate the start of a frame.
- The data is transmitted and received least significant bit first.
- A stop bit (logic one) is used to indicate the end of a frame. A frame consists of a start bit, a character of eight or nine data bits, and a stop bit.
- A break is defined as the transmission or reception of a low (logic zero) for at least one complete frame time (10 zeros for 8-bit format, 11 zeros for 9-bit).

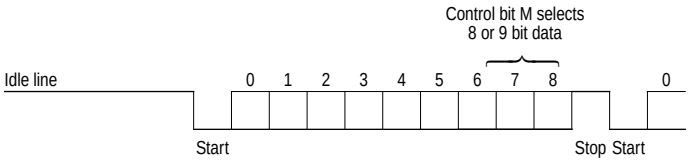


Figure 7-3 Data format

7.6 Receiver wake-up operation

The receiver logic hardware also supports a receiver wake-up function which is intended for systems having more than one receiver. With this function a transmitting device directs messages to an individual receiver or group of receivers by passing addressing information as the initial byte(s) of each message. The wake-up function allows receivers not addressed to remain in a dormant state for the remainder of the unwanted message. This eliminates any further software overhead to service the remaining characters of the unwanted message and thus improves system performance.

The receiver is placed in wake-up mode by setting the receiver wake-up bit (RWU) in the SCCR2 register. While RWU is set, all of the receiver related status flags (RDRF, IDLE, OR, NF, and FE) are inhibited (cannot become set). Note that the idle line detect function is inhibited while the RWU bit is set. Although RWU may be cleared by a software write to SCCR2, it would be unusual to do so. Normally RWU is set by software and is cleared automatically in hardware by one of the two methods described below.

7.10 SCI synchronous transmission

The SCI transmitter allows the user to control a one way synchronous serial transmission. The SCLK pin is the clock output of the SCI transmitter. No clocks are sent to that pin during start bit and stop bit. Depending on the state of the LBCL bit (bit 0 of SCCR1), clocks will or will not be activated during the last valid data bit (address mark). The CPOL bit (bit 2 of SCCR1) allows the user to select the clock polarity, and the CPHA bit (bit 1 of SCCR1) allows the user to select the phase of the external clock (see Figure 7-8, Figure 7-9 and Figure 7-10).

During idle, preamble and send break, the external SCLK clock is not activated.

These options allow the user to serially control peripherals which consist of shift registers, without losing any functions of the SCI transmitter which can still talk to other SCI receivers. These options do not affect the SCI receiver which is independent of the transmitter.

The SCLK pin works in conjunction with the TDO pin. When the SCI transmitter is disabled (TE = 0), the SCLK and TDO pins go to the high impedance state.

Note: The LBCL, CPOL and CPHA bits have to be selected before enabling the transmitter to ensure that the clocks function correctly. These bits should not be changed while the transmitter is enabled.

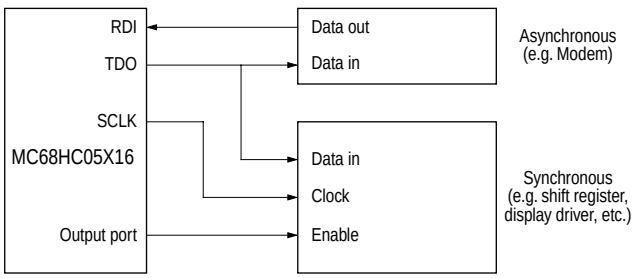


Figure 7-8 SCI example of synchronous and asynchronous transmission

8.2 PLM clock selection

The slow/fast mode of the PLM D/A converters is selected by bits 1, 2, and 3 of the miscellaneous register at address $000C (SFA bit for PLMA and SFB bit for PLMB). The slow/fast mode has no effect on the D/A converters' 8-bit resolution (see Figure 8-3).

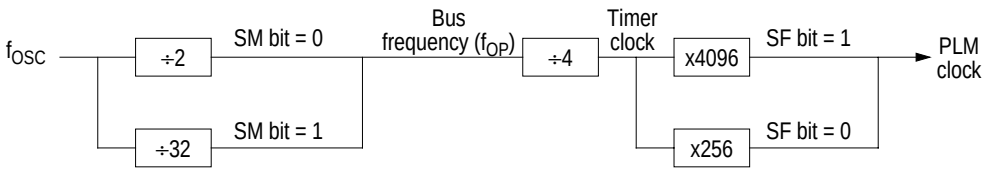


Figure 8-3 PLM clock selection

8.3 PLM during STOP mode

On entering STOP mode, the PLM outputs remain at their particular level. When STOP mode is exited by an interrupt, the PLM systems resume regular operation. If STOP mode is exited by power-on or external reset the registers values are forced to $00.

8.4 PLM during WAIT mode

The PLM system is not affected by WAIT mode and continues normal operation.

11.3 Addressing modes

Ten different addressing modes provide programmers with the flexibility to optimize their code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the longest instructions (three bytes) enable access to tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One or two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory locations.

The term 'effective address' (EA) is used in describing the various addressing modes. The effective address is defined as the address from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate 'contents of' the location or register referred to. For example, (PC) indicates the contents of the location pointed to by the PC (program counter). An arrow indicates 'is replaced by' and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the ***M6805 HMOS/M146805 CMOS Family Microcomputer/ Microprocessor User's Manual*** or to the ***M68HC05 Applications Guide***.

11.3.1 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as the control instruction, with no other arguments are included in this mode. These instructions are one byte long.

11.3.2 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g. a constant used to initialize a loop counter).

$$EA = PC+1;\ PC \leftarrow PC+2$$

11.3.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

$$EA = (PC+1);\ PC \leftarrow PC+2$$
$$\text{Address bus high} \leftarrow 0;\ \text{Address bus low} \leftarrow (PC+1)$$

A.3.4 Control timing

Table A-5 Control timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°**C** to +125°**C**)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation Oscillator frequency MCAN module clock frequency MCU bus frequency	 f_{OSC} f_{CAN} f_{MCU}	 0 0 0	 22 11 2.2	 MHz MHz MHz
Cycle time (see Figure 10-1)	t_{CYC}	455	—	ns
Crystal oscillator start-up time (see Figure 10-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width (mask option) 4064 cycle 16 cycle	 t_{PORL} t_{PORL}	 4064 16	 — —	 t_{CYC} t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time	t_{ERA}	10	10	ms
EEPROM byte program time(1)	t_{PROG}	10	10	ms
Timer (see Figure A-3) Resolution(2) Input capture pulse width Input capture pulse period	 t_{RESL} t_{TH}, t_{TL} t_{TLTL}	 4 125 —(3)	 — — —	 t_{CYC} ns t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns
Write/erase endurance(5)(6)	—	10000		cycles
Data retention(5)(6)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

(5) At a temperature of 85°C.

(6) Refer to Reliability Monitor Report (currrent quarterly issue) for current failure rate information.

B.9 Electrical specifications

B.9.1 Maximum ratings

Table B-7 Maximum ratings

Rating	Symbol	Value	Unit
Supply voltage(1)	V_{DD}	– 0.5 to +7.0	V
Input voltage	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input voltage – Bootstrap mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.5 to $2V_{DD}$ + 0.5	V
Operating temperature range	T_A	T_L to T_H –40 to +125	°C
Storage temperature range	T_{STG}	– 65 to +150	°C
Current drain per pin(2) (Excluding VDD, VSS, VDD1 and VSS1) – Source – Sink	 I_D I_S	 25 45	 mA mA
External oscillator frequency	f_{OSC}	22	MHz

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

B.9.2 DC electrical characteristics

Table B-8 DC electrical characteristics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, Output high voltage (I_{LOAD} = 1.6mA) TDO, SCLK, PLMA, PLMB Output high voltage (I_{LOAD} = –300µA) OSC2	 V_{OH} V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8 V_{DD} – 0.8	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.3	 — — 	V
Output low voltage (I_{LOAD} = 1.6mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6mA) $\overline{RESET}$ Output low voltage (I_{LOAD} = –100µA) OSC2	 V_{OL} V_{OL} V_{OL}	 — 	 0.1 0.2 0.2	 0.4 0.6 0.4	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI, CANE, MDS, NWOI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI, CANE, MDS, NWOI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Can comparator I_{DD} (I_{DD1})[3][4][5] Supply current in DIV2 mode RUN: CAN active[6] STOP: CAN active WAIT: CAN asleep[7] STOP: CAN asleep	 I_{DD1} I_{DD1} I_{DD1} I_{DD1}	 — — — —	 360 360 32 10	 900 900 100 30	 µA µA µA µA
MCU I_{DD}[3][4][8] Supply current in DIV 2 mode RUN (SM = 0): CAN active RUN (SM = 1): CAN active WAIT (SM = 0): CAN active WAIT (SM =1): CAN active WAIT (SM = 0): CAN asleep WAIT (SM = 1): CAN asleep STOP: CAN active STOP: CAN asleep	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — — — —	 7 2.2 2.4 1.9 1.3 0.7 0.5 90	 11.4 3.9 4.4 3.2 2.7 0.9 1.5 300	 mA mA mA mA mA mA mA µA
MCU I_{DD}[3][5][8] Supply current RUN (SM = 0): CAN active RUN (SM = 1): CAN active WAIT (SM = 0): CAN active WAIT (SM =1): CAN active WAIT (SM = 0): CAN asleep WAIT (SM = 1): CAN asleep STOP: CAN active STOP: CAN asleep	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — — — —	 3.9 1.2 1.4 1.0 1.1 0.6 0.16 90	 7 2.9 3.2 2.6 2 1.75 1.5 300	 mA mA mA mA mA mA mA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	±0.2	±1	µA

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8. How could we improve this document? _____

_____

_____

9. How would you rate Motorola's documentation?

	Excellent			Poor
– In general	❑	❑	❑	❑
– Against other semiconductor suppliers	❑	❑	❑	❑

10. Which semiconductor manufacturer provides the best technical documentation? _____

11. Which company (in any field) provides the best technical documentation? _____

12. How many years have you worked with microprocessors?

Less than 1 year ❑ 1–3 years ❑ 3–5 years ❑ More than 5 years ❑

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13. Currently there is some discussion in the semiconductor industry regarding a move towards providing data sheets in electronic form. If you have any opinion on this subject, please comment. _____

_____

14. We would be grateful if you would supply the following information (at your discretion), or attach your card.

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