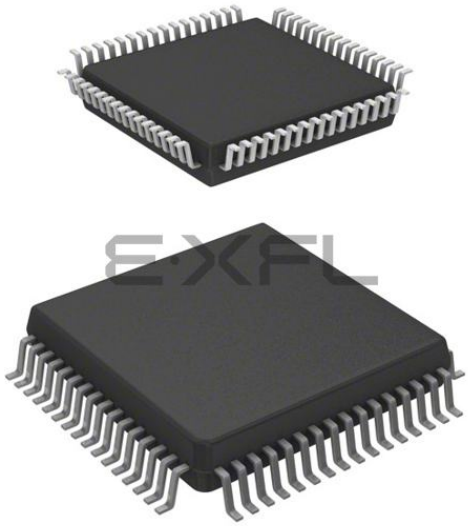

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	CANbus, SCI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	528 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705x32mfue4r

1.1 Features

Hardware features

- Fully static design featuring the industry standard M68HC05 family CPU core
- On chip crystal oscillator with divide-by -2, -4, -8 or -10, or a software selectable divide-by -32, -64, -128 or -160 option (SLOW mode)
- 352 bytes of RAM
- 15102 bytes of user ROM plus 16 bytes of user vectors
- 256 bytes of byte erasable EEPROM with internal charge pump and security bit
- Write/erase protect bit for 224 of the 256 bytes EEPROM
- Bootstrap firmware
- Power saving STOP, WAIT and SLOW modes
- Three 8-bit parallel I/O ports and one 8-bit input-only port; wired-OR interrupt capability on all port B pins
- Motorola controller area network (MCAN) with line interface circuitry
- Software option available to output the internal E-clock to port pin PC2
- 16-bit timer with 2 input captures and 2 output compares
- Computer operating properly (COP) watchdog timer
- Serial communications interface system (SCI) with independent transmitter/receiver baud rate selection; receiver wake-up function for use in multi-receiver systems
- 8 channel A/D converter
- 2 pulse length modulation systems which can be used as D/A converters
- One interrupt request input plus 4 on-board hardware interrupt sources
- 2.2 MHz bus speed
- –40 to +125°C temperature range
- Available in 64-pin quad flat pack (QFP) package
- Complete development system support available using the MMDS05 or M68MMPFB0508 development station with the M68EML05X32 emulation module or the M68HC05XEVS evaluation system

2.2.2 WAIT mode

The WAIT instruction places the MCU in a low power consumption mode, but WAIT mode consumes more power than STOP mode. All CPU action is suspended and the watchdog is disabled, but the timer, A/D and SCI and MCAN systems remain active and operate as normal (see flow chart in Figure 2-4). All other memory and registers remain unaltered and all parallel input/output lines remain unchanged. The programming or erase mechanism of the EEPROM is also unaffected, as well as the charge pump high voltage generator.

During WAIT mode the I-bit in the CCR is cleared to enable all interrupts. The INTE bit in the miscellaneous register (Section 2.2.3.1) is not affected by WAIT mode. When any interrupt or reset is sensed, the program counter vectors to the locations containing the start address of the interrupt or reset service routine.

Any interrupt or reset condition causes the processor to exit WAIT mode.

If an interrupt exit from WAIT mode is performed, the state of the remaining systems will be unchanged.

If a reset exit from WAIT mode is performed the entire system reverts to the disabled reset state.

Note: The stacking corresponding to an eventual interrupt to leave WAIT mode will only be executed when leaving WAIT mode.

3
MEMORY AND REGISTERS

The MC68HC05X16 MCU is capable of addressing 16384 bytes of memory and registers with its program counter. The memory map includes 15118 bytes of user ROM (including user vectors), 576 bytes of bootstrap ROM, 352 bytes of RAM and 256 bytes of EEPROM.

3.1 Registers

All the I/O, control and status registers of the MC68HC05X16 are contained within the first 32-byte block of the memory map, as shown in Figure 3-1. MCAN registers are contained in the next 30 bytes of memory.

The miscellaneous register is shown in Section 3.8 as this register contains bits which are relevant to several modules.

3.2 RAM

The user RAM comprises 176 bytes of memory, from $0050 to $00FF. This is shared with a 64 byte stack area. The stack begins at $00FF and may extend down to $00C0. The user RAM also comprises 176 bytes from $0250 to $02FF which is completely free for the user.

Note: Using the stack area for data storage or temporary work locations requires care to prevent the data from being overwritten due to stacking from an interrupt or subroutine call.

3.3 ROM

The user ROM consists of 15118 bytes of ROM mapped as follows:

- 15102 bytes of user ROM from $0300 to $3DFD
- 16 bytes of user vectors from $3FF0 to $3FFF

5.1 TBF – Transmit buffer

The transmit buffer is an interface between the CPU and the bit stream processor (BSP) and is able to store a complete message. The buffer is written by the CPU and read by the BSP. The CPU may access this buffer whenever transmit buffer access is set to released. On requesting a transmission (by setting transmission request in the MCAN command register to present) transmit buffer access is set to locked, giving the BSP exclusive access to this buffer. The transmit buffer is released after the message transfer has been completed or aborted.

The TBF is 10 bytes long and holds the identifier (1 byte), the control field (1 byte) and the data field (maximum length 8 bytes). The buffer is implemented as a single-ported RAM, with mutually exclusive access by the CPU and the BSP.

5.2 RBF – Receive buffer

The receive buffer is an interface between the BSP and the CPU and stores a message received from the bus line. Once filled by the BSP and allocated to the CPU (by the IML), the receive buffer cannot be used to store subsequent received messages until the CPU has acknowledged the reading of the buffer's contents. Thus, unless the CPU releases a receive buffer within a protocol defined time frame, future messages to be received may be lost.

To reduce the requirements on the CPU, two receive buffers (RBF0 and RBF1) are implemented. While one receive buffer is allocated to the CPU, the BSP may write to the other buffer. RBF0 and RBF1 are each 10 bytes long and hold the identifier (1 byte), the control field (1 byte) and the data field (maximum length 8 bytes). The buffers are implemented as single-ported RAMs with mutually exclusive access from the CPU and the BSP. The BSP signals the MCU to read the receive buffer only when the message being received has an identifier that passes the acceptance filter. Note that a message being transmitted will be automatically written to the receive buffer if the identifier passes the acceptance filter. This is because it cannot be known, until after the first byte has been stored, whether or not the transmitting node will lose arbitration to another node.

5.3 Interface to the MC68HC05X16 CPU

The MCAN handles all the communication transactions flowing across the serial bus. For example, the CPU merely places a message to be transmitted into the transmit buffer and sets the TR bit. The MCAN will begin transmitting the message when it has determined that the bus is idle. In the event of a transmission error, the MCAN will initiate a repeated transmission automatically.

In a similar manner, the CPU module is notified that a message has been received only if it was error free. If any error occurs, the MCAN signals the error within the CAN protocol without CPU intervention.

The MCAN within the MC68HC05X16 is controlled using a block of 30 registers. This comprises 10 control registers, 10 Transmit buffer registers and 10 receive buffer registers. These registers are memory mapped between $20 and $3D (see Figure 5-3).

Note: There is an offset of $20 between the MC68HC05X16 addresses and the MCAN internal addresses, i.e. MCAN addresses $00 to $1D, as defined in the BOSCH CAN specification, are mapped to MC68HC05X16 addresses $20 to $3D.

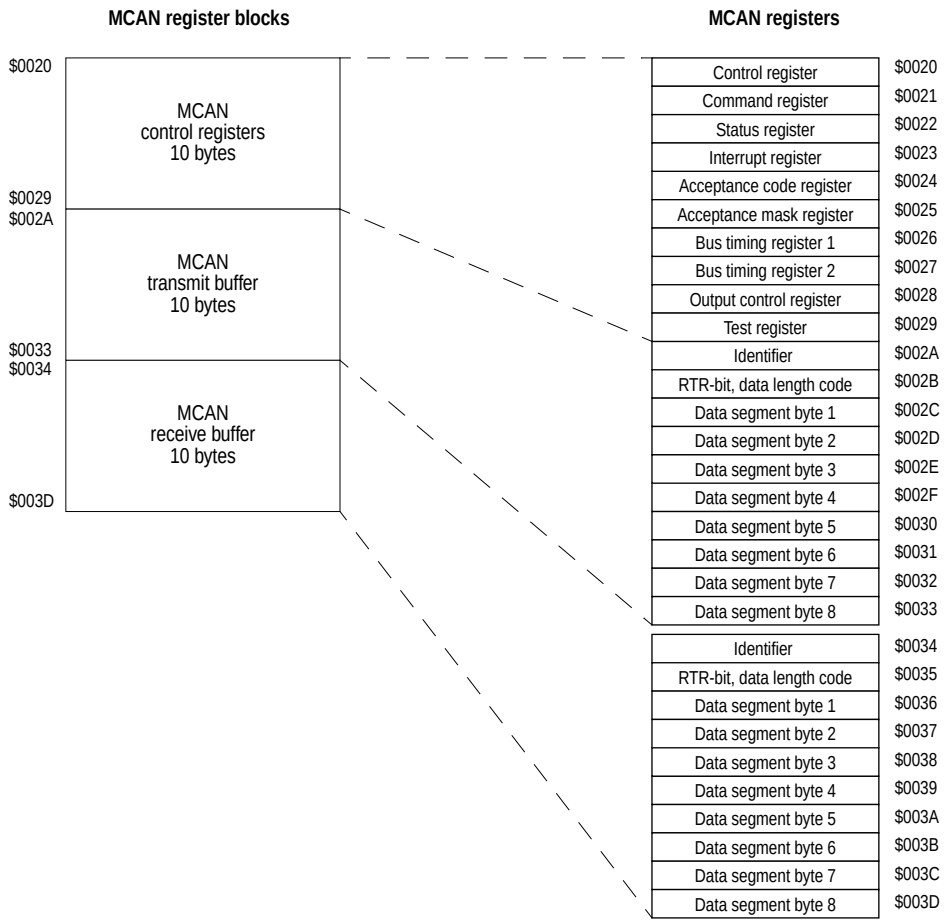

Figure 5-3 MCAN module memory map

6.4 Output compare

'Output compare' is a technique which may be used, for example, to generate an output waveform, or to signal when a specific time period has elapsed, by presetting the output compare register to the appropriate value.

There are two output compare registers: output compare register 1 (OCR1) and output compare register 2 (OCR2).

Note: The same output compare interrupt enable bit (OCIE) is used for the two output compares.

6.4.1 Output compare register 1 (OCR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined

The 16-bit output compare register 1 is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The contents of the output compare register 1 are compared with the contents of the free-running counter continually and, if a match is found, the corresponding output compare flag (OCF1) in the timer status register is set and the output level (OLVL1) is transferred to pin TCMP1. The output compare register 1 values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OCIE) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the output compare register 1 containing the MSB ($16), the output compare function is inhibited until the LSB ($17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare 1 function. The processor can write to either byte of the output compare register 1 without affecting the other byte. The output level (OLVL1) bit is clocked to the output level register and hence to the TCMP1 pin whether the output compare flag 1 (OCF1) is set or clear. The minimum time required to update the output compare register 1 is a function of the program rather than the internal hardware. Because the output compare flag 1 and the output compare register 1 are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

- Write to output compare high 1 to inhibit further compares;
- Read the timer status register to clear OCF1 (if set);
- Write to output compare low 1 to enable the output compare 1 function.

6.6 Timer during STOP mode

When the MCU enters STOP mode, the timer counter stops counting and remains at that particular count value until STOP mode is exited by an interrupt. If STOP mode is exited by power-on or external reset, the counter is forced to $FFFC but if it is exited by external interrupt ($\overline{IRQ}$) then the counter resumes from its stopped value.

Another feature of the programmable timer is that if at least one valid input capture edge occurs at one of the TCAP pins while in STOP mode, the corresponding input capture detect circuitry is armed. This action does not wake the MCU or set any timer flags, but when the MCU does wake-up there will be an active input capture flag (and data) from that first valid edge which occurred during STOP mode.

If STOP mode is exited by an external reset then no such input capture flag or data action takes place even if there was a valid input capture edge (at one of the TCAP pins) during STOP mode.

6.7 Timer during WAIT mode

The timer system is not affected by WAIT mode and continues normal operation. Any valid timer interrupt will wake-up the system.

6.8 Timer state diagrams

The relationships between the internal clock signals, the counter contents and the status of the flag bits are shown in the following figures. It should be noted that the signals labelled ‘internal’ (processor clock, timer clocks and reset) are not available to the user.

Note: Since the PLM system uses the timer counter, PLM results will be affected while resetting the timer counter. Both D/A registers are reset to $00 during power-on or external reset. WAIT mode does not affect the output waveform of the D/A converters.

8.1 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG	u001 000u

SFA — Slow or fast mode selection for PLMA

This bit allows the user to select the slow or fast mode of the PLMA pulse length modulation output.

1 (set) – Slow mode PLMA (4096 x timer clock period).

0 (clear) – Fast mode PLMA (256 x timer clock period).

SFB — Slow or fast mode selection for PLMB

This bit allows the user to select the slow or fast mode of the PLMB pulse length modulation output.

1 (set) – Slow mode PLMB (4096 x timer clock period).

0 (clear) – Fast mode PLMB (256 x timer clock period).

The highest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 256. The lowest speed of the PLM system corresponds to the frequency of the TOF bit being set, multiplied by 16. Because the SFA bit and SFB bit are not double buffered, it is mandatory to set them to the desired values before writing to the PLM registers; not doing so could temporarily give incorrect values at the PLM outputs.

SM — Slow mode

1 (set) – The system runs at a bus speed 16 times lower than normal (f_{OSC}/32). SLOW mode affects all sections of the device, including SCI, A/D and timer.

0 (clear) – The system runs at normal bus speed (f_{OSC}/2).

The SM bit is cleared by external or power-on reset. The SM bit is automatically cleared when entering STOP mode.

Note: The bits that are shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

The A/D reference input (AN0–AN7) is applied to a precision internal D/A converter. Control logic drives this D/A converter and the analog output is successively compared with the analog input sampled at the beginning of the conversion. The conversion is monotonic with no missing codes.

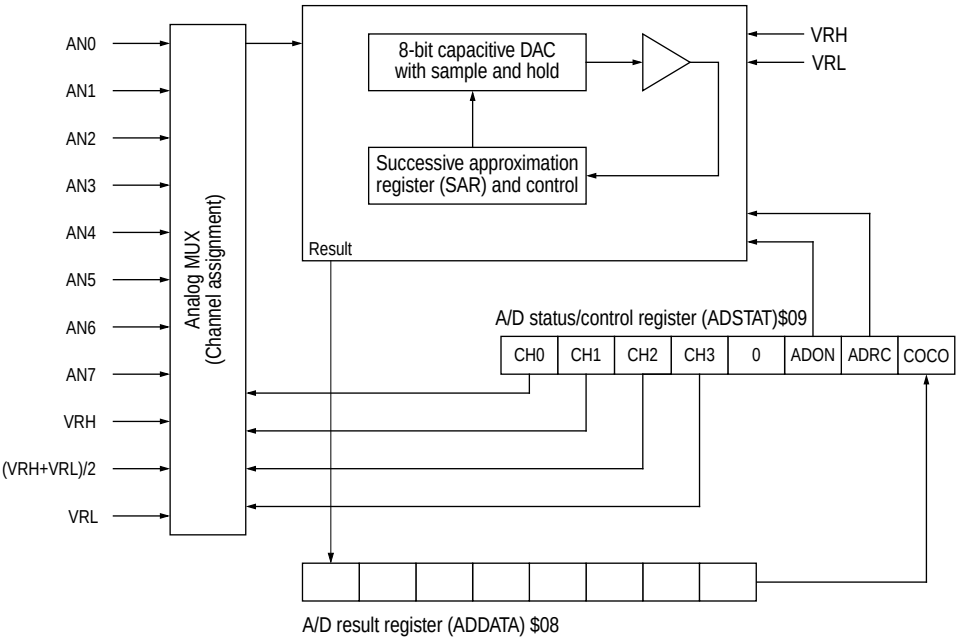

Figure 9-1 A/D converter block diagram

The result of each successive comparison is stored in the SAR and, when the conversion is complete, the contents of the SAR are transferred to the read-only result data register ($08), and the conversion complete flag, COCO, is set in the A/D status/control register ($09).

Warning: Any write to the A/D status/control register will abort the current conversion, reset the conversion complete flag and start a new conversion on the selected channel.

At power-on or external reset, both the ADRC and ADON bits are cleared; thus the A/D is disabled.

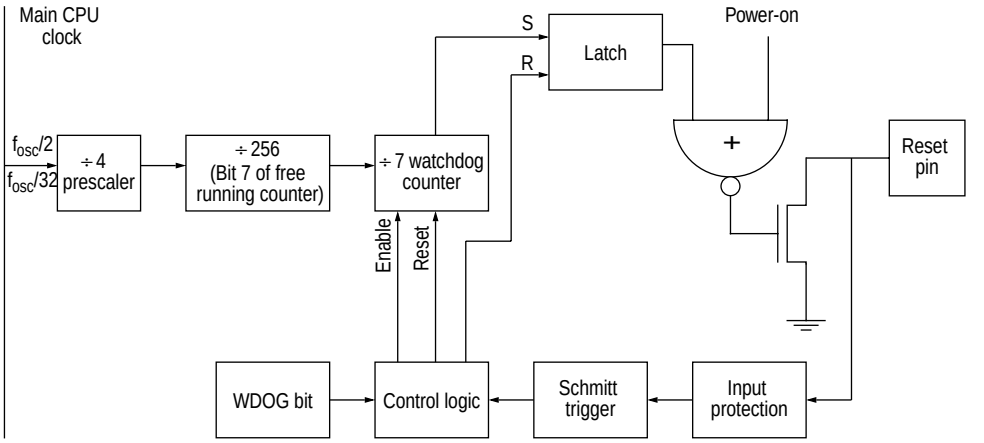

Figure 10-3 Watchdog system block diagram

The watchdog system can be automatically enabled, following power-on or external reset, via a mask option (see Section 1.2), or it can be enabled by software by writing a '1' to the WDOG bit in the miscellaneous register at $000C (see Section 10.1.2). Once enabled, the watchdog system cannot be disabled by software (writing a 'zero' to the WDOG bit has no effect at any time). In addition, the WDOG bit acts as a reset mechanism for the watchdog counter. Writing a '1' to this bit clears the counter to its initial value and prevents a watchdog timeout.

WDOG — Watchdog enable/disable

The WDOG bit can be used to enable the watchdog timer previously disabled by a mask option. Following a watchdog reset the state of the WDOG bit is as defined by the mask option specified.

1 (set) – Watchdog enabled and counter cleared.

0 (clear) – The watchdog cannot be disabled by software; writing a zero to this bit has no effect.

The divide-by-7 watchdog counter will generate a main reset of the chip when it reaches its final state; seven clocks are necessary to bring the watchdog counter from its clear state to its final state. This reset appears after time t_{DOG} since the last clear or since the enable of the watchdog counter system. The watchdog counter, therefore, has to be cleared periodically, by software, with a period less than t_{DOG}.

The reset generated by the watchdog system is apparent at the $\overline{\text{RESET}}$ pin (see Figure 10-3). The $\overline{\text{RESET}}$ pin level is re-entered in the control logic, and when it has been maintained at level 'zero' for a minimum of t_{DOGL}, the $\overline{\text{RESET}}$ pin is released.

Table 11-7 Instruction set (Continued)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
COM											•	•	◊	◊	1
CPX											•	•	◊	◊	◊
DEC											•	•	◊	◊	•
EOR											•	•	◊	◊	•
INC											•	•	◊	◊	•
JMP											•	•	•	•	•
JSR											•	•	•	•	•
LDA											•	•	◊	◊	•
LDX											•	•	◊	◊	•
LSL											•	•	◊	◊	◊
LSR											•	•	0	◊	◊
MUL											0	•	•	•	0
NEG											•	•	◊	◊	◊
NOP											•	•	•	•	•
ORA											•	•	◊	◊	•
ROL											•	•	◊	◊	◊
ROR											•	•	◊	◊	◊
RSP											•	•	•	•	•
RTI											?	?	?	?	?
RTS											•	•	•	•	•
SBC											•	•	◊	◊	◊
SEC											•	•	•	•	1
SEI											•	1	•	•	•
STA											•	•	◊	◊	•
STOP											•	0	•	•	•
STX											•	•	◊	◊	•
SUB											•	•	◊	◊	◊
SWI											•	1	•	•	•
TAX											•	•	•	•	•
TST											•	•	◊	◊	•
TXA											•	•	•	•	•
WAIT											•	0	•	•	•

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset

Not implemented

Condition code symbols

H	Half carry (from bit 3)	◊	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table A-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	WOIE	CAF	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	u001 000u
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1 = watchdog enabled, 0 = watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

A.3.4 Control timing

Table A-5 Control timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°**C** to +125°**C**)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation Oscillator frequency MCAN module clock frequency MCU bus frequency	 f_{OSC} f_{CAN} f_{MCU}	 0 0 0	 22 11 2.2	 MHz MHz MHz
Cycle time (see Figure 10-1)	t_{CYC}	455	—	ns
Crystal oscillator start-up time (see Figure 10-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width (mask option) 4064 cycle 16 cycle	 t_{PORL} t_{PORL}	 4064 16	 — —	 t_{CYC} t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time	t_{ERA}	10	10	ms
EEPROM byte program time(1)	t_{PROG}	10	10	ms
Timer (see Figure A-3) Resolution(2) Input capture pulse width Input capture pulse period	 t_{RESL} t_{TH}, t_{TL} t_{TLTL}	 4 125 —(3)	 — — —	 t_{CYC} ns t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns
Write/erase endurance(5)(6)	—	10000		cycles
Data retention(5)(6)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{cyc}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

(5) At a temperature of 85°C.

(6) Refer to Reliability Monitor Report (currrent quarterly issue) for current failure rate information.

B
MC68HC705X32

Important note

The following applies to the D59J MC68HC705X32 mask set only.

– A mask option register (MOR) on the MC68HC705X32 allows the customer to select POR delay cycles and oscillator DIV ratio. However, during reset, options of 4064 cycles POR and DIV10 are forced, regardless of which options the customer has selected. Therefore, a power-on reset delay of 40640 oscillator cycles is forced.

On the D59J mask set, the oscillator divide ratio depends on the CANE pin:

CANE = 1 DIV10 forced in bootloader mode
CANE = 0 DIV2 forced in bootloader mode

On later mask set revisions, including G47V, DIV2 is forced in bootloader mode, regardless of the CANE pin.

The following applies to the D40J and D59J MC68HC705X32 mask sets only:

– The minimum external RESET input pulse width, t_{RL} (Table B-10) is 1.5 t_{CYC}
– Maximum bus speed 2.2 MHz

The MC68HC705X32 is a device similar to the MC68HC05X16, but with 32K bytes of EPROM instead of 16K bytes of ROM. In addition, the bootstrap routines available in the MC68HC05X16 are replaced by bootstrap routines specific to the MC68HC705X32. The entire MC68HC05X16 data sheet applies to the MC68HC705X32, with the exceptions outlined in this appendix.

B.4 Block diagram, memory map and register outline

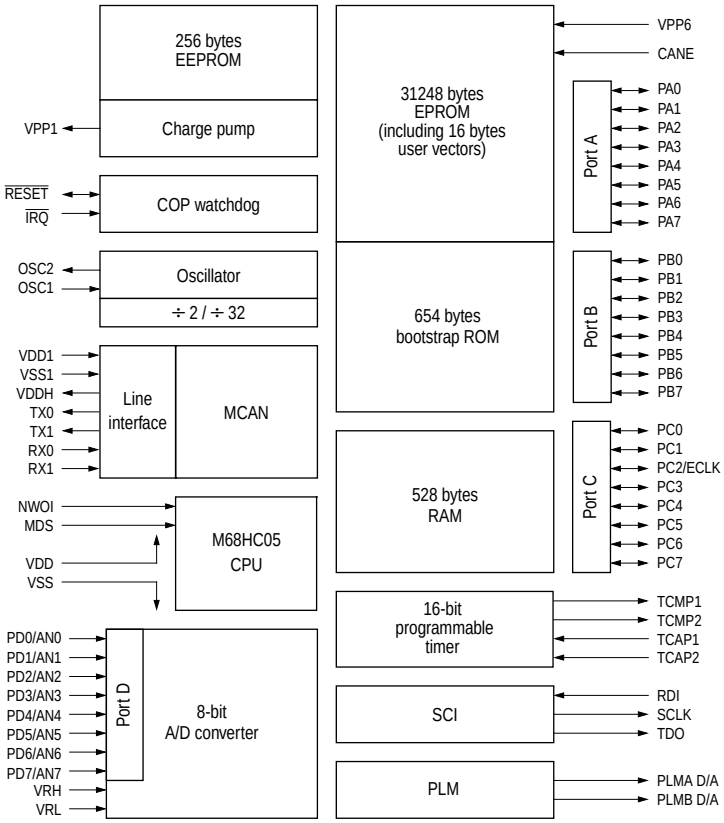

Figure B-1 MC68HC705X32 block diagram

B.9.6 MCAN bus interface DC electrical characteristics

Table B-12 MCAN bus interface DC electrical characteristics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Symbol	Min	Max	Unit
MCAN bus input comparator: pins RX0 and RX1				
Input voltage	V_{IN}	0.5	V_{DD} +0.5	V
Common mode range	C_{MR}	1.5	V_{DD} –1.5	V
Latch-up trigger current(1)	I_{LT}	–100	+100	mA
Input offset voltage	V_{OFS}	–30	+30	mV
Hysteresis	V_{HYS}	1	22	mV
V_{DD} ÷ 2 generator: pin VDDH				
Output voltage difference to V_{DD} ÷ 2 for –100 µA < I_{OUT} < +100 µA	DV_{OUT}	–200	+200	mV
Output current	I_{OUT}	–100	+100	µA
Latch-up trigger current[1]	I_{LT}	–100	+100	mA
MCAN bus output driver: pins TX0 and TX1				
Source current per pin (V_{OUT} = V_{DD}–1.0V)	I_{OH}	–10	—	mA
Sink current per pin (V_{OUT} = 1.0V)	I_{OL}	10	—	mA
Latch-up trigger current[1]	I_{LT}	–100	+100	mA

(V_{DD} = 5.0 Vdc ± 2%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Symbol	Min	Max	Unit
V_{DD} ÷ 2 generator: pin VDDH				
Output voltage difference to V_{DD} ÷ 2 for –100 µA < I_{OUT} < +100 µA	DV_{OUT}	–180	+180	mV

(1) Maximum DC current should comply with maximum ratings.

B.9.7 MCAN bus interface control timing characteristics

Table B-13 MCAN bus interface control timing characteristics

(4.5V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Symbol	Min	Max	Unit
MCAN bus output driver				
Rise and fall time (C_{LOAD} = 100pF)	T_{RF}	—	25	ns

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C.2 Control Timing

Table C-2 Control timing

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Oscillator frequency	f_{OSC}	0	16	MHz
MCAN module clock frequency	f_{CAN}	0	4	MHz
MCU bus frequency	f_{MCU}	0	4	MHz
Cycle time (see Figure 10-1)	t_{CYC}	250	—	ns

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