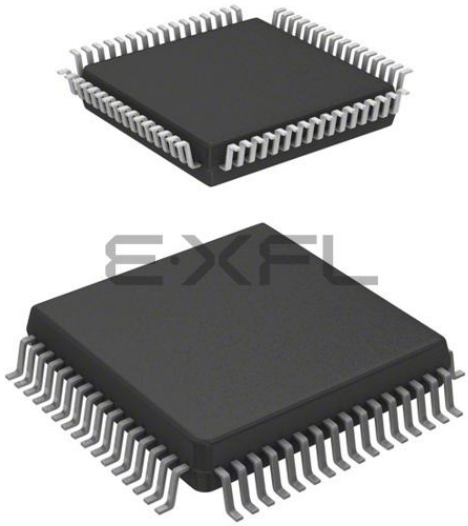

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	CANbus, SCI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	528 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705x32vfue

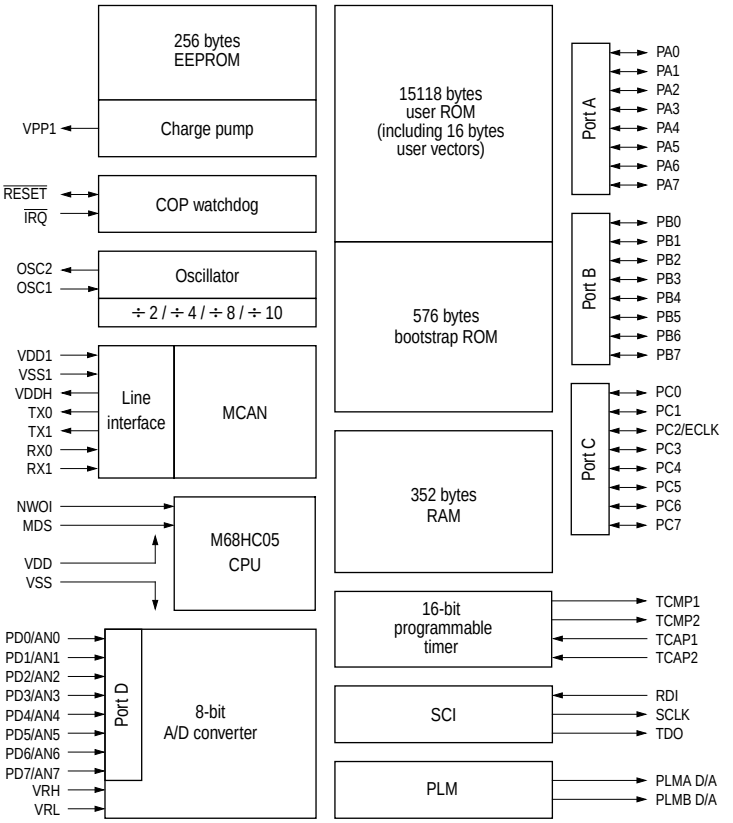
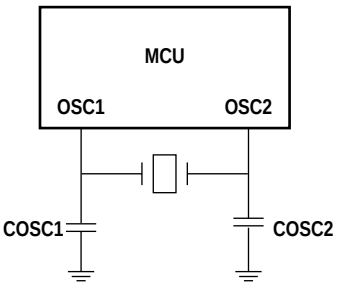
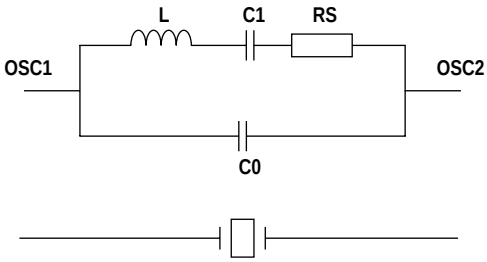


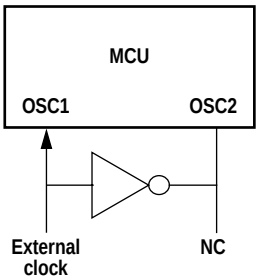
Figure 1-1 MC68HC05X16 block diagram



(a) Crystal/ceramic resonator oscillator connections



(b) Crystal equivalent circuit



(c) External clock source connections

Crystal

	2MHz	4MHz	Unit
R_S(max)	400	75	W
C_0	5	7	pF
C_1	8	12	*f*F
C_{OSC1}	15 – 40	15 – 30	pF
C_{OSC2}	15 – 30	15 – 25	pF
Q	30 000	40 000	—

Ceramic resonator

	2 – 4MHz	Unit
R_S(typ)	10	W
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
Q	1250	—

(d) Typical crystal and ceramic resonator parameters

Figure 2-6 Oscillator connections

2.3.21 VDD1

This pin is the power input for the input comparator of the MCAN module.

2.3.22 VSS1

This pin is the ground connection for the input comparator of the MCAN bus.

2.3.23 VDDH

This pin provides the high voltage reference output for the MCAN bus. The output voltage is equal to VDD÷2.

2.3.24 RX0/RX1

These input pins connect the physical bus lines to the input comparator (receive). When the MCAN is in SLEEP mode, a dominant level on these pins will wake it up.

2.3.25 TX0/TX1

These output pins connect the output drivers of the MCAN bus to the physical bus lines (transmit).

MCAN bus lines. The bus can have one of two complementary values: dominant or recessive. During simultaneous transmission of dominant and recessive bits the resulting bus value will be dominant. For example with a positive logic wired-AND implementation of the bus, the dominant level would correspond to a logic 0 and the recessive level to a logic 1.

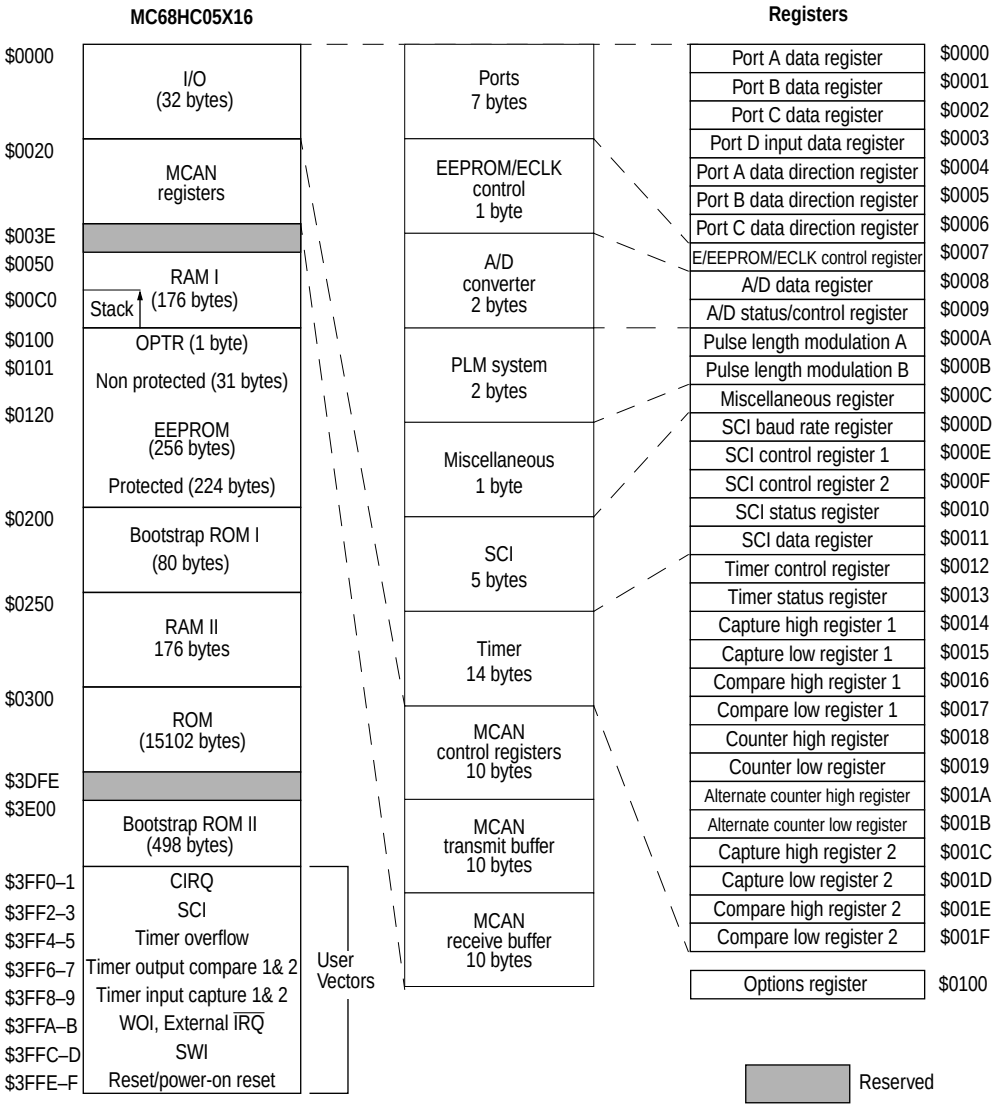


Figure 3-1 Memory map of the MC68HC05X16

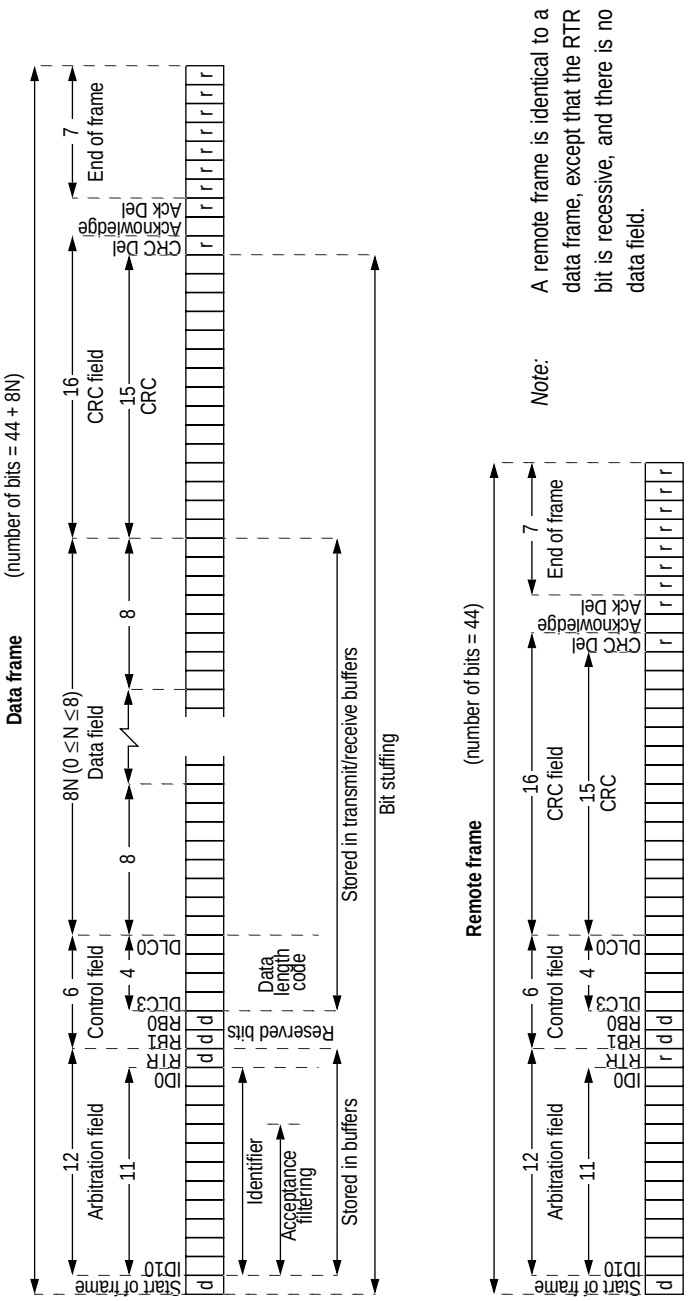


Figure 5-2 MCAN frame formats

RIF — Receive interrupt flag

The RIF bit is set by the MCAN when a new message is available in the receive buffer, and the RIE bit in CCNTRL is set. At the same time RBS is set. Like all the bits in this register, RIF is cleared by reading the register, or when reset request is set.

1 (set) – A new message is available in the receive buffer.

0 (clear) – No receive interrupt has occurred.

5.3.5 MCAN acceptance code register (CACC)

On reception each message is written into the current receive buffer. The MCU is only signalled to read the message however, if it passes the criteria in the acceptance code and acceptance mask registers (accepted); otherwise, the message will be overwritten by the next message (dropped).

Note: This register can only be accessed when the reset request bit in the CCNTRL register is set.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
MCAN acceptance code (CACC)	$0024	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Undefined

AC7 – AC0 — Acceptance code bits

AC7 – AC0 comprise a user defined sequence of bits with which the 8 most significant bits of the data identifier (ID10 – ID3) are compared. The result of this comparison is then masked with the acceptance mask register. Once a message has passed the acceptance criterion the respective identifier, data length code and data are sequentially stored in a receive buffer, providing there is one free. If there is no free buffer, the data overrun condition will be signalled.

On acceptance the receive buffer status bit is set to full and the receive interrupt bit is set (provided RIE = enabled).

6.2 Timer control and status

The various functions of the timer are monitored and controlled using the timer control and status registers described below.

6.2.1 Timer control register (TCR)

The timer control register ($0012) is used to enable the input captures (ICIE), output compares (OCIE), and timer overflow (TOIE) functions as well as forcing output compares (FOLV1 and FOLV2), selecting input edge sensitivity (IEDG1) and levels of output polarity (OLV1 and OLV2).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLV1	0000 00u0

ICIE — Input captures interrupt enable

If this bit is set, a timer interrupt is enabled whenever the ICF1 or ICF2 status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

OCIE — Output compares interrupt enable

If this bit is set, a timer interrupt is enabled whenever the OCF1 or OCF2 status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

TOIE — Timer overflow interrupt enable

If this bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

7
SERIAL COMMUNICATIONS INTERFACE

A full-duplex asynchronous serial communications interface (SCI) is provided with a standard non-return-to-zero (NRZ) format and a variety of baud rates. The SCI transmitter and receiver are functionally independent and have their own baud rate generator; however they share a common baud rate prescaler and data format.

The serial data format is standard mark/space (NRZ) and provides one start bit, eight or nine data bits, and one stop bit.

The SCLK pin is the output of the transmitter clock. It outputs the transmitter data clock for synchronous transmission (no clocks on start bit and stop bit, and a software option to send clock on last data bit). This allows control of peripherals containing shift registers (e.g. LCD drivers). Phase and polarity of these clocks are software programmable.

Any SCI bidirectional communication requires a two-wire system: receive data in (RDI) and transmit data out (TDO).

‘Baud’ and ‘bit rate’ are used synonymously in the following description.

7.1 SCI two-wire system features

- Standard NRZ (mark/space) format
- Advanced error detection method with noise detection for noise duration of up to 1/16th bit time
- Full-duplex operation (simultaneous transmit and receive)
- 32 software selectable baud rates
- Different baud rates for transmit and receive; for each transmit baud rate, 8 possible receive baud rates
- Software selectable word length (eight or nine bits)
- Separate transmitter and receiver enable bits
- Capable of being interrupt driven
- Transmitter clocks available without altering the regular transmitter or receiver functions
- Four separate enable bits for interrupt control

10.1.1 Power-on reset

A power-on reset occurs when a positive transition is detected on VDD. The power-on reset function is strictly for power turn-on conditions and should not be used to detect drops in the power supply voltage. The power-on circuitry provides a stabilization delay (t_{PORL}) from when the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of this delay then the processor remains in the reset state until $\overline{\text{RESET}}$ goes high. The user must ensure that the voltage on VDD has risen to a point where the MCU can operate properly by the time t_{PORL} has elapsed. If there is doubt, the external $\overline{\text{RESET}}$ pin should remain low until the voltage on VDD has reached the specified minimum operating voltage. This may be accomplished by connecting an external RC circuit to this pin to generate a power-on reset (POR). In this case, the time constant must be great enough to allow the oscillator circuit to stabilize.

During power-on reset, the $\overline{\text{RESET}}$ pin is driven low during a t_{PORL} delay start-up sequence. t_{PORL} is defined by a user specified mask option to be either 16 cycles or 4064 cycles (see Section 1.2).

A software distinction between a power-on reset and an external reset can be made using the POR bit in the miscellaneous register (see Section 10.1.2).

10.1.2 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	u001 000u

(1) The POR bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent on the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

POR — Power-on reset bit

This bit is set each time the device is powered on. Therefore, the state of the POR bit allows the user to make a software distinction between a power-on and an external reset. This bit cannot be set by software and is cleared by writing it to zero.

1 (set) – A power-on reset has occurred.

0 (clear) – No power-on reset has occurred.

Note: The bits shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

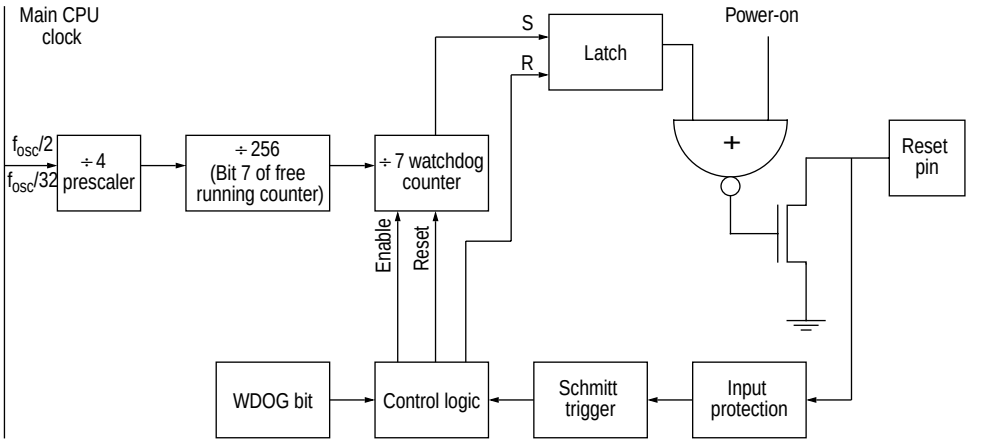


Figure 10-3 Watchdog system block diagram

The watchdog system can be automatically enabled, following power-on or external reset, via a mask option (see Section 1.2), or it can be enabled by software by writing a '1' to the WDOG bit in the miscellaneous register at $000C (see Section 10.1.2). Once enabled, the watchdog system cannot be disabled by software (writing a 'zero' to the WDOG bit has no effect at any time). In addition, the WDOG bit acts as a reset mechanism for the watchdog counter. Writing a '1' to this bit clears the counter to its initial value and prevents a watchdog timeout.

WDOG — Watchdog enable/disable

The WDOG bit can be used to enable the watchdog timer previously disabled by a mask option. Following a watchdog reset the state of the WDOG bit is as defined by the mask option specified.

1 (set) – Watchdog enabled and counter cleared.

0 (clear) – The watchdog cannot be disabled by software; writing a zero to this bit has no effect.

The divide-by-7 watchdog counter will generate a main reset of the chip when it reaches its final state; seven clocks are necessary to bring the watchdog counter from its clear state to its final state. This reset appears after time t_{DOG} since the last clear or since the enable of the watchdog counter system. The watchdog counter, therefore, has to be cleared periodically, by software, with a period less than t_{DOG}.

The reset generated by the watchdog system is apparent at the $\overline{\text{RESET}}$ pin (see Figure 10-3). The $\overline{\text{RESET}}$ pin level is re-entered in the control logic, and when it has been maintained at level 'zero' for a minimum of t_{DOGL}, the $\overline{\text{RESET}}$ pin is released.

10.2 Interrupts

The MCU can be interrupted by five different sources: three maskable hardware interrupts, one non maskable software interrupt and one maskable MCAN interrupt:

- External signal on the $\overline{IRQ}$ pin, WOI on port B pins or NWOI pin
- Serial communications interface (SCI)
- Programmable timer
- Software interrupt instruction (SWI)
- MCAN interrupt (CIRQ)

Interrupts cause the processor to save the register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. The RTI instruction (return from interrupt) causes the register contents to be recovered from the stack and normal processing to resume. While executing the RTI instruction, the value of the I-bit is replaced by the corresponding I-bit stored on the stack.

Unlike reset, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete. The current instruction is the one already fetched and being operated on. When the current instruction is complete, the processor checks all pending hardware interrupts. If interrupts are not masked (I-bit clear) and the corresponding interrupt enable bit is set, the processor proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

Note: Power-on and external reset clear all interrupt enable bits to prevent interrupts during the reset sequence, but set the INTE bit (see Section 3.8).

10.2.3.1 Miscellaneous register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous	$000C	POR	INTP	INTN	INTE	SFA	SFB	SM	WDOG	u001 000u

Note: The bits shown shaded in the above representation are explained individually in the relevant sections of this manual. The complete register plus an explanation of each bit can be found in Section 3.8.

INTP, INTN — External interrupt sensitivity options

These two bits allow the user to select which edge the $\overline{\text{IRQ}}$ and WOI pins are sensitive to as shown in Table 10-3. Both bits can be written to only while the I-bit is set, and are cleared by power-on or external reset. Therefore the device is initialised with negative edge and low level sensitivity.

Table 10-3 $\overline{\text{IRQ}}$ and WOI sensitivity

INTP	INTN	$\overline{\text{IRQ}}$ sensitivity	WOI interrupt sensitivity
0	0	Negative edge and low level sensitive	Positive edge and high level sensitive
0	1	Negative edge only	Positive edge only
1	0	Positive edge only	Negative edge only
1	1	Positive and negative edge sensitive	Positive and negative edge sensitive

Interrupt sensitivity options selected by INTP and INTN of the miscellaneous register apply to external interrupt signal, EI. EI is an OR function of all enabled WOI pins (port B and NWOI) and of the inverted value of the $\overline{\text{IRQ}}$ pin. When one WOI pin is high, it masks any subsequent edge or level on any other EI pin ($\overline{\text{IRQ}}$, port B or NWOI).

INTE — External interrupt enable

1 (set) – External interrupt ($\overline{\text{IRQ}}$) and wired-OR interrupt (WOI) enabled.

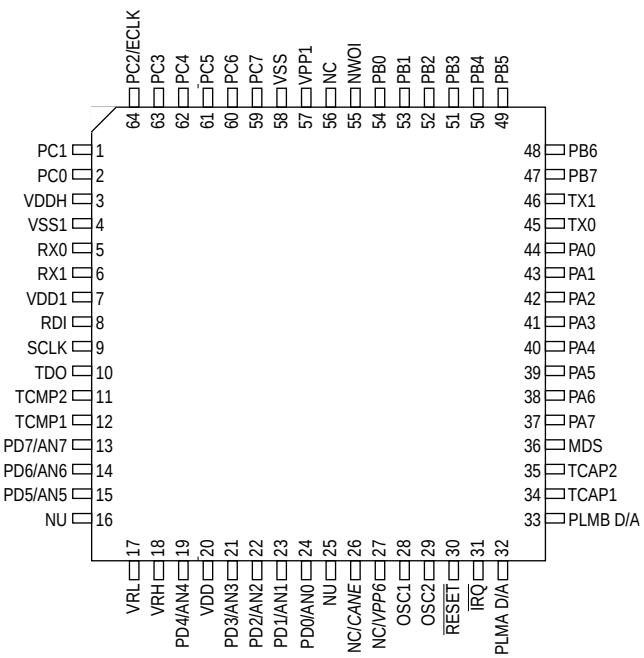
0 (clear) – External interrupt ($\overline{\text{IRQ}}$) and wired-OR interrupt (WOI) disabled.

The INTE bit can be written to only while the I-bit is set, and is set by power-on or external reset, thus enabling the external interrupt function.

Table 10-3 describes the various triggering options available for the $\overline{\text{IRQ}}$ and WOI pins, however it is important to re-emphasize here that in order to avoid any conflict and spurious interrupt, it is possible to change the external interrupt options only while the I-bit is set. Any attempt to change the external interrupt option while the I-bit is clear will be unsuccessful. If an external interrupt is pending, it will automatically be cleared when selecting a different interrupt option.

13
MECHANICAL DATA

13.1 64-pin quad flat pack (QFP) pinout



Device	Pin 26	Pin 27
MC68HC05X16, MC68HC05X32	NC	NC
MC68HC705X32	*CANE*	*VPP6*

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Note: Unless otherwise stated, a pin labelled 'NU' should be tied to V_{SS} in an electrically noisy environment. Pins labelled 'NC' can be left floating, since they are not bonded to any part of the device.

Figure 13-1 64-pin QFP pinout

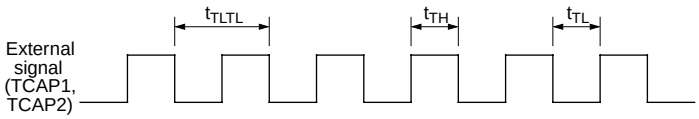


Figure A-3 Timer relationship

A.3.5 MCAN bus interface DC electrical characteristics

Table 1-6 MCAN bus interface DC electrical characteristics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Symbol	Min	Max	Unit
MCAN bus input comparator: pins RX0 and RX1				
Input voltage	V_{IN}	0.5	V_{DD} +0.5	V
Common mode range	C_{MR}	1.5	V_{DD} –1.5	V
Latch-up trigger current(1)	I_{LT}	–100	+100	mA
Input offset voltage	V_{OFS}	–30	+30	mV
Hysteresis	V_{HYS}	1	22	mV
V_{DD} ÷ 2 generator: pin VDDH				
Output voltage difference to V_{DD} ÷ 2 for –100 µA < I_{OUT} < +100 µA	DV_{OUT}	–200	+200	mV
Output current	I_{OUT}	–100	+100	mA
Latch-up trigger current(1)	I_{LT}	–100	+100	mA
MCAN bus output driver: pins TX0 and TX1				
Source current per pin (V_{OUT} = V_{DD}–1.0V)	I_{OH}	–10	—	mA
Sink current per pin (V_{OUT} = 1.0V)	I_{OL}	10	—	mA
Latch-up trigger current(1)	I_{LT}	–100	+100	mA

(V_{DD} = 5.0 Vdc ± 2%, V_{SS} = 0 Vdc, T_A = –40°C to +125°C)

Characteristic	Symbol	Min	Max	Unit
V_{DD} ÷ 2 generator: pin VDDH				
Output voltage difference to V_{DD} ÷ 2 for –100 µA < I_{OUT} < +100 µA	DV_{OUT}	–180	+180	mV

(1) Maximum DC current should comply with maximum ratings.

A.3.6 MCAN bus interface control timing characteristics

Table 1-7 MCAN bus interface control timing characteristics

($4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0$ Vdc, $T_A = -40°C$ to $+125°C$)

Characteristic	Symbol	Min	Max	Unit
MCAN bus output driver Rise and fall time (C_{LOAD} = 100pF)	T_{RF}	—	25	ns

B.1 Features

- –40 to +125°C operating temperature range
- 31232 bytes user EPROM plus 16 bytes of EPROM user vectors
- 528 bytes of RAM
- 654 bytes bootstrap ROM
- Simultaneous programming of up to 16 bytes of EPROM
- 4 MHz bus speed
- Available in 64-pin QFP package

Note: The electrical characteristics for the MC68HC05X16 should not be used for the MC68HC705X32. Section B.9.2 and Section B.9.5 contain data specific to this device.

B.2 VPP6

The VPP6 pin is the voltage input for the EPROM in both read and programming modes (see Section B.5).

B.3 CANE

This pin is the MCAN enable input. If CANE is connected to VDD, the internal MCAN module is selected and its registers are mapped at addresses $0020 to $003D.

Note: Although this pin can be left floating to disconnect the MCAN module, it is advisable to connect it to VSS when the module is not in use.

B.5.2 EPROM program operation

Typically the EPROM will be programmed by the bootstrap routines resident in the on-chip ROM. However, the user program can be used to program some EPROM locations if the proper procedure is followed. In particular, the programming sequence must be running in RAM, as the EPROM will not be available for code execution while the E6LAT bit is set. The V_{PP6} switching must occur externally after the E6PGM bit is set, for example under control of a signal generated on a pin by the programming routine.

Note: When the part becomes a PROM, only the cumulative programming of bits to logic '1' is possible if multiple programming is made on the same byte.

To allow simultaneous programming of up to sixteen bytes, these bytes must be in the same group of addresses which share the same most significant address bits; only the four least significant bits can change.

B.5.3 EPROM/EEPROM/ECLK control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EPROM/EEPROM/ECLK control	$0007	WOIE	CAF	E6LAT	E6PGM	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

WOIE — Wired-OR interrupt enable bit

1 (set) – Wired-OR interrupts are enabled, provided the WOI bit in register MOR is set.

0 (clear) – Wired-OR interrupts are disabled.

The WOIE bit can be used to enable the wired-OR interrupts (WOI) on the NWOI pin and on all port B pins that have been programmed as inputs. WOI is activated if the WOIE bit is set and if the WOI bit in the mask options register (MOR) is also set (see Section B.7). If WOI is not set then WOIE is forced to zero. External and power-on resets clear the WOIE bit.

CAF — MCAN asleep flag

This flag is set by the MCU when the MCAN module enters SLEEP mode.This is the only indication that the MCAN is asleep (see Section 5.5). The bit is cleared when the MCAN wakes up.

1 (set) – The MCAN module is in sleep mode.

0 (clear) – The MCAN module is not in sleep mode.

B.8 Bootstrap mode

Oscillator divide-by-two is forced in bootstrap mode; all other options stay as programmed in the mask options register (see Section B.7).

The bootstrap firmware is located in mask ROM at address locations $0200 to $024F, $03B0 to $3FFF, $7E00 to $7FDD and $7FE0 to $7FEF. This firmware can be used to program the EPROM and the EEPROM, to check if the EPROM is erased, or to load and execute routines in RAM.

After reset, while going to the bootstrap mode, the vector located at address $7FEE and $7FEF ($\overline{\text{RESET}}$) is fetched to start execution of the bootstrap program. To place the part in bootstrap mode, the following conditions must be met during transition of the $\overline{\text{RESET}}$ pin from low to high:

1) $\overline{\text{IRQ}}$ pin at $2xV_{DD}$ or MDS pin at V_{DD}
2) TCAP1 pin at V_{DD}
3) TCAP2 pin at V_{SS}

The hold time on the $\overline{\text{IRQ}}$, MDS, TCAP1 and TCAP2 pins is two clock cycles after the external $\overline{\text{RESET}}$ pin is brought high.

When the MC68HC705X32 is placed in the bootstrap mode, the bootstrap reset vector will be fetched and the bootstrap firmware will start to execute. Table B-5 shows the conditions required to enter each level of bootstrap mode on the rising edge of $\overline{\text{RESET}}$.

The bootstrap program first copies part of itself into RAM (except ‘RAM parallel load’), as the program cannot be executed in ROM during verification/programming of the EPROM.

Table B-5 Mode of operation selection

MDS		$\overline{\text{IRQ}}$	TCAP1	TCAP2	PD1	PD2	PD3	PD4	Mode
V_{SS}	AND	V_{SS} to V_{DD}	V_{SS} to V_{DD}	x	x	x	x	x	Single-chip mode
									Bootstrap mode:
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	0	0	0	x	EPROM erase check
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	1	0	0	x	EPROM erase check, erase EEPROM, parallel EPROM/EEPROM program/verify
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	0	1	0	x	Parallel EEPROM only verify (SEC bit not active)
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	1	1	0	x	EPROM erase check, erase EEPROM, parallel EPROM only program/verify
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	x	1	1	0	Jump to RAM $0051 (SEC bit not active)
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	x	x	1	1	Serial RAM load and execute (SEC bit not active)

x = Don’t care

X

Z