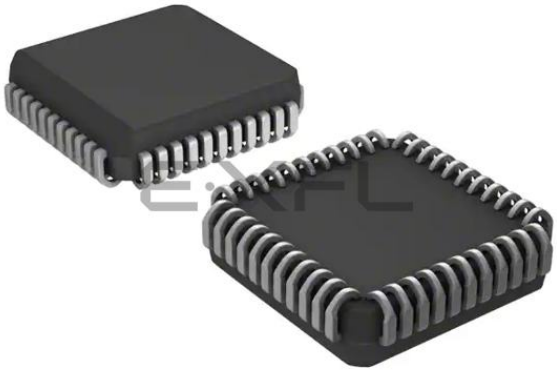

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lv51rb2ba-512

4. Block diagram

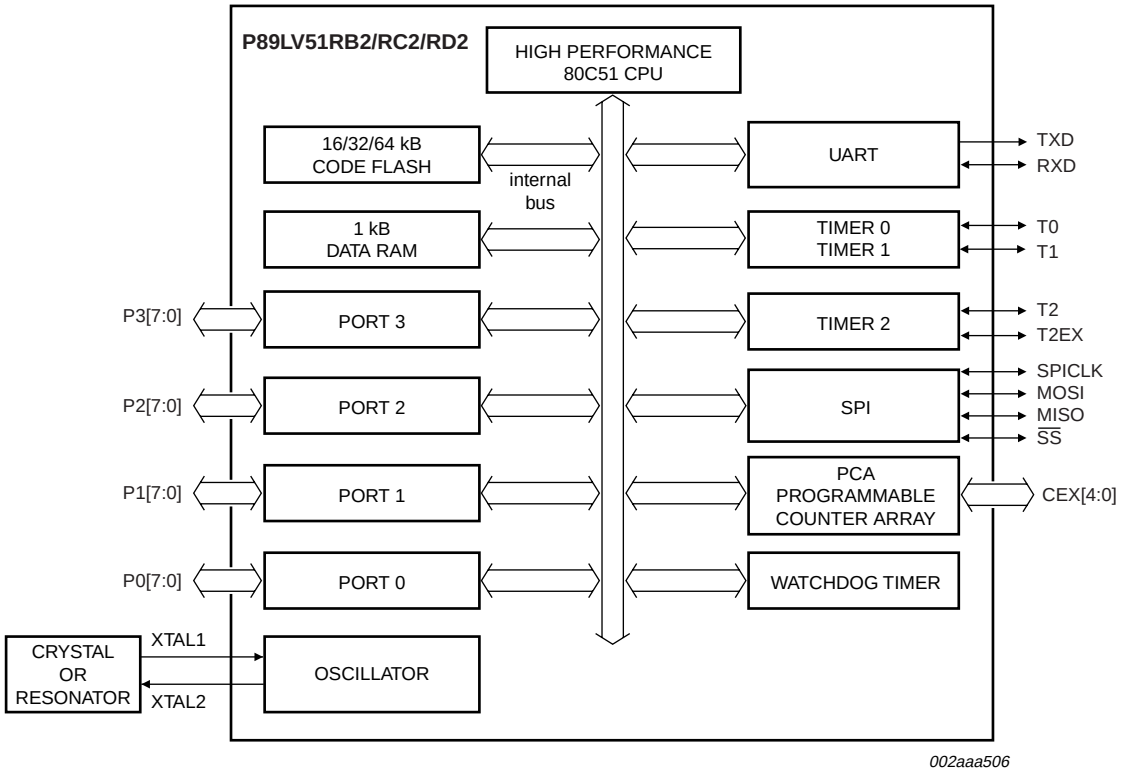

Fig 1. Block diagram

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Table 3. P89LV51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin		Type	Description
	TQFP44	PLCC44		
P2.7/A15	25	31	I/O	**P2.7 —** Port 2 bit 7.
			O	**A15 —** Address bit 15.
P3.0 to P3.7			I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3.0/RXD	5	11	I	**P3.0 —** Port 3 bit 0.
			I	**RXD —** Serial input port.
P3.1/TXD	7	13	O	**P3.1 —** Port 3 bit 1.
			O	**TXD —** Serial output port.
P3.2/$\overline{\text{INT0}}$	8	14	I	**P3.2 —** Port 3 bit 2.
			I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
P3.3/$\overline{\text{INT1}}$	9	15	I	**P3.3 —** Port 3 bit 3.
			I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P3.4/T0	10	16	I/O	**P3.4 —** Port 3 bit 4.
			I	**T0 —** External count input to Timer/counter 0.
P3.5/T1	11	17	I/O	**P3.5 —** Port 3 bit 5.
			I	**T1 —** External count input to Timer/counter 1.
P3.6/$\overline{\text{WR}}$	12	18	O	**P3.6 —** Port 3 bit 6.
			O	**$\overline{\text{WR}}$ —** External data memory write strobe.
P3.7/$\overline{\text{RD}}$	13	19	O	**P3.7 —** Port 3 bit 7.
			O	**$\overline{\text{RD}}$ —** External data memory read strobe.
$\overline{\text{PSEN}}$	26	32	I/O	**Program Store Enable**: $\overline{\text{PSEN}}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{\text{PSEN}}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. A forced HIGH-to-LOW input transition on the $\overline{\text{PSEN}}$ pin while the RST input is continually held HIGH for more than 10 machine cycles will cause the device to enter external host mode programming.
RST	4	10	I	**Reset**: While the oscillator is running, a HIGH logic state on this pin for two machine cycles will reset the device. If the $\overline{\text{PSEN}}$ pin is driven by a HIGH-to-LOW input transition while the RST input pin is held HIGH, the device will enter the external host mode, otherwise the device will enter the normal operation mode.
$\overline{\text{EA}}$	29	35	I	**External Access Enable**: $\overline{\text{EA}}$ must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. $\overline{\text{EA}}$ must be strapped to V_{DD} for internal program execution. The $\overline{\text{EA}}$ pin can tolerate a high voltage of 12 V.

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Table 3. P89LV51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin		Type	Description
	TQFP44	PLCC44		
ALE/$\overline{PROG}$	27	33	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input ($\overline{PROG}$) for flash programming. Normally the ALE[1] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[2] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if bit AO is set to '1', ALE is disabled.
n.c.	6, 17, 28, 39	1, 12, 23, 34	I/O	not connected
XTAL1	15	21	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	14	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	38	44	I	**Power supply**
V_{SS}	16	22	I	**Ground**

[1] ALE loading issue: When ALE pin experiences higher loading (> 30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to connect a pull-up resistor of 3 kΩ to 50 kΩ from pin ALE to V_{DD}.

[2] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

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work during initial power up, before the voltage reaches the brownout detection level. The POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain active until cleared by software.

Following a power-on or external reset the P89LV51RB2/RC2/RD2 will force the SWR and BSEL bits (FCF[1:0]) to 00. This causes the boot block to be mapped into the lower 8 kB of code memory and the device will execute the ISP code in the boot block and attempt to autobaud to the host. If the autobaud is successful the device will remain in ISP mode. If, after approximately 400 ms, the autobaud is unsuccessful the boot block code will check to see if the SoftICE flag is set (from a previous programming operation). If the SoftICE flag is set the device will enter SoftICE mode. If the SoftICE flag is cleared, the boot code will execute a software reset causing the device to execute the user code from block 0 starting at address 0000H. Note that an external reset applied to the RST pin has the same effect as a power-on reset.

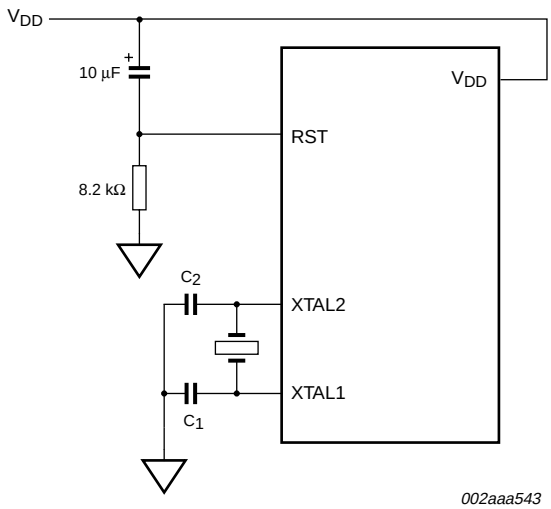

Fig 4. Power-on reset circuit

6.2.3 Software reset

A software reset is executed by changing the SWR bit (FCF.1) from '0' to '1'. A software reset will reset the program counter to address 0000H and force both the SWR and BSEL bits (FCF[1:0]) to 10. This will result in the lower 8 kB of the user code memory being mapped into the user code memory space. Thus the user's code will be executed starting at address 0000H. A software reset will not change bit WDTC.2 or RAM data. Other SFRs will be set to their reset values.

6.2.4 Brownout detect reset

The device includes a brownout detection circuit to protect the system from severe supply voltage fluctuations. The P89LV51RB2/RC2/RD2's brownout detection threshold is 2.35 V. When V_{DD} drops below this voltage threshold, the brownout detect triggers the circuit to generate a brownout interrupt but the CPU still runs until the supplied voltage returns to the brownout detection voltage V_{bo}. The default operation for a brownout detection is to cause a processor reset.

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Since the upper 128 B occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

Table 7. AUXR - Auxiliary register (address 8EH) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXTRAM	AO

Table 8. AUXR - Auxiliary register (address 8EH) bit descriptions

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to '0' by user programs.
1	EXTRAM	Internal/External RAM access using MOVX-@Ri/@DPTR. When '0', core attempts to access internal XRAM with address specified in MOVX instruction. If address supplied with this instruction exceeds on-chip available XRAM, off-chip XRAM is going to be selected and accessed. When '1', every MOVX-@Ri/@DPTR instruction targets external data memory by default.
0	AO	ALE off: disables/enables ALE. AO = 0 results in ALE emitted at a constant rate of $\frac{1}{2}$ the oscillator frequency. In case of AO = 1, ALE is active only during a MOVX or MOVC.

When instructions access addresses in the upper 128 B (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in '#data' is written to RAM location 90H rather than port 1.

Direct access:

MOV90H, #data; write data to P1

Data in '#data' is written to port 1. Instructions that write directly to the address, write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 B of memory is physically located on the chip and logically occupies the first 768 B of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 ($\overline{WR}$), P3.7 ($\overline{RD}$), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM access (indirect addressing only):

MOVX@DPTR, A DPTR contains 0A0H

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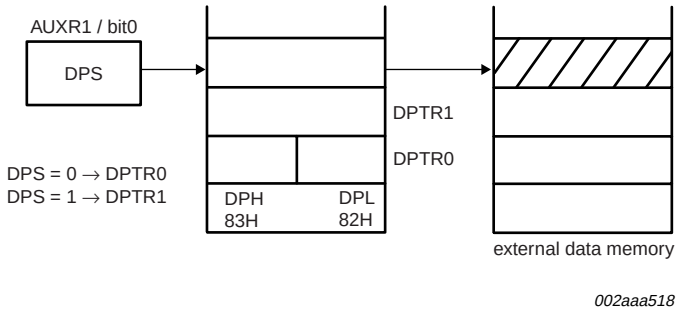

Fig 6. Dual data pointer organization

Table 10. AUXR1 - Auxiliary register 1 (address A2H) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	GF2	0	-	DPS

Table 11. AUXR1 - Auxiliary register 1 (address A2H) bit descriptions

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Should be set to ‘0’ by user programs.
3	GF2	General purpose user-defined flag.
2	0	This bit contains a hard-wired ‘0’. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to ‘0’ by user programs.
0	DPS	Data pointer select. Chooses one of two Data Pointers for use by the program. See text for details.

6.3 Flash memory IAP

6.3.1 Flash organization

The P89LV51RB2/RC2/RD2 program memory consists of a 16/32/64 kB block. ISP capability, in a second 8 kB block, is provided to allow the user code to be programmed in-circuit through the serial port. There are three methods of erasing or programming of the flash memory that may be used. First, the flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point (IAP). Second, the on-chip ISP bootloader may be invoked. This ISP bootloader will, in turn, call low-level routines through the same common entry point that can be used by the end-user application. Third, the flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device.

6.3.2 Boot block (block 1)

When the microcontroller programs its own flash memory, all of the low level details are handled by code that is contained in block 1. A user program calls the common entry point in the block 1 with appropriate parameters to accomplish the desired operation. Boot block operations include erase user code, program user code, program security bits, etc.

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Table 12. ISP hex record formats *…continued*

Record type	Command/data function
03	Miscellaneous Write functions :nnxxxx03ffssddcc Where: nn = number of bytes in the record xxxx = required field but value is a 'don't care' ff = subfunction code ss = selection code dd = data (if needed) cc = checksum Subfunction code = 01 (Erase block 0) ff = 01 Subfunction code = 05 (Program security bit, Double Clock) ff = 05 ss = 01 program security bit ss = 05 program double clock bit Subfunction code = 08 (Erase sector, 128 B) ff = 08 ss = high byte of sector address (A15:8) dd = low byte of sector address (A7, A6:0]= 0) Example: :0300000308E000F2 (erase sector at E000H)
04	Display Device Data or Blank Check :05xxxx04sssseeeeffcc Where 05 = number of bytes in the record xxxx = required field but value is a 'don't care' 04 = function code for display or blank check ssss = starting address, MSB first eeee = ending address, MSB first ff = subfunction 00 = display data 01 = blank check cc = checksum Subfunction codes: Example: :0500000400001FFF00D9 (display from 0000H to 1FFFH)

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Table 13. IAP function calls *...continued*

IAP function	IAP call parameters
Read Security Bit, Double Clock, SoftICE	**Input parameters:** ACC = 07H **Return parameter(s):** ACC = 000 S/N-match 0 SB 0 DBL_CLK
Read Security Bit, Double Clock, SoftICE	**Input parameters:** ACC = 07H **Return parameter(s):** ACC = 00 SoftICE S/N-match 0 SB 0 DBL_CLK
Erase sector	**Input parameters:** R1 = 08H DPH = sector address high byte DPL = sector address low byte **Return parameter(s):** ACC = 00 = pass ACC = !00 = fail

6.4 Timers/counters 0 and 1

The two 16-bit Timer/counter registers: Timer 0 and Timer 1 can be configured to operate either as timers or event counters (see Table 14 and Table 15).

In the ‘Timer’ function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of six oscillator periods, the count rate is $\frac{1}{6}$ of the oscillator frequency.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once every machine cycle.

When the samples show a HIGH in one cycle and a LOW in the next cycle, the count is incremented. The new count value appears in the register in the machine cycle following the one in which the transition was detected. Since it takes two machine cycles (12 oscillator periods) for 1-to-0 transition to be recognized, the maximum count rate is $\frac{1}{12}$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle. In addition to the ‘Timer’ or ‘Counter’ selection, Timer 0 and Timer 1 have four operating modes from which to select.

The ‘Timer’ or ‘Counter’ function is selected by control bits C/T in the special function register TMOD. These two timer/counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both timers/counters. Mode 3 is different. The four operating modes are described in the following text.

Table 14. TMOD - Timer/counter mode control register (address 89H) bit allocation

Not bit addressable; reset value: 0000 0000B; reset source(s): any source.

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

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Table 18. TCON - Timer/counter control register (address 88H) bit descriptions *...continued*

Bit	Symbol	Description
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level that triggers external interrupt 1.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge/low level is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level that triggers external interrupt 0.

6.4.1 Mode 0

Putting either Timer into mode 0 makes it look like an 8048 Timer, which is an 8-bit counter with a fixed divide-by-32 prescaler. Figure 7 shows mode 0 operation.

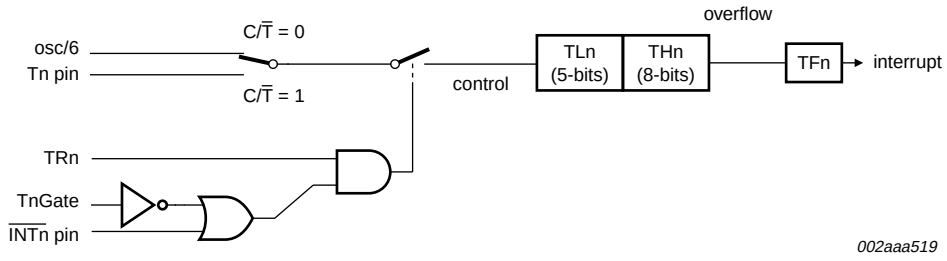

Fig 7. Timer/counter 0 or 1 in mode 0 (13-bit counter)

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements. TRn is a control bit in the Special Function Register TCON (Figure 6). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1 (see Figure 7). There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

6.4.2 Mode 1

Mode 1 is the same as mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 8.

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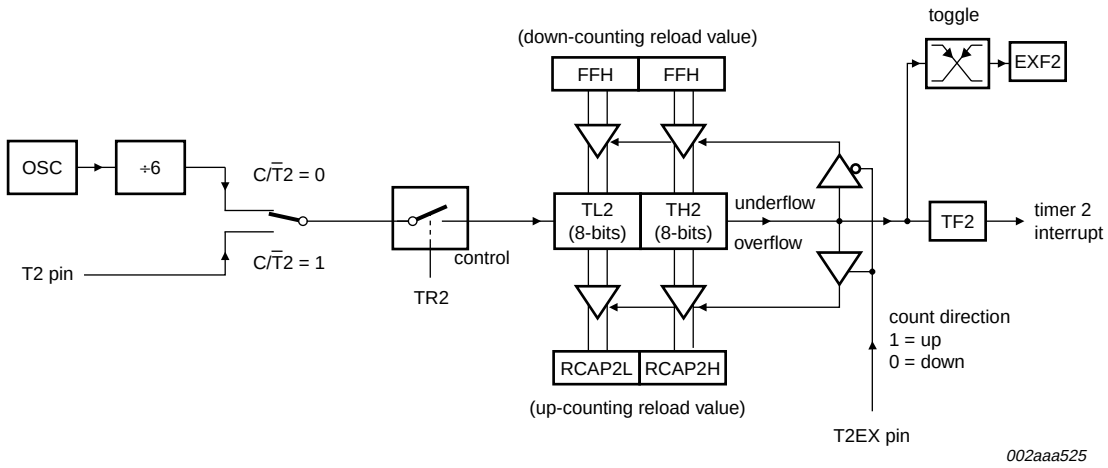

Fig 13. Timer 2 in Auto Reload mode (DCEN = 1)

A logic 0 applied at pin T2EX causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2. The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1.0). This pin, besides being a I/O pin, has two additional functions. It can be programmed:

- To input the external clock for Timer/counter 2, or
- To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the Timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{Oscillator\ Frequency}{2 \times (65536 \angle (RCAP2H, RCAP2L))} \quad (2)$$

Where (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART transmit and receive baud rates to be derived from either Timer 1 or Timer 2 (See Section 6.6 “UART” on page 37 for details). When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When

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The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF.

6.6.8 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed so that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in a way that the 9th bit is ‘1’ in an address byte and ‘0’ in the data byte. With SM2 = 1, no slave will be interrupted by a data byte, i.e. the received 9th bit is ‘0’. However, an address byte having the 9th bit set to ‘1’ will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed or not. The addressed slave will clear its SM2 bit and prepare to receive the data (still 9 bits long) that follow. The slaves that weren’t being addressed leave their SM2 bits set and ignore the subsequent data bytes.

SM2 has no effect in mode 0, and in mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. When the UART receives data in mode 1 and SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.6.9 Automatic address recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled for the UART by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the ‘Given’ address or the ‘Broadcast' address. The 9 bit mode requires that the 9th information bit is a ‘1’ to indicate that the received information is an address and not data.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two Special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are ‘don’t care’. The SADEN mask can be logically ANDed with the SADDR to create the ‘Given’ address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others.

This device uses the methods presented in Figure 15 to determine if a ‘Given’ or ‘Broadcast’ address has been received or not.

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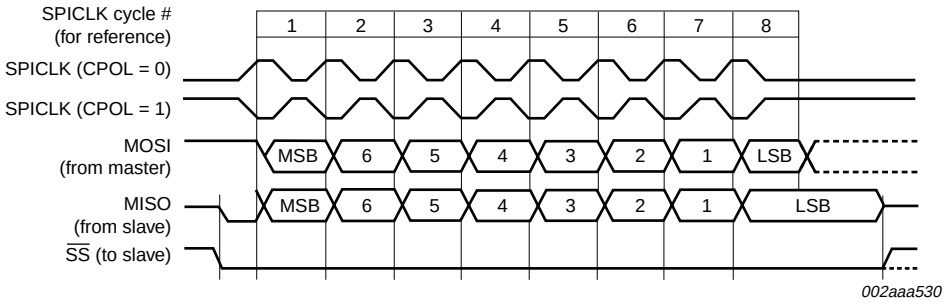

Fig 18. SPI transfer format with CPHA = 1

6.8 Watchdog timer

The device offers a programmable Watchdog Timer (WDT) for fail safe protection against software deadlock and automatic recovery.

To protect the system against software deadlock, the user software must refresh the WDT within a user-defined time period. If the software fails to do this periodical refresh, an internal hardware reset will be initiated if enabled (WDRE = 1). The software can be designed such that the WDT times out if the program does not work properly.

The WDT in the device uses the system clock (XTAL1) as its time base. So strictly speaking, it is a Watchdog counter rather than a WDT. The WDT register will increment every 344064 crystal clocks. The upper 8-bits of the time base register (WDTD) are used as the reload register of the WDT.

The WDTS flag bit is set by WDT overflow and is not changed by WDT reset. User software can clear WDTS by writing '1' to it.

Figure 19 provides a block diagram of the WDT. Two SFRs (WDTC and WDTD) control WDT operation. During Idle mode, WDT operation is temporarily suspended, and resumes upon an interrupt exit from idle.

The time-out period of the WDT is calculated as follows:

$$\text{Period} = (255 - \text{WDTD}) \times 344064 \times 1 / f_{CLK\ (XTAL1)}$$

where WDTD is the value loaded into the WDTD register and f_{osc} is the oscillator frequency.

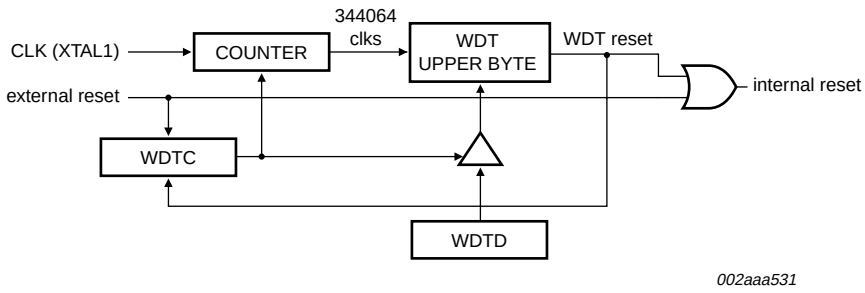

Fig 19. Block diagram of programmable WDT

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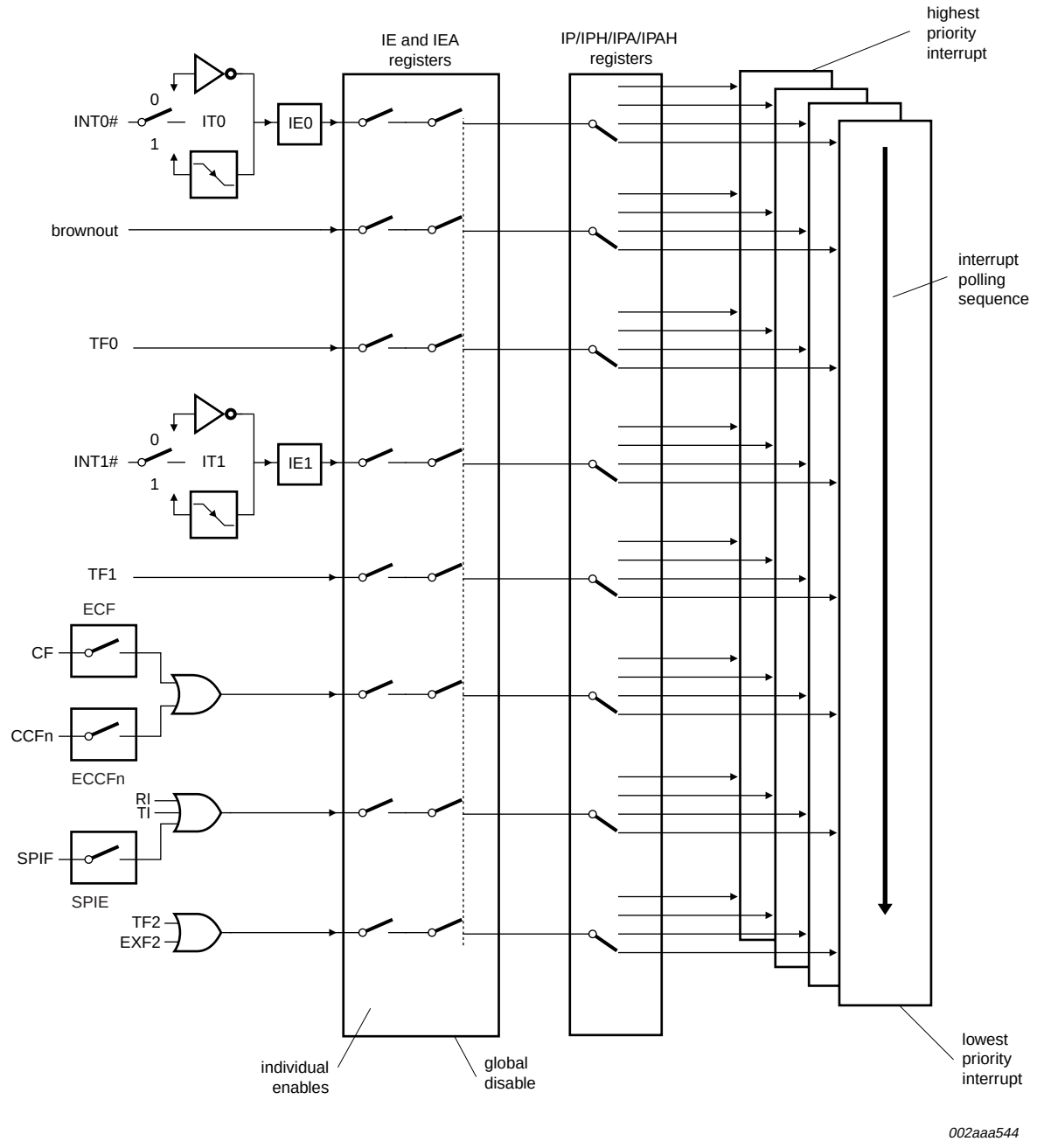

Fig 26. Interrupt structure

Table 44. IEN0 - Interrupt enable register 0 (address A8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

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Table 45. IEN0 - Interrupt enable register 0 (address A8H) bit descriptions

Bit	Symbol	Description
7	EA	Interrupt Enable Bit: EA = 1 interrupt(s) can be serviced, EA = 0 interrupt servicing disabled.
6	EC	PCA Interrupt Enable bit.
5	ET2	Timer 2 Interrupt Enable.
4	ES	Serial Port Interrupt Enable.
3	ET1	Timer 1 Overflow Interrupt Enable.
2	EX1	External Interrupt 1 Enable.
1	ET0	Timer 0 Overflow Interrupt Enable.
0	EX0	External Interrupt 0 Enable.

Table 46. IEN1 - Interrupt enable register 1 (address E8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EBO	-	-	-

Table 47. IEN1 - Interrupt enable register 1 (address E8H) bit descriptions

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Should be set to ‘0’ by user programs.
3	EBO	Brownout Interrupt Enable. 1 = enable, 0 = disable.
2 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

Table 48. IP0 - Interrupt priority 0 low register (address B8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Table 49. IP0 - Interrupt priority 0 low register (address B8H) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	PPC	PCA interrupt priority LOW bit.
5	PT2	Timer 2 interrupt priority LOW bit.
4	PS	Serial Port interrupt priority LOW bit.
3	PT1	Timer 1 interrupt priority LOW bit.
2	PX1	External interrupt 1 priority LOW bit.
1	PT0	Timer 0 interrupt priority LOW bit.
0	PX0	External interrupt 0 priority LOW bit.

Table 50. IP0H - Interrupt priority 0 high register (address B7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

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Table 51. IP0H - Interrupt priority 0 high register (address B7H) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	PPCH	PCA interrupt priority HIGH bit.
5	PT2H	Timer 2 interrupt priority HIGH bit.
4	PSH	Serial Port interrupt priority HIGH bit.
3	PT1H	Timer 1 interrupt priority HIGH bit.
2	PX1H	External interrupt 1 priority HIGH bit.
1	PT0H	Timer 0 interrupt priority HIGH bit.
0	PX0H	External interrupt 0 priority HIGH bit.

Table 52. IP1 - Interrupt priority 1 register (address F8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	PBO	-	-	-	-

Table 53. IP1 - Interrupt priority 1 register (address F8H) bit descriptions

Bit	Symbol	Description
7 to 5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	PBO	Brownout interrupt priority bit.
3 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

Table 54. IP1H - Interrupt priority 1 high register (address F7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	PBOH	-	-	-	-

Table 55. IP1H - Interrupt priority 1 high register (address F7H) bit descriptions

Bit	Symbol	Description
7 to 5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	PBOH	Brownout interrupt priority bit.
3 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

6.12 Power-saving modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are Idle and Power-down, see Table 56.

6.12.1 Idle mode

Idle mode is entered by setting the IDL bit in the PCON register. In Idle mode, the Program Counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

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7. Limiting values

Table 61. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_I	input voltage	on $\overline{EA}$ pin to V_{SS}	–0.5	+14	V
V_n	voltage on any other pin	except V_{SS}; with respect to V_{DD}	–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin	pins P1.5, P1.6, P1.7	-	20	mA
		all other pins	-	15	mA
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 62. Static characteristics

T_{amb} = 0 °C to +70 °C or –40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions		Min	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1]	10000	-	cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1]	100	-	years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1]	100 + I_{DD}	-	mA
V_{IL}	LOW-level input voltage	2.7 V < V_{DD} < 3.6 V		–0.5	+0.7	V
V_{IH}	HIGH-level input voltage	2.7 V < V_{DD} < 3.6 V		0.2V_{DD} + 0.9	V_{DD} + 0.5	V
		XTAL1, RST		0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	LOW-level output voltage	V_{DD} = 2.7 V; ports 1.5, 1.6, 1.7				
		I_{OL} = 16 mA		-	1.0	V
		V_{DD} = 2.7 V; ports 1, 2, 3, except $\overline{PSEN}$, ALE	[2][3][4]			
		I_{OL} = 100 µA		-	0.3	V
		I_{OL} = 1.6 mA		-	0.45	V
		I_{OL} = 3.5 mA		-	1.0	V
		V_{DD} = 2.7 V; port 0, $\overline{PSEN}$, ALE				
		I_{OL} = 200 µA		-	0.3	V
		I_{OL} = 3.2 mA		-	0.45	V

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Table 62. Static characteristics *...continued*

T_{amb} = 0 °C to +70 °C or −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	HIGH-level output voltage	V_{DD} = 2.7 V; ports 1, 2, 3, ALE, $\overline{PSEN}$	[5]			
		I_{OH} = −10 µA		V_{DD} − 0.3	-	V
		I_{OH} = −30 µA		V_{DD} − 0.7	-	V
		I_{OH} = −60 µA		V_{DD} − 1.5	-	V
		V_{DD} = 2.7 V; port 0 in External Bus mode				
		I_{OH} = −200 µA		V_{DD} − 0.3	-	V
		I_{OH} = −3.2 mA		V_{DD} − 0.7	-	V
V_{bo}	brownout trip voltage			2.35	2.55	V
I_{IL}	LOW-level input current	V_I = 0.4 V; ports 1, 2, 3		-	−75	µA
I_{THL}	HIGH-LOW transition current	V_I = 2 V; ports 1, 2, 3	[6]	-	−650	µA
I_{LI}	input leakage current	0.45 V < V_I < V_{DD} − 0.3 V; port 0		-	±10	µA
R_{pd}	pull-down resistance	on pin RST		-	225	kΩ
C_{iss}	input capacitance	1 MHz; T_{amb} = 25 °C	[7]	-	15	pF
$I_{DD(oper)}$	operating supply current	f_{osc} = 12 MHz		-	11.5	mA
		f_{osc} = 33 MHz		-	30	mA
$I_{DD(idle)}$	Idle mode supply current	f_{osc} = 12 MHz		-	8.5	mA
		f_{osc} = 33 MHz		-	21	mA
$I_{DD(pd)}$	Power-down mode supply current	minimum V_{DD} = 2 V				
		T_{amb} = 0 °C to +70 °C		-	45	µA
		T_{amb} = −40 °C to +85 °C		-	55	µA

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per 8-bit port: 26 mA

b) Maximum I_{OL} total for all outputs: 71 mA

c) If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[3] Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

[4] Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[5] Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD} − 0.7 V specification when the address bits are stabilizing.

[6] Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_I is approximately 2 V.

[7] Pin capacitance is characterized but not tested. Pin $\overline{EA}$ = 25 pF (max).

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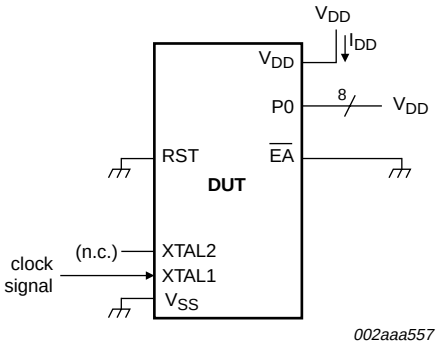
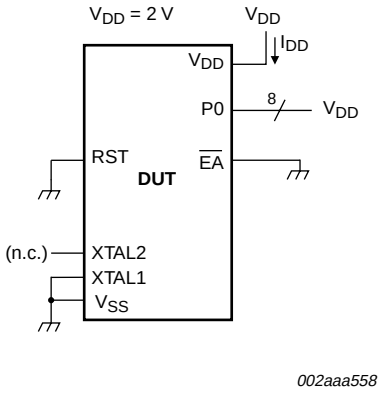


All other pins disconnected

Fig 36. I_{DD} test condition, Idle mode



All other pins disconnected

Fig 37. I_{DD} test condition, Power-down mode

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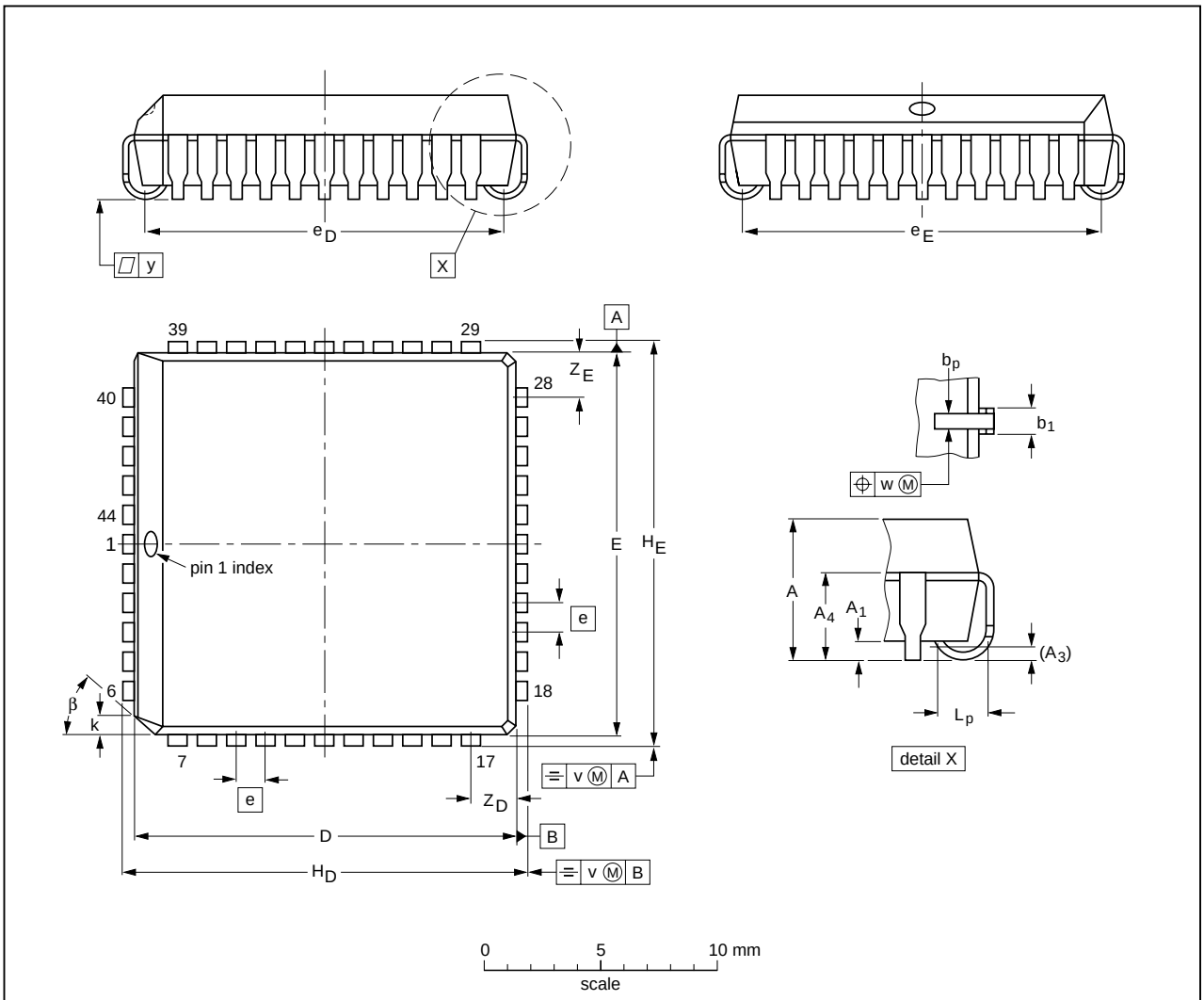
10. Package outline

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 38. Package outline SOT187-2 (PLCC44)

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11. Abbreviations

Table 66. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	Electro-Magnetic Interference
IAP	In-Application Programming
ISP	In-System Programming
MCU	Microcontroller Unit
PCA	Programmable Counter Array
PWM	Pulse Width Modulator
RC	Resistance-Capacitance
SFR	Special Function Register
SPI	Serial Peripheral Interface
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

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