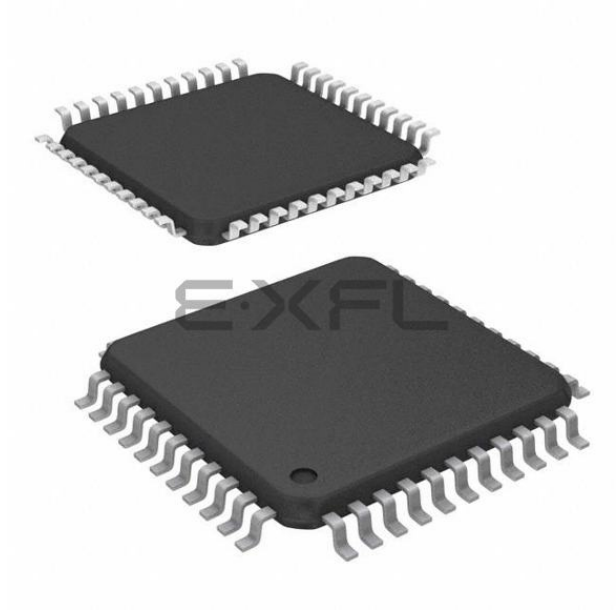

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lv51rb2bbc-557

Table 3. P89LV51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin		Type	Description
	TQFP44	PLCC44		
P1.3/CEX0	43	5	I/O	**P1.3 —** Port 1 bit 3.
			I/O	**CEX0 —** Capture/compare external I/O for PCA Module 0. Each capture/compare module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O.
P1.4/$\overline{SS}$/CEX1	44	6	I/O	**P1.4 —** Port 1 bit 4.
			I	**$\overline{SS}$ —** Slave port select input for SPI.
			I/O	**CEX1 —** Capture/compare external I/O for PCA Module 1.
P1.5/MOSI/ CEX2	1	7	I/O	**P1.5 —** Port 1 bit 5.
			I/O	**MOSI —** Master Output Slave Input for SPI.
			I/O	**CEX2 —** Capture/compare external I/O for PCA Module 2.
P1.6/MISO/ CEX3	2	8	I/O	**P1.6 —** Port 1 bit 6.
			I/O	**MISO —** Master Input Slave Output for SPI.
			I/O	**CEX3 —** Capture/compare external I/O for PCA Module 3.
P1.7/SPICLK/ CEX4	3	9	I/O	**P1.7 —** Port 1 bit 7.
			I/O	**SPICLK —** Serial clock input/output for SPI.
			I/O	**CEX4 —** Capture/compare external I/O for PCA Module 4.
P2.0 to P2.7			I/O with internal pull-up	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to '1's. Port 2 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P2.0/A8	18	24	I/O	**P2.0 —** Port 2 bit 0.
			O	**A8 —** Address bit 8.
P2.1/A9	19	25	I/O	**P2.1 —** Port 2 bit 1.
			O	**A9 —** Address bit 9.
P2.2/A10	20	26	I/O	**P2.2 —** Port 2 bit 2.
			O	**A10 —** Address bit 10.
P2.3/A11	21	27	I/O	**P2.3 —** Port 2 bit 3.
			O	**A11 —** Address bit 11.
P2.4/A12	22	28	I/O	**P2.4 —** Port 2 bit 4.
			O	**A12 —** Address bit 12.
P2.5/A13	23	29	I/O	**P2.5 —** Port 2 bit 5.
			O	**A13 —** Address bit 13.
P2.6/A14	24	30	I/O	**P2.6 —** Port 2 bit 6.
			O	**A14 —** Address bit 14.

Table 3. P89LV51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin		Type	Description
	TQFP44	PLCC44		
P2.7/A15	25	31	I/O	**P2.7 —** Port 2 bit 7.
			O	**A15 —** Address bit 15.
P3.0 to P3.7			I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3.0/RXD	5	11	I	**P3.0 —** Port 3 bit 0.
			I	**RXD —** Serial input port.
P3.1/TXD	7	13	O	**P3.1 —** Port 3 bit 1.
			O	**TXD —** Serial output port.
P3.2/$\overline{\text{INT0}}$	8	14	I	**P3.2 —** Port 3 bit 2.
			I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
P3.3/$\overline{\text{INT1}}$	9	15	I	**P3.3 —** Port 3 bit 3.
			I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P3.4/T0	10	16	I/O	**P3.4 —** Port 3 bit 4.
			I	**T0 —** External count input to Timer/counter 0.
P3.5/T1	11	17	I/O	**P3.5 —** Port 3 bit 5.
			I	**T1 —** External count input to Timer/counter 1.
P3.6/$\overline{\text{WR}}$	12	18	O	**P3.6 —** Port 3 bit 6.
			O	**$\overline{\text{WR}}$ —** External data memory write strobe.
P3.7/$\overline{\text{RD}}$	13	19	O	**P3.7 —** Port 3 bit 7.
			O	**$\overline{\text{RD}}$ —** External data memory read strobe.
$\overline{\text{PSEN}}$	26	32	I/O	**Program Store Enable**: $\overline{\text{PSEN}}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{\text{PSEN}}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. A forced HIGH-to-LOW input transition on the $\overline{\text{PSEN}}$ pin while the RST input is continually held HIGH for more than 10 machine cycles will cause the device to enter external host mode programming.
RST	4	10	I	**Reset**: While the oscillator is running, a HIGH logic state on this pin for two machine cycles will reset the device. If the $\overline{\text{PSEN}}$ pin is driven by a HIGH-to-LOW input transition while the RST input pin is held HIGH, the device will enter the external host mode, otherwise the device will enter the normal operation mode.
$\overline{\text{EA}}$	29	35	I	**External Access Enable**: $\overline{\text{EA}}$ must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. $\overline{\text{EA}}$ must be strapped to V_{DD} for internal program execution. The $\overline{\text{EA}}$ pin can tolerate a high voltage of 12 V.

Table 3. P89LV51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin		Type	Description
	TQFP44	PLCC44		
ALE/$\overline{PROG}$	27	33	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input ($\overline{PROG}$) for flash programming. Normally the ALE[1] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[2] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if bit AO is set to '1', ALE is disabled.
n.c.	6, 17, 28, 39	1, 12, 23, 34	I/O	not connected
XTAL1	15	21	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	14	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	38	44	I	**Power supply**
V_{SS}	16	22	I	**Ground**

[1] ALE loading issue: When ALE pin experiences higher loading (> 30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to connect a pull-up resistor of 3 kΩ to 50 kΩ from pin ALE to V_{DD}.

[2] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

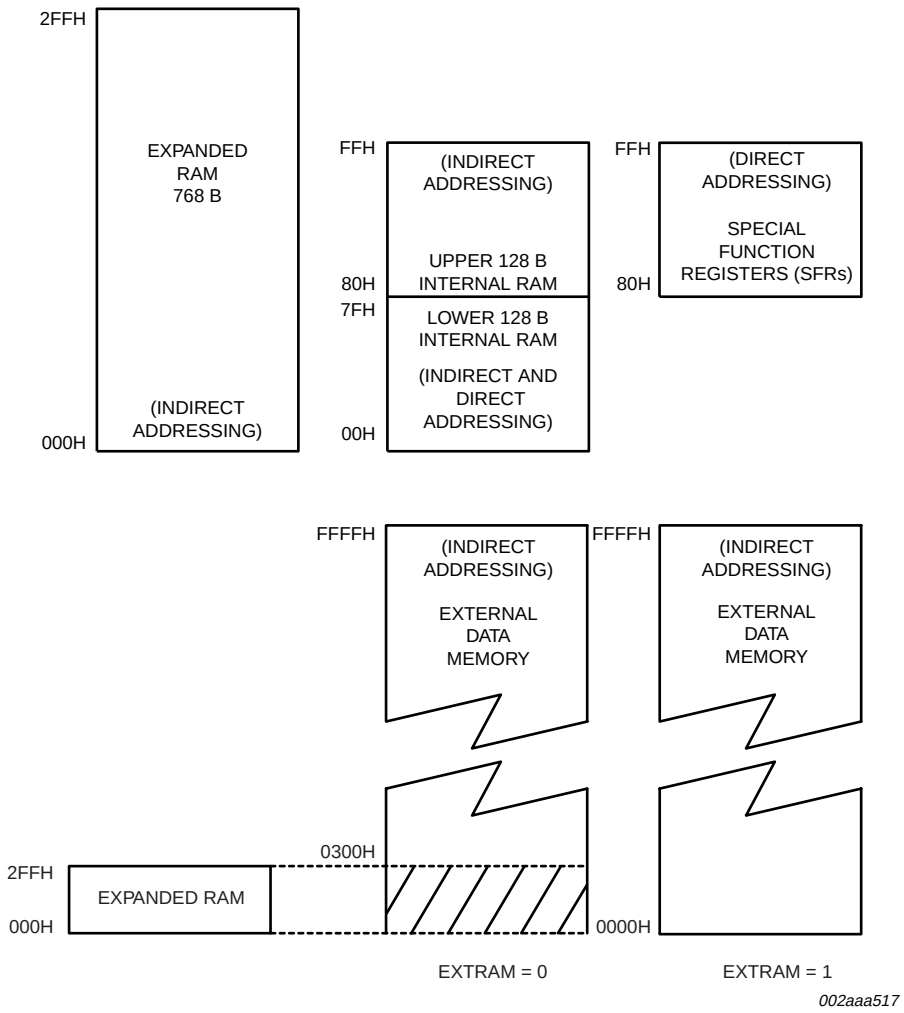


Fig 5. Internal and external data memory structure

6.2.8 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1 (see Figure 6).

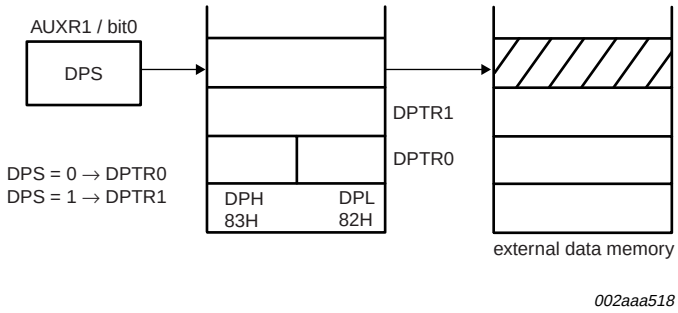


Fig 6. Dual data pointer organization

Table 10. AUXR1 - Auxiliary register 1 (address A2H) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	GF2	0	-	DPS

Table 11. AUXR1 - Auxiliary register 1 (address A2H) bit descriptions

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Should be set to ‘0’ by user programs.
3	GF2	General purpose user-defined flag.
2	0	This bit contains a hard-wired ‘0’. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to ‘0’ by user programs.
0	DPS	Data pointer select. Chooses one of two Data Pointers for use by the program. See text for details.

6.3 Flash memory IAP

6.3.1 Flash organization

The P89LV51RB2/RC2/RD2 program memory consists of a 16/32/64 kB block. ISP capability, in a second 8 kB block, is provided to allow the user code to be programmed in-circuit through the serial port. There are three methods of erasing or programming of the flash memory that may be used. First, the flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point (IAP). Second, the on-chip ISP bootloader may be invoked. This ISP bootloader will, in turn, call low-level routines through the same common entry point that can be used by the end-user application. Third, the flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device.

6.3.2 Boot block (block 1)

When the microcontroller programs its own flash memory, all of the low level details are handled by code that is contained in block 1. A user program calls the common entry point in the block 1 with appropriate parameters to accomplish the desired operation. Boot block operations include erase user code, program user code, program security bits, etc.

Table 12. ISP hex record formats

Record type	Command/data function
00	Program User Code Memory :nnaaaa00dd..ddcc Where: nn = number of bytes to program aaaa = address dd..dd = data bytes cc = checksum Example: :10000000010203040500607080 9cc
01	End of File (EOF), no operation :xxxxxx01cc Where: xxxxxx = required field but value is a ‘don’t care’ cc = checksum Example: :00000001FF
02	Set SoftICE mode Following the next reset the device will enter the SoftICE mode. Will erase user code memory, and erase device serial number. :00000002cc Where: xxxxxx = required field but value is a ‘don’t care’ cc = checksum Example: :00000002FE

Table 12. ISP hex record formats *…continued*

Record type	Command/data function
03	Miscellaneous Write functions :nnxxxx03ffssddcc Where: nn = number of bytes in the record xxxx = required field but value is a 'don't care' ff = subfunction code ss = selection code dd = data (if needed) cc = checksum Subfunction code = 01 (Erase block 0) ff = 01 Subfunction code = 05 (Program security bit, Double Clock) ff = 05 ss = 01 program security bit ss = 05 program double clock bit Subfunction code = 08 (Erase sector, 128 B) ff = 08 ss = high byte of sector address (A15:8) dd = low byte of sector address (A7, A6:0]= 0) Example: :0300000308E000F2 (erase sector at E000H)
04	Display Device Data or Blank Check :05xxxx04sssseeeeffcc Where 05 = number of bytes in the record xxxx = required field but value is a 'don't care' 04 = function code for display or blank check ssss = starting address, MSB first eeee = ending address, MSB first ff = subfunction 00 = display data 01 = blank check cc = checksum Subfunction codes: Example: :0500000400001FFF00D9 (display from 0000H to 1FFFH)

Table 15. TMOD - Timer/counter mode control register (address 89H) bit descriptions

Bit	Symbol	Description
	T1/T0	Bits controlling Timer1/Timer0
	GATE	Gating control when set. Timer/counter 'x' is enabled only while 'INTx' $\overline{\text{INTx}}$ pin is HIGH and 'TRx' control pin is set. When cleared, Timer 'x' is enabled whenever 'TRx' control bit is set.
	C/$\overline{\text{T}}$	Gating Timer or Counter Selector cleared for Timer operation (input from internal system clock). Set for Counter operation (input from 'Tx' input pin).

Table 16. TMOD - Timer/counter mode control register (address 89H) M1/M0 operating mode

M1	M0	Operating mode	
0	0	0	8048 timer 'TLx' serves as 5-bit prescaler
0	1	1	16-bit Timer/counter 'THx' and 'TLx' are cascaded; there is no prescaler.
1	0	2	8-bit auto-reload Timer/counter 'THx' holds a value which is to be reloaded into 'TLx' each time it overflows.
1	1	3	(Timer 0) TL0 is an 8-bit Timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/counter 1 stopped.

Table 17. TCON - Timer/counter control register (address 88H) bit allocation

Bit addressable; reset value: 0000 0000B; reset source(s): any reset.

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 18. TCON - Timer/counter control register (address 88H) bit descriptions

Bit	Symbol	Description
7	TF1	Timer 1 overflow flag. Set by hardware on Timer/counter overflow. Cleared by hardware when the processor vectors to Timer 1 Interrupt routine, or by software.
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/counter 1 on/off.
5	TF0	Timer 0 overflow flag. Set by hardware on Timer/counter overflow. Cleared by hardware when the processor vectors to Timer 0 Interrupt routine, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/counter 0 on/off.
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/low level is detected. Cleared by hardware when the interrupt is processed, or by software.

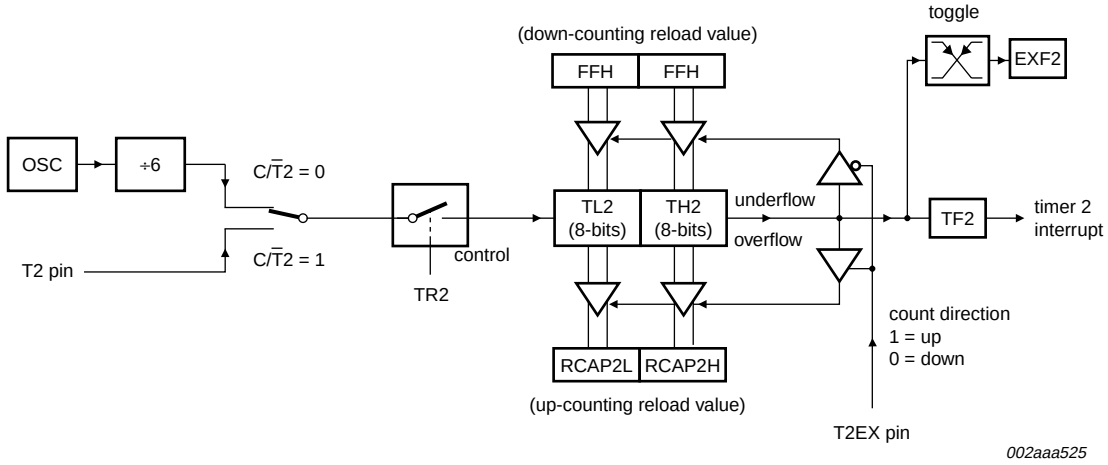


Fig 13. Timer 2 in Auto Reload mode (DCEN = 1)

A logic 0 applied at pin T2EX causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2. The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1.0). This pin, besides being a I/O pin, has two additional functions. It can be programmed:

- To input the external clock for Timer/counter 2, or
- To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the Timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{Oscillator\ Frequency}{2 \times (65536 \angle (RCAP2H, RCAP2L))} \quad (2)$$

Where (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART transmit and receive baud rates to be derived from either Timer 1 or Timer 2 (See Section 6.6 “UART” on page 37 for details). When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When

Table 29. SPCTL - SPI control register (address D5H) bit descriptions *...continued*

Bit	Symbol	Description
2	CPHA	Clock Phase control bit. 1 = shift triggered on the trailing edge of the clock; 0 = shift triggered on the leading edge of the clock.
1	PSC1	SPI Clock Rate Select bit 1. Along with PSC0 controls the SPICLK rate of the device when a master. PSC1 and PSC0 have no effect on the slave. See Table 30.
0	PSC0	SPI Clock Rate Select bit 0. Along with PSC1 controls the SPICLK rate of the device when a master. PSC1 and PSC0 have no effect on the slave. See Table 30.

Table 30. SPCTL - SPI control register (address D5H) clock rate selection

PSC1	PSC0	SPICLK = f_{osc} divided by
0	0	4
0	1	16
1	0	64
1	1	128

Table 31. SPCFG - SPI status register (address AAH) bit allocation

Bit addressable; reset source(s): any reset; reset value: 0000 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIF	WCOL	-	-	-	-	-	-

Table 32. SPCFG - SPI status register (address AAH) bit descriptions

Bit	Symbol	Description
7	SPIF	SPI interrupt flag. Upon completion of data transfer, this bit is set to '1'. If SPIE = 1 and ES = 1, an interrupt is then generated. This bit is cleared by software.
6	WCOL	Write Collision Flag. Set if the SPI data register is written to during data transfer. This bit is cleared by software.
5 to 0	-	Reserved for future use. Should be set to '0' by user programs.

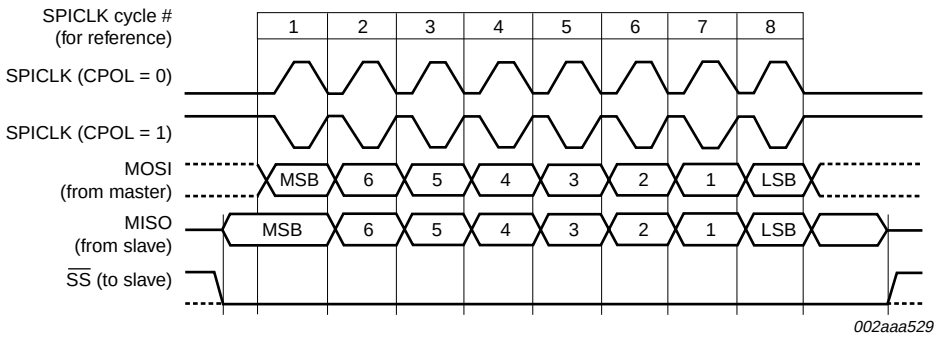


Fig 17. SPI transfer format with CPHA = 0

In the CMOD SFR there are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during Idle mode, WDTE which enables or disables the Watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The watchdog timer function is implemented in module 4 of PCA.

The CCON SFR contains the run control bit (CR) for the PCA and the flags for the PCA timer (CF) and each module (CCF4:0). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software. All the modules share one interrupt vector. The PCA interrupt system is shown in Figure 21.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. The registers contain the bits that control the mode that each module operates in.

The ECCFn bit (from CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on the module) enables the CCFn flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module (see Figure 21).

PWM (CCAPMn.1) enables the pulse width modulation mode.

The TOGn bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.

The match bit MATn (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPNn (CCAPMn.4) and CAPPn (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPPn bit enables the positive edge. If both bits are set, both edges will be enabled and a capture will occur for either transition.

The last bit in the register ECOMn (CCAPMn.6) when set enables the comparator function.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

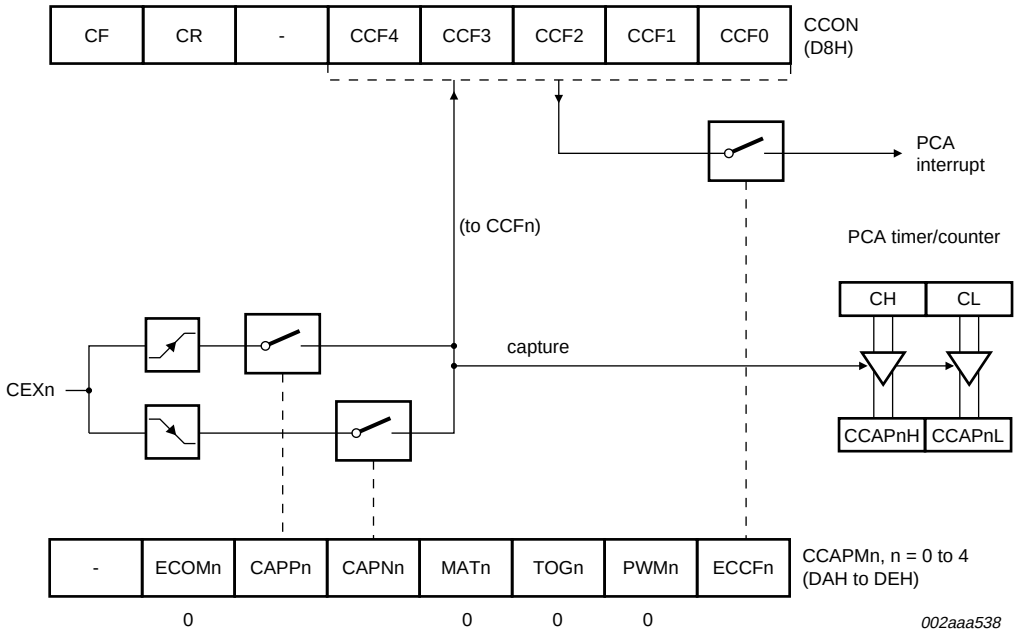


Fig 22. PCA capture mode

If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated.

6.9.2 16-bit software timer mode

The PCA modules can be used as software timers (Figure 23) by setting both the ECOMn and MATn bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

6.10 Security bit

The Security Bit protects against software piracy and prevents the contents of the flash from being read by unauthorized parties in Parallel Programmer mode. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory.

When the Security Bit is activated, all parallel programming commands except for Chip-Erase are ignored (thus the device cannot be read). However, ISP reading, writing, or erasing of the user's code can still be performed if the serial number and length has not been programmed. **Therefore, when a user requests to program the Security Bit, the programmer should prompt the user and program a serial number into the device.**

6.11 Interrupt priority and polling sequence

The device supports eight interrupt sources under a four level priority scheme. Table 43 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. (See Figure 26).

Table 43. Interrupt polling sequence

Description	Interrupt flag	Vector address	Interrupt enable bit	Interrupt priority bit	Service priority	Wake-up power-down
External interrupt 0	IE0	0003H	EX0	PX0/H	1 (highest)	yes
Brownout	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
External interrupt 1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	7	no
T2	TF2, EXF2	002BH	ET2	PT2/H	8	no

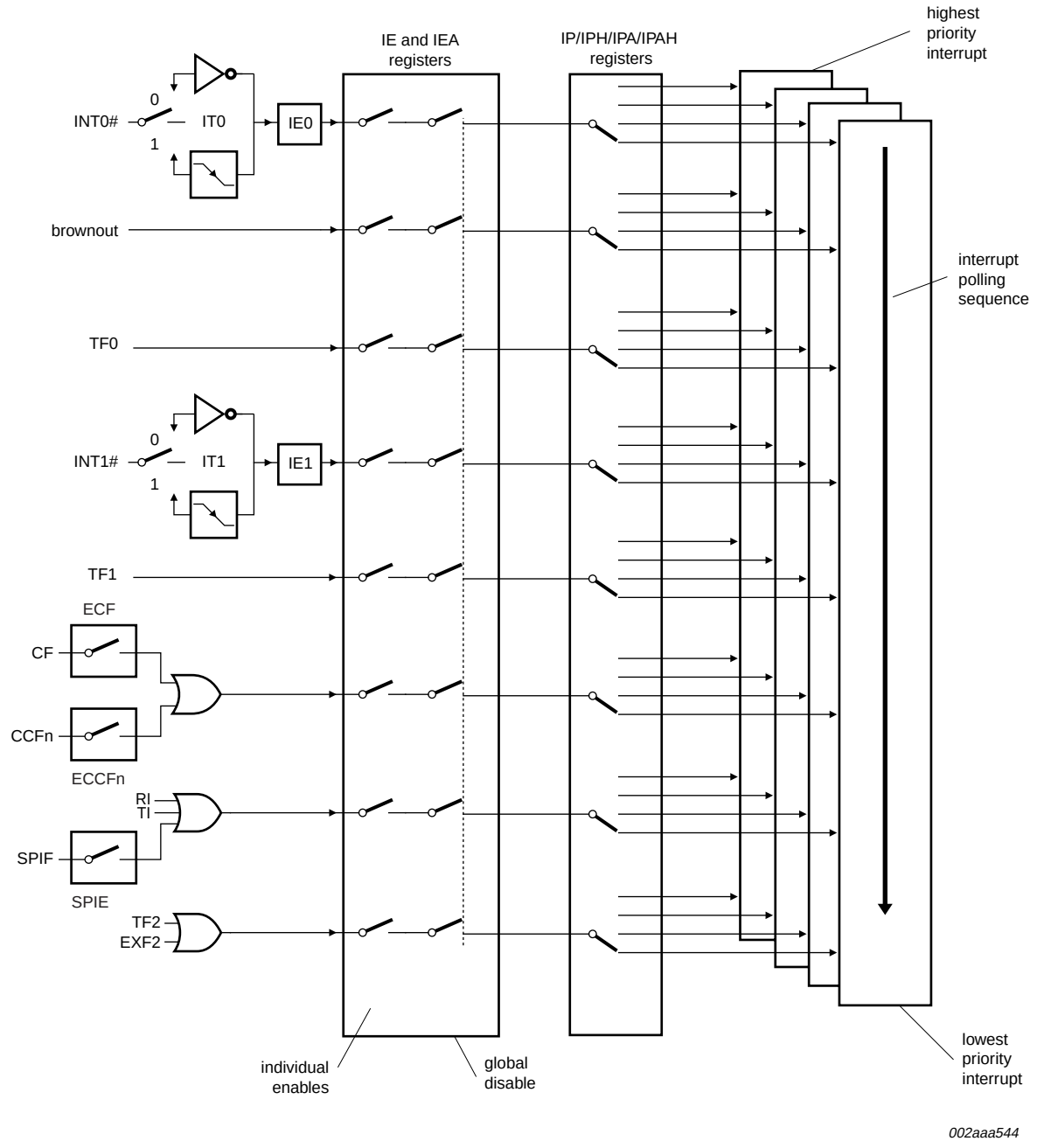


Fig 26. Interrupt structure

Table 44. IEN0 - Interrupt enable register 0 (address A8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Table 51. IP0H - Interrupt priority 0 high register (address B7H) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	PPCH	PCA interrupt priority HIGH bit.
5	PT2H	Timer 2 interrupt priority HIGH bit.
4	PSH	Serial Port interrupt priority HIGH bit.
3	PT1H	Timer 1 interrupt priority HIGH bit.
2	PX1H	External interrupt 1 priority HIGH bit.
1	PT0H	Timer 0 interrupt priority HIGH bit.
0	PX0H	External interrupt 0 priority HIGH bit.

Table 52. IP1 - Interrupt priority 1 register (address F8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	PBO	-	-	-	-

Table 53. IP1 - Interrupt priority 1 register (address F8H) bit descriptions

Bit	Symbol	Description
7 to 5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	PBO	Brownout interrupt priority bit.
3 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

Table 54. IP1H - Interrupt priority 1 high register (address F7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	PBOH	-	-	-	-

Table 55. IP1H - Interrupt priority 1 high register (address F7H) bit descriptions

Bit	Symbol	Description
7 to 5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	PBOH	Brownout interrupt priority bit.
3 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

6.12 Power-saving modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are Idle and Power-down, see Table 56.

6.12.1 Idle mode

Idle mode is entered by setting the IDL bit in the PCON register. In Idle mode, the Program Counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits Idle mode through either a system interrupt or a hardware reset. When exiting Idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits Idle mode. After exiting the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the Idle mode. A hardware reset starts the device similar to a power-on reset.

6.12.2 Power-down mode

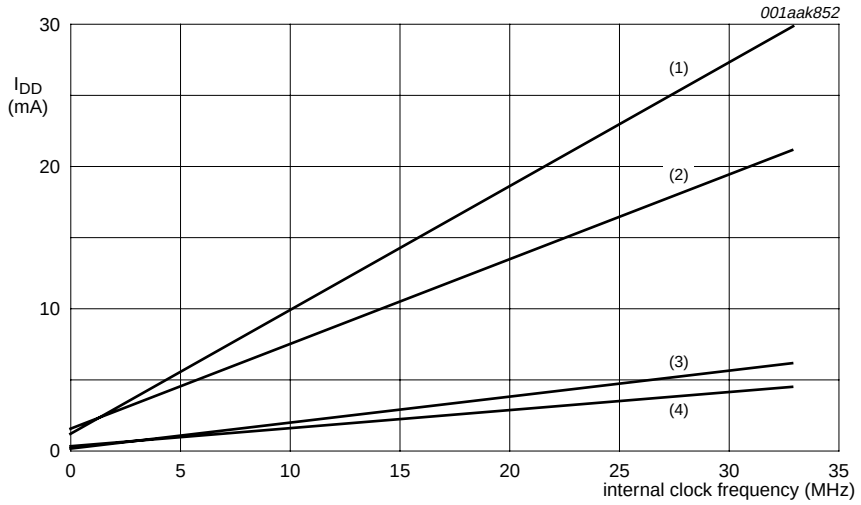
The Power-down mode is entered by setting the PD bit in the PCON register. In the Power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during Power-down mode, and the minimum V_{DD} level is 2.0 V.

The device exits Power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits Power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal restored to logic V_{IH}, the interrupt service routine program execution resumes beginning at the instruction immediately following the instruction which invoked Power-down mode. A hardware reset starts the device similar to power-on reset.

To exit properly out of Power-down mode, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

Table 56. Power-saving modes

Mode	Initiated by	State of MCU	Exited by
Idle mode	Software (Set IDL bit in PCON) MOV PCON, #01H	Clock is running. Interrupts, serial port and timers/counters are active. Program Counter is stopped. ALE and $\overline{PSEN}$ signals are HIGH level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, after the ISR (Interrupt Service Routine) RETI (Return from Interrupt) instruction, program resumes execution beginning at the instruction following the one that invoked Idle mode. A user could consider placing two or three NOP (No Operation) instructions after the instruction that invokes Idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power-down mode	Software (Set PD bit in PCON) MOV PCON, #02H	Clock is stopped. On-chip SRAM and SFR data is maintained. ALE and $\overline{PSEN}$ signals are LOW level during power-down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits Power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Power-down mode. A user could consider placing two or three NOP instructions after the instruction that invokes Power-down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.



(1) Maximum $I_{DD(oper)}$

(2) Maximum $I_{DD(idle)}$

(3) Typical $I_{DD(oper)}$

(4) Typical $I_{DD(idle)}$

Fig 28. Supply current versus frequency

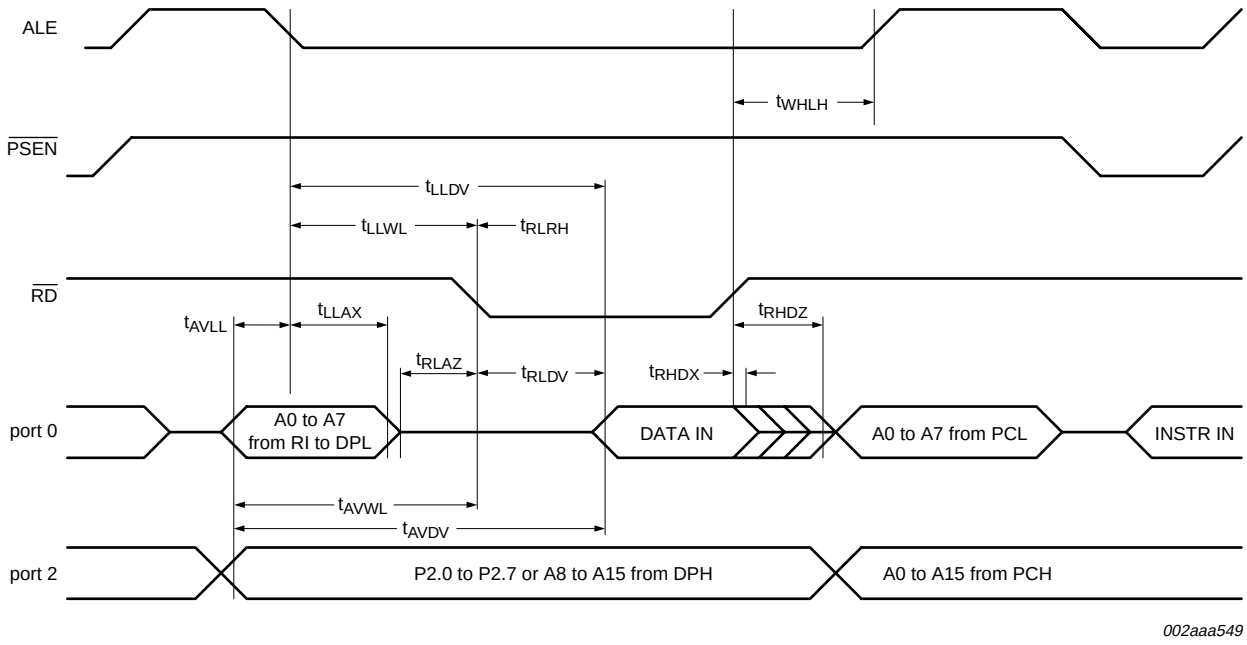


Fig 30. External data memory read cycle

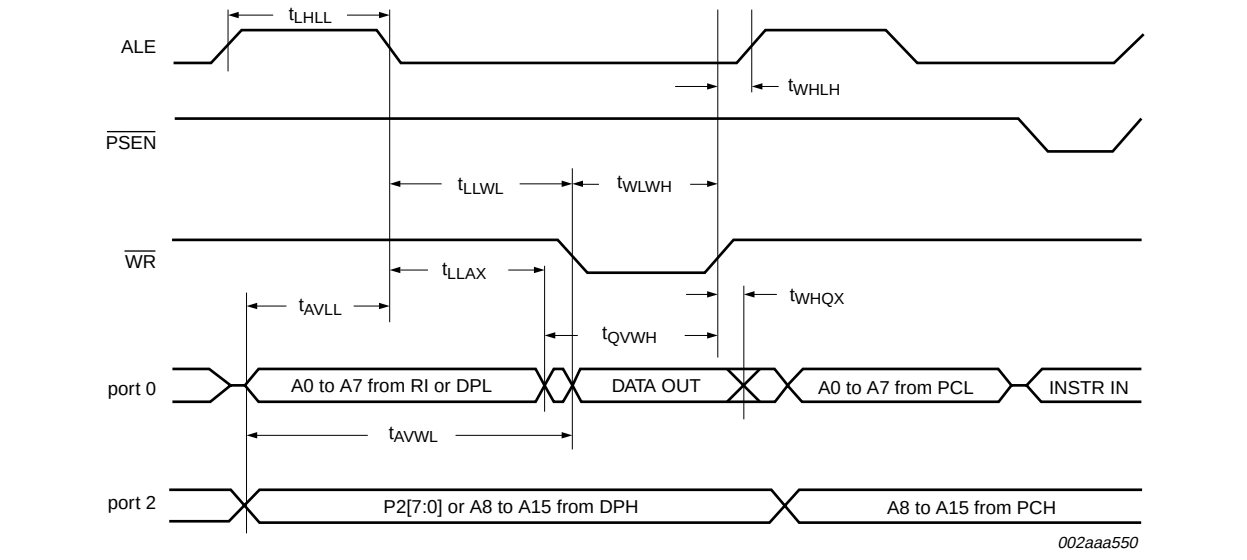


Fig 31. External data memory write cycle

Table 64. External clock drive

Symbol	Parameter	Oscillator				Unit
		12 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	33	MHz
$T_{cy(clk)}$	clock cycle time	83	-	-	-	ns
t_{CHCX}	clock HIGH time	-	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	-	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	20	-	-	ns
t_{CHCL}	clock fall time	-	20	-	-	ns

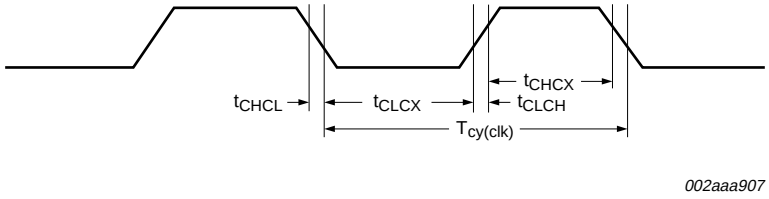


Fig 32. External clock drive waveform

Table 65. Serial port timing

Symbol	Parameter	Oscillator				Unit
		12 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	1.0	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	700	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	50	-	$2T_{cy(clk)} - 50$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	700	-	$10T_{cy(clk)} - 133$	ns

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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