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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lv51rc2bn-112

Table 4. Special function registers ...continued

* Indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses							
			MSB				LSB			
FST	Flash Status Register	B6	-	SB	-	-	EDC	-	-	-
		Bit address	AF	AE	AD	AC	AB	AA	A9	A8
IEN0*	Interrupt Enable 0	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8
IEN1*	Interrupt Enable 1	E8H	-	-	-	-	EBO	-	-	-
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8
IP0*	Interrupt Priority	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0
IP0H	Interrupt Priority 0 HIGH	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8
IP1*	Interrupt Priority 1	F8H	-	-	-	PBO	-	-	-	-
IP1H	Interrupt Priority 1 HIGH	F7H	-	-	-	PBOH	-	-	-	-
FCF		B1H	-	-	-	-	-	-	SWR	BSEL
		Bit address	87	86	85	84	83	82	81	80
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Bit address	97	96	95	94	93	92	91	90
P1*	Port 1	90H	CEX4/ SPICLK	CEX3/ MISO	CEX2/ MOSI	CEX1/ \overline{SS}	CEX0	ECI	T2EX	T2
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0
P3*	Port 3	B0H	\overline{RD}	\overline{WR}	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD
PCON	Power Control Register	87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P
RCAP2H	Timer2 Capture HIGH	CBH								
RCAP2L	Timer2 Capture LOW	CAH								
		Bit address	9F	9E	9D	9C	9B	9A	99	98
SCON*	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	Serial Port Data Buffer Register	99H								

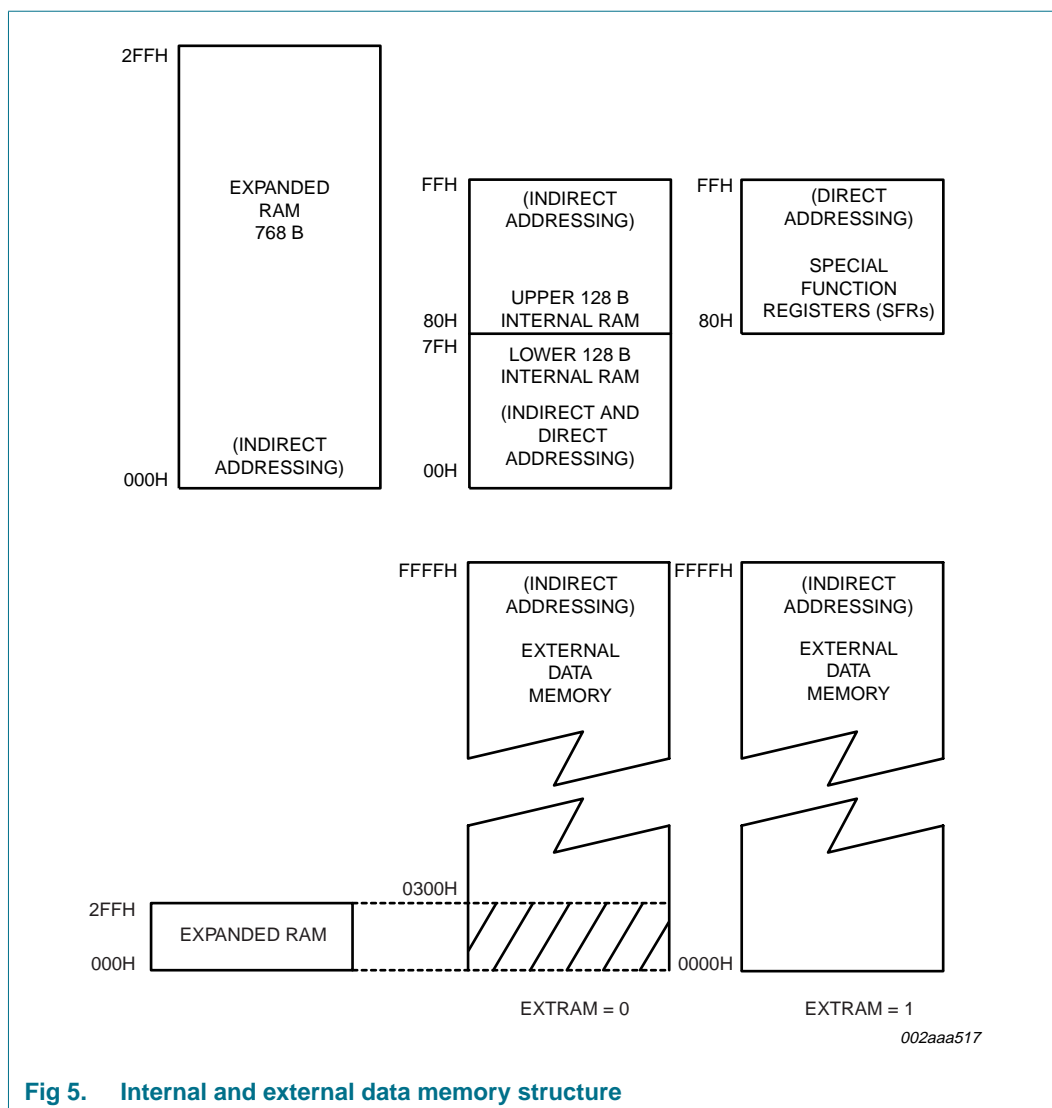


Fig 5. Internal and external data memory structure

6.2.8 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1 (see [Figure 6](#)).

Table 12. ISP hex record formats ...continued

Record type	Command/data function
09	Write serial number :nnxxx09ss..sscc Where: xxxxxx = required field but value is a 'don't care' 09 = write serial number function ss..ss = serial number contents cc = checksum Example: :03000009010203EE (write serial number = 010203)
0A	Display serial number :xxxxxx0Acc Where: xxxxxx = required field but value is a 'don't care' 0A = display serial number function cc = checksum Example: :0000000AF6
0B	Reset and run user code :xxxxxx0Bcc Where: xxxxxx = required field but value is a 'don't care' 0B = reset and run user code cc = checksum Example: :0000000BF5

6.3.5 Using the serial number

This device has the option of storing a 31 B serial number along with the length of the serial number (for a total of 32 B) in a non-volatile memory space. When ISP mode is entered, the serial number length is evaluated to determine if the serial number is in use. If the length of the serial number is programmed to either 00H or FFH, the serial number is considered not in use. If the serial number is in use, reading, programming, or erasing of the user code memory or the serial number is blocked until the user transmits a 'verify serial number' record containing a serial number and length that matches the serial number and length previously stored in the device. The user can reset the serial number to all zeros and set the length to zero by sending the 'reset serial number' record. In addition, the 'reset serial number' record will also erase all user code.

6.3.6 IAP method

Several IAP calls are available for use by an application program to permit selective erasing, reading and programming of flash sectors, security bit, configuration bytes, and device id. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at 1FF0H. The IAP calls are shown in [Table 13](#).

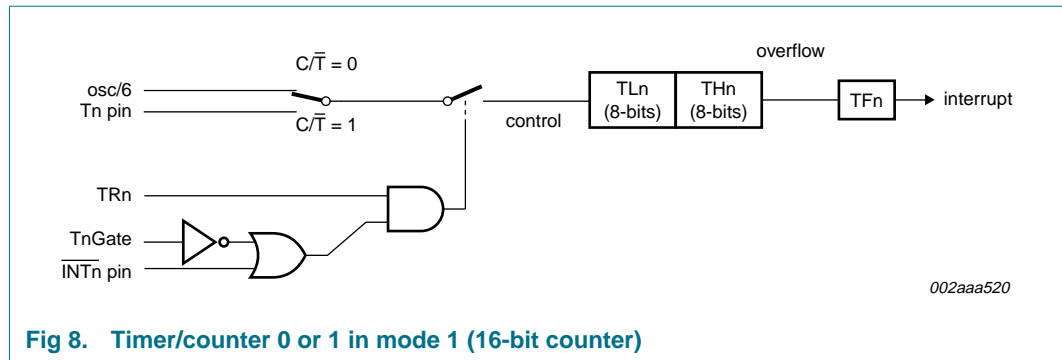


Fig 8. Timer/counter 0 or 1 in mode 1 (16-bit counter)

6.4.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 9. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

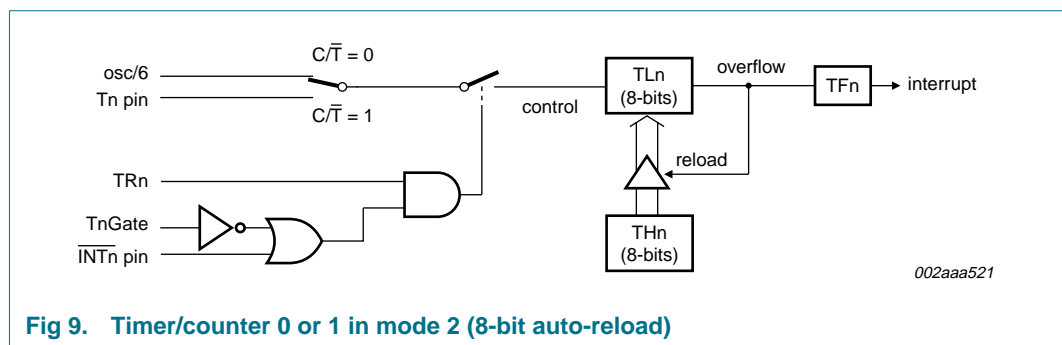


Fig 9. Timer/counter 0 or 1 in mode 2 (8-bit auto-reload)

6.4.4 Mode 3

When timer 1 is in mode 3 it is stopped (holds its count). The effect is the same as setting TR1 = 0.

Timer 0 in mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for mode 3 and Timer 0 is shown in Figure 10. TL0 uses the Timer 0 control bits: T0C/T-bar, T0GATE, TR0, INT0-bar, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the 'Timer 1' interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in mode 3, the P89LV51RB2/RC2/RD2 can look like it has an additional Timer.

Note: When Timer 0 is in mode 3, Timer 1 can be turned on and off by switching it into and out of its own mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

Table 21. T2CON - Timer/counter 2 control register (address C8H) bit descriptions

Bit	Symbol	Description
4	TCLK	Transmit clock flag. When set, causes the UART to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	Start/stop control for Timer 2. A logic '1' enables the timer to run.
1	C/ \bar{T} 2	Timer or counter select. (Timer 2) 0 = internal timer ($f_{osc} / 6$) 1 = external event counter (falling edge triggered; external clock's maximum rate = $f_{osc} / 12$)
0	CP/ \bar{R} L2	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 22. T2MOD - Timer 2 mode control register (address C9H) bit allocation

Not bit addressable; Reset value: XX00 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T2OE	DCEN

Table 23. T2MOD - Timer 2 mode control register (address C9H) bit descriptions

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to '0' by user programs.
1	T2OE	Timer 2 Output Enable bit. Used in programmable clock-out mode only.
0	DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

6.5.1 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter (as selected by C/ \bar{T} 2 in T2CON) which upon overflowing sets bit TF2, the Timer 2 overflow bit.

The capture mode is illustrated in [Figure 11](#).

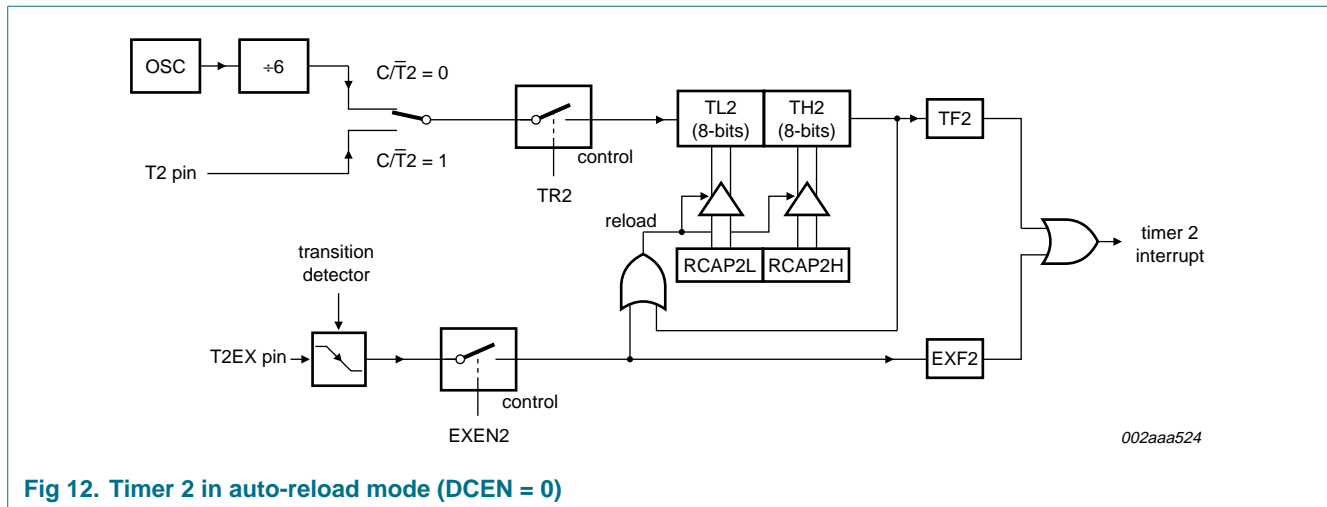


Fig 12. Timer 2 in auto-reload mode (DCEN = 0)

In this mode, there are two options selected by bit EXEN2 in T2CON register. If EXEN2 = 0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

Auto reload frequency when Timer 2 is counting up can be determined from this formula:

$$\frac{\text{Supply Frequency}}{(65536 \angle (RCAP2H, RCAP2L))} \quad (1)$$

Where Supply frequency is either f_{osc} ($C/\overline{T}2 = 0$) or frequency of signal on T2 pin ($C/\overline{T}2 = 1$).

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 is '1'.

Microcontroller's hardware will need three consecutive machine cycles in order to recognize the falling edge on T2EX and to set EXF2 = 1: in the first machine cycle pin T2EX has to be sampled as '1'; in the second machine cycle it has to be sampled as '0', and in the third machine cycle EXF2 will be set to '1'.

In [Figure 13](#), DCEN = 1 and Timer 2 is enabled to count up or down. This mode allows pin T2EX to control the direction of count. When a logic '1' is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and sets the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

TCLK = 1, Timer 2 is used as the UART transmit baud rate generator. RCLK has the same effect for the UART receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – Timer 1 or Timer 2.

Figure 14 shows Timer 2 in baud rate generator mode.

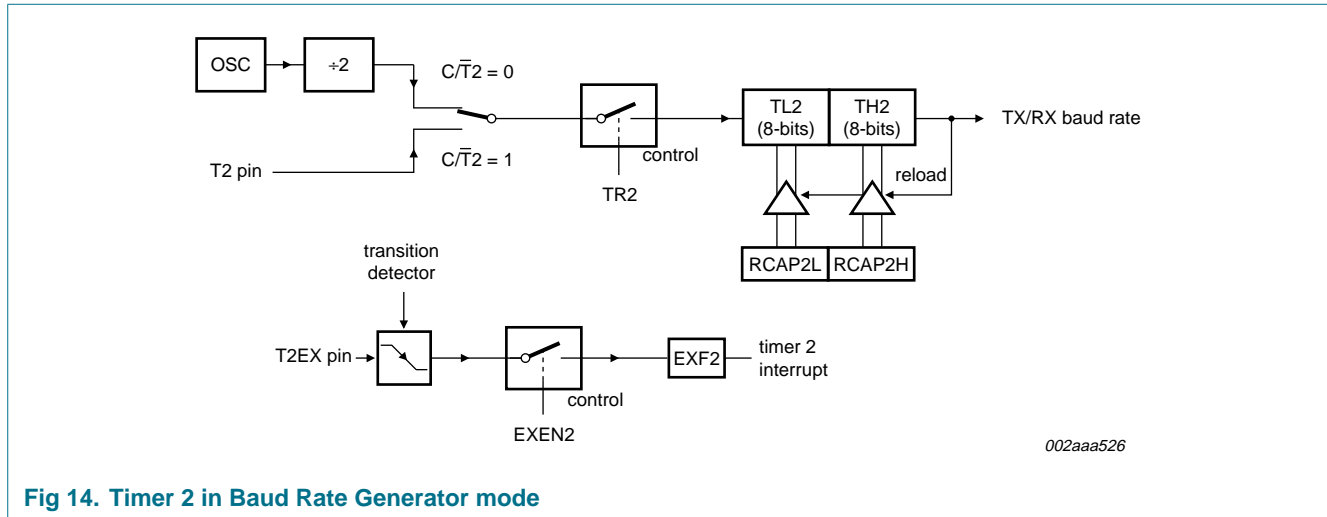


Fig 14. Timer 2 in Baud Rate Generator mode

The baud rate generation mode is like the auto-reload mode, when a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 baud rates} = \text{Timer 2 Overflow Rate} / 16$$

The timer can be configured for either 'timer' or 'counter' operation. In many applications, it is configured for 'timer' operation ($C/\overline{T}2 = 0$). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., $1/6$ the oscillator frequency). As a baud rate generator, it increments at the oscillator frequency. Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 baud rates} =$$

$$\frac{\text{Oscillator Frequency}}{(16 \times (65536 - (RCAP2H, RCAP2L)))} \quad (3)$$

Where: (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will

Table 26. SCON - Serial port control register (address 98H) bit descriptions ...continued

Bit	Symbol	Description
2	RB8	In modes 2 and 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is undefined.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or approximately halfway through the stop bit time in all other modes. (See SM2 for exceptions). Must be cleared by software.

Table 27. SCON - Serial port control register (address 98H) SM0/SM1 mode definitions

SM0, SM1	UART mode	Baud rate
0 0	0: shift register	CPU clock / 6
0 1	1: 8-bit UART	variable
1 0	2: 9-bit UART	CPU clock / 32 or CPU clock / 16
1 1	3: 9-bit UART	variable

6.6.5 Framing error

Framing error (FE) is reported in the SCON.7 bit if SMOD0 (PCON.6) = 1. If SMOD0 = 0, SCON.7 is the SM0 bit for the UART, it is recommended that SM0 is set up before SMOD0 is set to '1'.

6.6.6 More about UART mode 1

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset to align its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated.

6.6.7 More about UART modes 2 and 3

Reception is performed in the same manner as in mode 1.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF.

6.6.8 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed so that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in a way that the 9th bit is '1' in an address byte and '0' in the data byte. With SM2 = 1, no slave will be interrupted by a data byte, i.e. the received 9th bit is '0'. However, an address byte having the 9th bit set to '1' will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed or not. The addressed slave will clear its SM2 bit and prepare to receive the data (still 9 bits long) that follow. The slaves that weren't being addressed leave their SM2 bits set and ignore the subsequent data bytes.

SM2 has no effect in mode 0, and in mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. When the UART receives data in mode 1 and SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.6.9 Automatic address recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled for the UART by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the 'Given' address or the 'Broadcast' address. The 9 bit mode requires that the 9th information bit is a '1' to indicate that the received information is an address and not data.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two Special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are 'don't care'. The SADEN mask can be logically ANDed with the SADDR to create the 'Given' address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others.

This device uses the methods presented in [Figure 15](#) to determine if a 'Given' or 'Broadcast' address has been received or not.

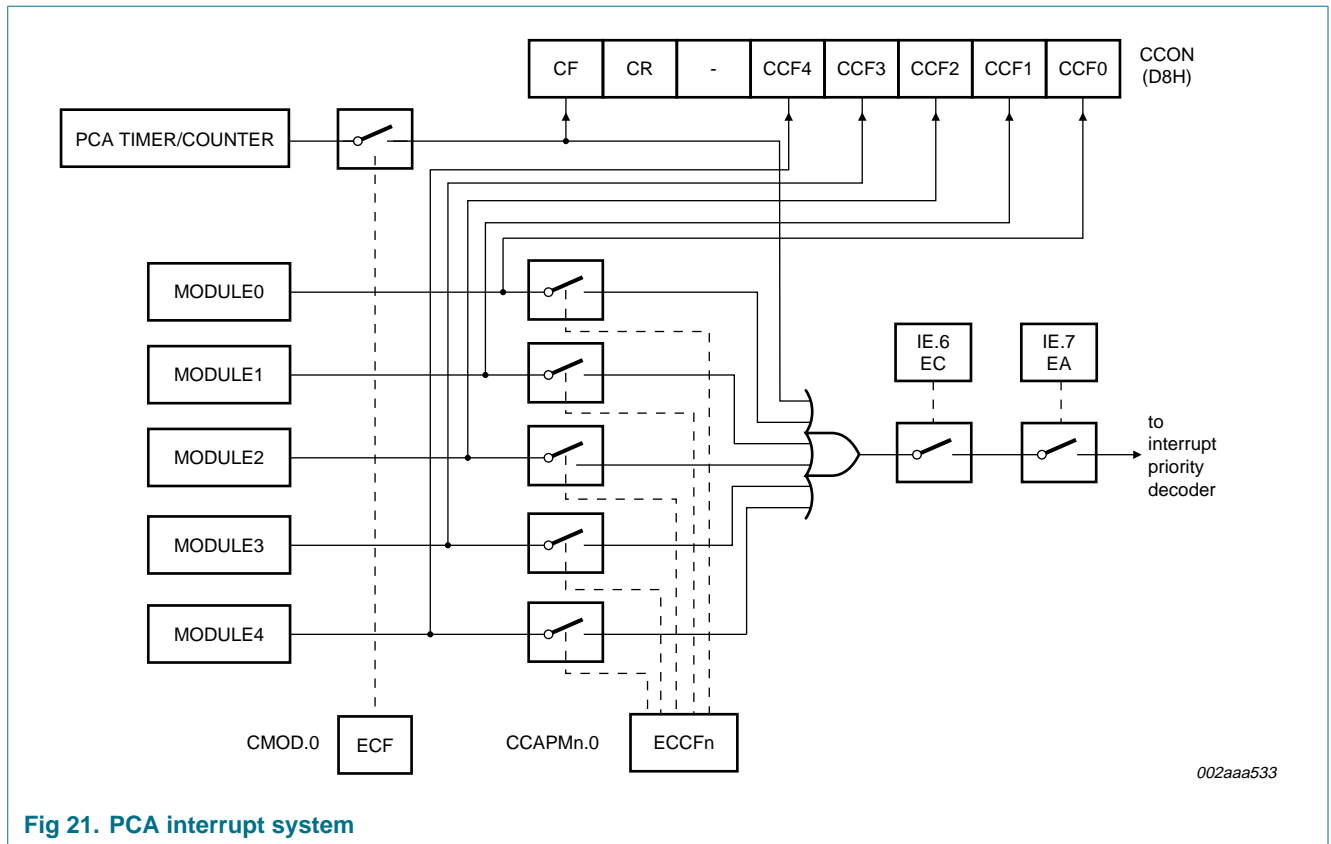


Fig 21. PCA interrupt system

Table 35. CMOD - PCA counter mode register (address D9H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Table 36. CMOD - PCA counter mode register (address D9H) bit descriptions

Bit	Symbol	Description
7	CIDL	Counter Idle Control: CIDL = 0 programs the PCA Counter to continue functioning during Idle mode. CIDL = 1 programs it to be gated off during idle.
6	WDTE	Watchdog Timer Enable: WDTE = 0 disables watchdog timer function on module 4. WDTE = 1 enables it.
5 to 3	-	Reserved for future use. Should be set to '0' by user programs.
2 to 1	CPS1, CPS0	PCA Count Pulse Select (see Table 37 below).
0	ECF	PCA Enable Counter Overflow Interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function.

Table 37. CMOD - PCA counter mode register (address D9H) count pulse select

CPS1	CPS0	Select PCA input
0	0	0 Internal clock, $f_{osc} / 6$
0	1	1 Internal clock, $f_{osc} / 2$
1	0	2 Timer 0 overflow
1	1	3 External clock at ECI/P1.2 pin (maximum rate = $f_{osc} / 4$)

Table 38. CCON - PCA counter control register (address 0D8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Table 39. CCON - PCA counter control register (address 0D8H) bit descriptions

Bit	Symbol	Description
7	CF	PCA Counter Overflow Flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
6	CR	PCA Counter Run Control Bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
5	-	Reserved for future use. Should be set to '0' by user programs.
4	CCF4	PCA Module 4 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
3	CCF3	PCA Module 3 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
2	CCF2	PCA Module 2 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
1	CCF1	PCA Module 1 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
0	CCF0	PCA Module 0 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.

Table 40. CCAPMn - PCA modules compare/capture register (address CCAPM0: 0DAH, CCAPM1: 0DBH, CCAPM2: 0DCH, CCAPM3: 0DDH, CCAPM4: 0DEH) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Table 41. CCAPMn - PCA modules compare/capture register (address CCAPM0: 0DAH, CCAPM1: 0DBH, CCAPM2: 0DCH, CCAPM3: 0DDH, CCAPM4: 0DEH) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to '0' by user programs.
6	ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
5	CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
4	CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.

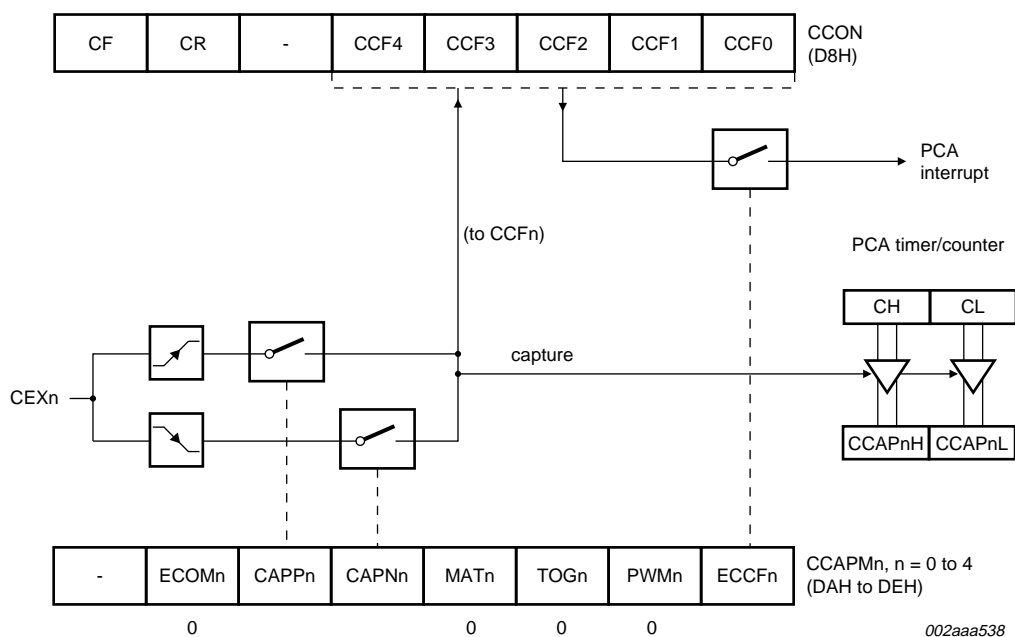


Fig 22. PCA capture mode

If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated.

6.9.2 16-bit software timer mode

The PCA modules can be used as software timers ([Figure 23](#)) by setting both the ECOMn and MATn bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

Table 58. Clock doubling features

Device	Standard mode (X1)		Clock double mode (X2)	
	Clocks per machine cycle	Maximum external clock frequency (MHz)	Clocks per machine cycle	Maximum external clock frequency (MHz)
P89LV51RB2/RC2/RD2	12	33	6	16

Table 59. FST - Flash status register (address B6) bit allocation

Not Bit addressable; reset value: xxxx x0xxB.

Bit	7	6	5	4	3	2	1	0
Symbol	-	SB	-	-	EDC	-	-	-

Table 60. FST - Flash status register (address B6) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to '0' by user programs.
6	SB	Security bit.
5 to 4	-	Reserved for future use. Should be set to '0' by user programs.
3	EDC	Enable double clock.
2 to 0	-	Reserved for future use. Should be set to '0' by user programs.

7. Limiting values

Table 61. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

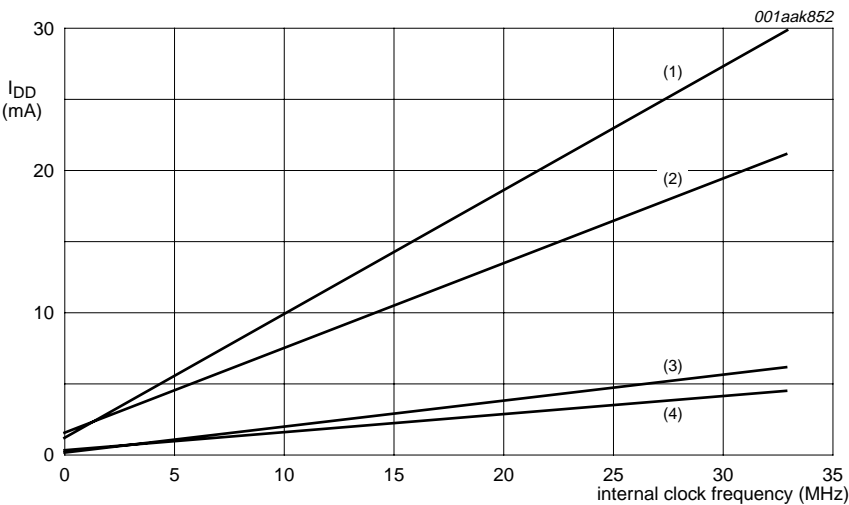
Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		-55	+125	°C
T_{stg}	storage temperature		-65	+150	°C
V_I	input voltage	on \overline{EA} pin to V_{SS}	-0.5	+14	V
V_n	voltage on any other pin	except V_{SS} ; with respect to V_{DD}	-0.5	$V_{DD} + 0.5$	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin	pins P1.5, P1.6, P1.7	-	20	mA
		all other pins	-	15	mA
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 62. Static characteristics

$T_{amb} = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ or $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD} = 2.7\text{ V}$ to 3.6 V ; $V_{SS} = 0\text{ V}$.

Symbol	Parameter	Conditions	Min	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1] 10000	-	cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1] 100	-	years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1] $100 + I_{DD}$	-	mA
V_{IL}	LOW-level input voltage	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-0.5	+0.7	V
V_{IH}	HIGH-level input voltage	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	$0.2V_{DD} + 0.9$	$V_{DD} + 0.5$	V
		XTAL1, RST	$0.7V_{DD}$	$V_{DD} + 0.5$	V
V_{OL}	LOW-level output voltage	$V_{DD} = 2.7\text{ V}$; ports 1.5, 1.6, 1.7			
		$I_{OL} = 16\text{ mA}$	-	1.0	V
		$V_{DD} = 2.7\text{ V}$; ports 1, 2, 3, except PSEN, ALE	[2][3][4]		
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.3	V
		$I_{OL} = 1.6\text{ mA}$	-	0.45	V
		$I_{OL} = 3.5\text{ mA}$	-	1.0	V
		$V_{DD} = 2.7\text{ V}$; port 0, PSEN, ALE			
		$I_{OL} = 200\text{ }\mu\text{A}$	-	0.3	V
		$I_{OL} = 3.2\text{ mA}$	-	0.45	V



- (1) Maximum $I_{DD(oper)}$
- (2) Maximum $I_{DD(idle)}$
- (3) Typical $I_{DD(oper)}$
- (4) Typical $I_{DD(idle)}$

Fig 28. Supply current versus frequency

9. Dynamic characteristics

Table 63. Dynamic characteristics

Over operating conditions: load capacitance for Port 0, ALE, and $\overline{\text{PSEN}} = 100 \text{ pF}$; load capacitance for all other outputs = 80 pF ; $T_{\text{amb}} = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -40°C to $+85^\circ\text{C}$; $V_{\text{DD}} = 2.7 \text{ V}$ to 3.6 V at 33 MHz ; $V_{\text{SS}} = 0 \text{ V}$. [1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	X1 mode	0	-	33	MHz
		X2 mode	0	-	16	MHz
		IAP	0.25	-	33	MHz
t_{LHLL}	ALE pulse width		$2T_{\text{cy}(\text{clk})} - 15$	-	-	ns
t_{AVLL}	address valid to ALE LOW time		$T_{\text{cy}(\text{clk})} - 25$	-	-	ns
t_{LLAX}	address hold after ALE LOW time		$T_{\text{cy}(\text{clk})} - 25$	-	-	ns
t_{LLIV}	ALE LOW to valid instruction in time		-	-	$4T_{\text{cy}(\text{clk})} - 65$	ns
t_{LLPL}	ALE LOW to $\overline{\text{PSEN}}$ LOW time		$T_{\text{cy}(\text{clk})} - 25$	-	-	ns
t_{PLPH}	$\overline{\text{PSEN}}$ pulse width		$T_{\text{cy}(\text{clk})} - 25$	-	-	ns
t_{PLIV}	$\overline{\text{PSEN}}$ LOW to valid instruction in time		-	-	$3T_{\text{cy}(\text{clk})} - 55$	ns
t_{PXIX}	input instruction hold after $\overline{\text{PSEN}}$ time		0	-	-	ns
t_{PXIZ}	input instruction float after $\overline{\text{PSEN}}$ time		-	-	$T_{\text{cy}(\text{clk})} - 5$	ns
t_{PXAV}	$\overline{\text{PSEN}}$ to address valid time		$T_{\text{cy}(\text{clk})} - 8$	-	-	ns
t_{AVIV}	address to valid instruction in time		-	-	$5T_{\text{cy}(\text{clk})} - 80$	ns
t_{PLAZ}	$\overline{\text{PSEN}}$ LOW to address float time		-	-	10	ns
t_{RLRH}	$\overline{\text{RD}}$ LOW pulse width		$6T_{\text{cy}(\text{clk})} - 40$	-	-	ns
t_{WLWH}	$\overline{\text{WR}}$ LOW pulse width		$6T_{\text{cy}(\text{clk})} - 40$	-	-	ns
t_{RLDV}	$\overline{\text{RD}}$ LOW to valid data in time		-	-	$5T_{\text{cy}(\text{clk})} - 90$	ns
t_{RHDX}	data hold after $\overline{\text{RD}}$ time		0	-	-	ns
t_{RHDZ}	data float after $\overline{\text{RD}}$ time		-	-	$2T_{\text{cy}(\text{clk})} - 25$	ns
t_{LLDV}	ALE LOW to valid data in time		-	-	$8T_{\text{cy}(\text{clk})} - 90$	ns
t_{AVDV}	address to valid data in time		-	-	$9T_{\text{cy}(\text{clk})} - 90$	ns
t_{LLWL}	ALE LOW to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ LOW time		$3T_{\text{cy}(\text{clk})} - 25$	-	$3T_{\text{cy}(\text{clk})} + 25$	ns
t_{AVWL}	address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ LOW time		$4T_{\text{cy}(\text{clk})} - 75$	-	-	ns
t_{WHQX}	data hold after $\overline{\text{WR}}$ time		$T_{\text{cy}(\text{clk})} - 27$	-	-	ns
t_{QVWH}	data output valid to $\overline{\text{WR}}$ HIGH time		$7T_{\text{cy}(\text{clk})} - 70$	-	-	ns
t_{RLAZ}	$\overline{\text{RD}}$ LOW to address float time		-	-	0	ns
t_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ HIGH to ALE HIGH time		$T_{\text{cy}(\text{clk})} - 25$	-	$T_{\text{cy}(\text{clk})} + 25$	ns

[1] $T_{\text{cy}(\text{clk})} = 1 / f_{\text{osc}}$.

[2] Calculated values are for 6-clock mode only.

9.1 Explanation of symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The characters are described below:

- A** — Address
- C** — Clock
- D** — Input data
- H** — Logic level HIGH
- I** — Instruction (program memory contents)
- L** — Logic level LOW or ALE
- P** — $\overline{\text{PSEN}}$
- Q** — Output data
- R** — $\overline{\text{RD}}$ signal
- T** — Time
- V** — Valid
- W** — $\overline{\text{WR}}$ signal
- X** — No longer a valid logic level
- Z** — High impedance (Float)

Example:

t_{AVLL} = Address valid to ALE LOW time

t_{LLPL} = ALE LOW to $\overline{\text{PSEN}}$ LOW time

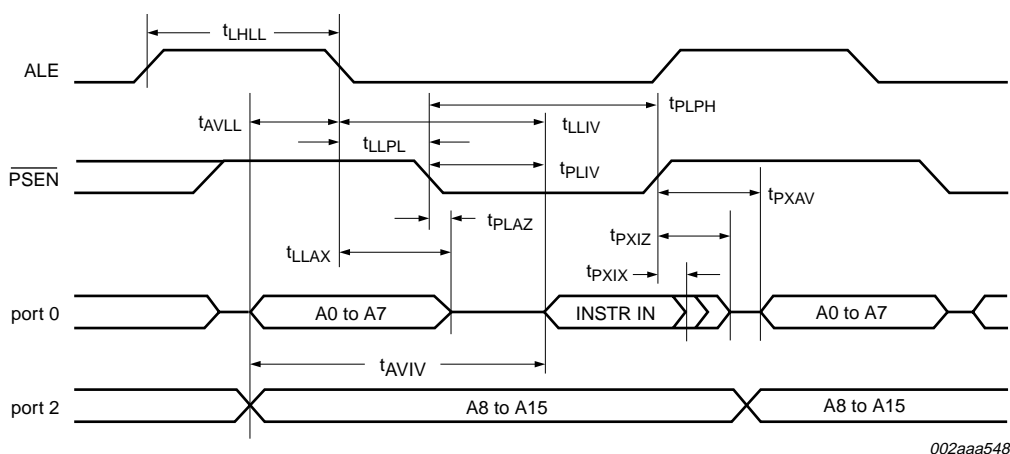


Fig 29. External program memory read cycle

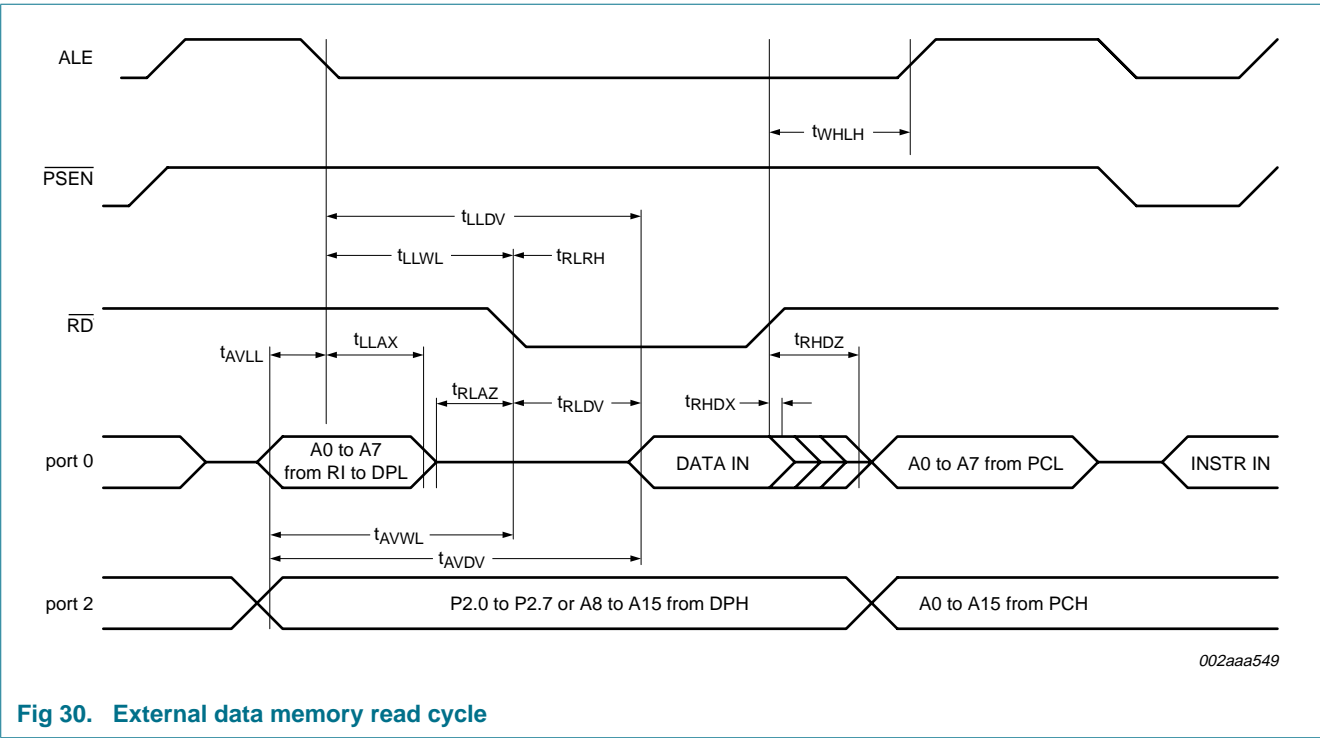


Fig 30. External data memory read cycle

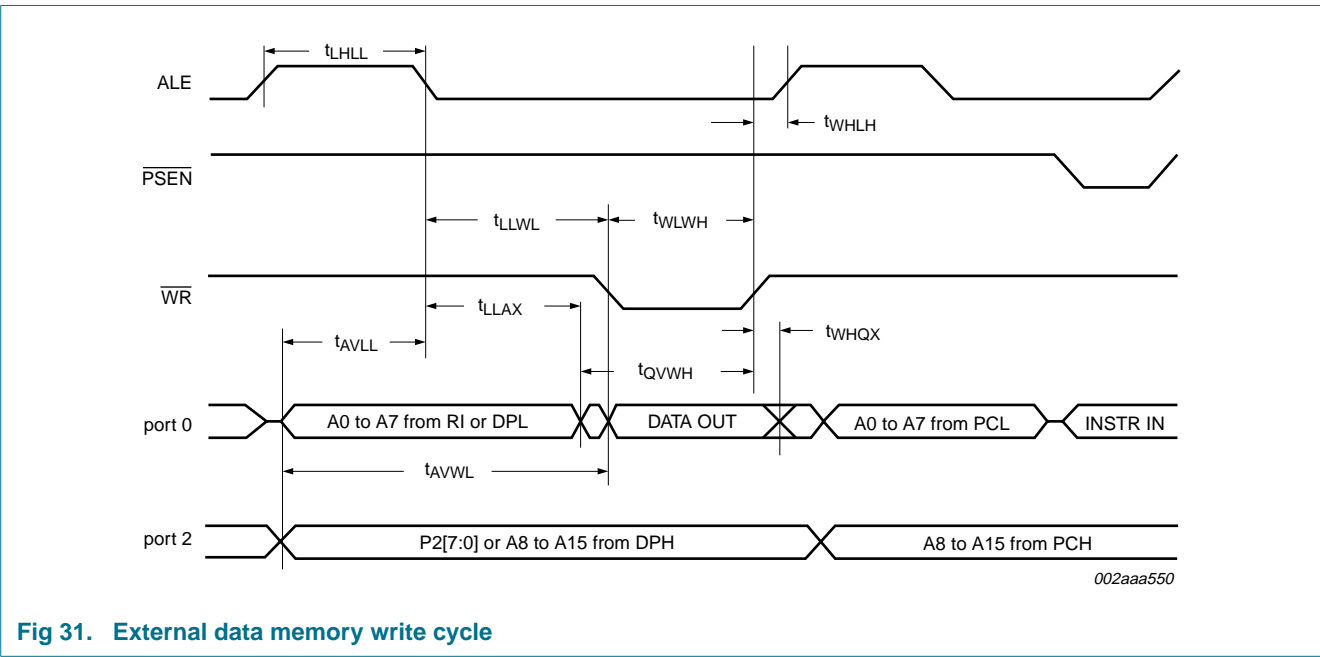
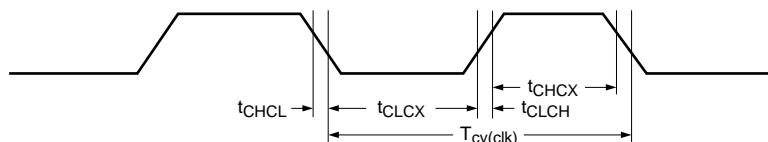


Fig 31. External data memory write cycle

Table 64. External clock drive

Symbol	Parameter	Oscillator				Unit
		12 MHz		Variable		
		Min	Max	Min	Max	
f _{osc}	oscillator frequency	-	-	0	33	MHz
T _{cy(clk)}	clock cycle time	83	-	-	-	ns
t _{CHCX}	clock HIGH time	-	-	0.35T _{cy(clk)}	0.65T _{cy(clk)}	ns
t _{CLCX}	clock LOW time	-	-	0.35T _{cy(clk)}	0.65T _{cy(clk)}	ns
t _{CLCH}	clock rise time	-	20	-	-	ns
t _{CHCL}	clock fall time	-	20	-	-	ns



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Fig 32. External clock drive waveform

Table 65. Serial port timing

Symbol	Parameter	Oscillator				Unit
		12 MHz		Variable		
		Min	Max	Min	Max	
T _{XLXL}	serial port clock cycle time	1.0	-	12T _{cy(clk)}	-	μs
t _{QVXH}	output data set-up to clock rising edge time	700	-	10T _{cy(clk)} – 133	-	ns
t _{XHQX}	output data hold after clock rising edge time	50	-	2T _{cy(clk)} – 50	-	ns
t _{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t _{XHDV}	input data valid to clock rising edge time	-	700	-	10T _{cy(clk)} – 133	ns

TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm

SOT376-1

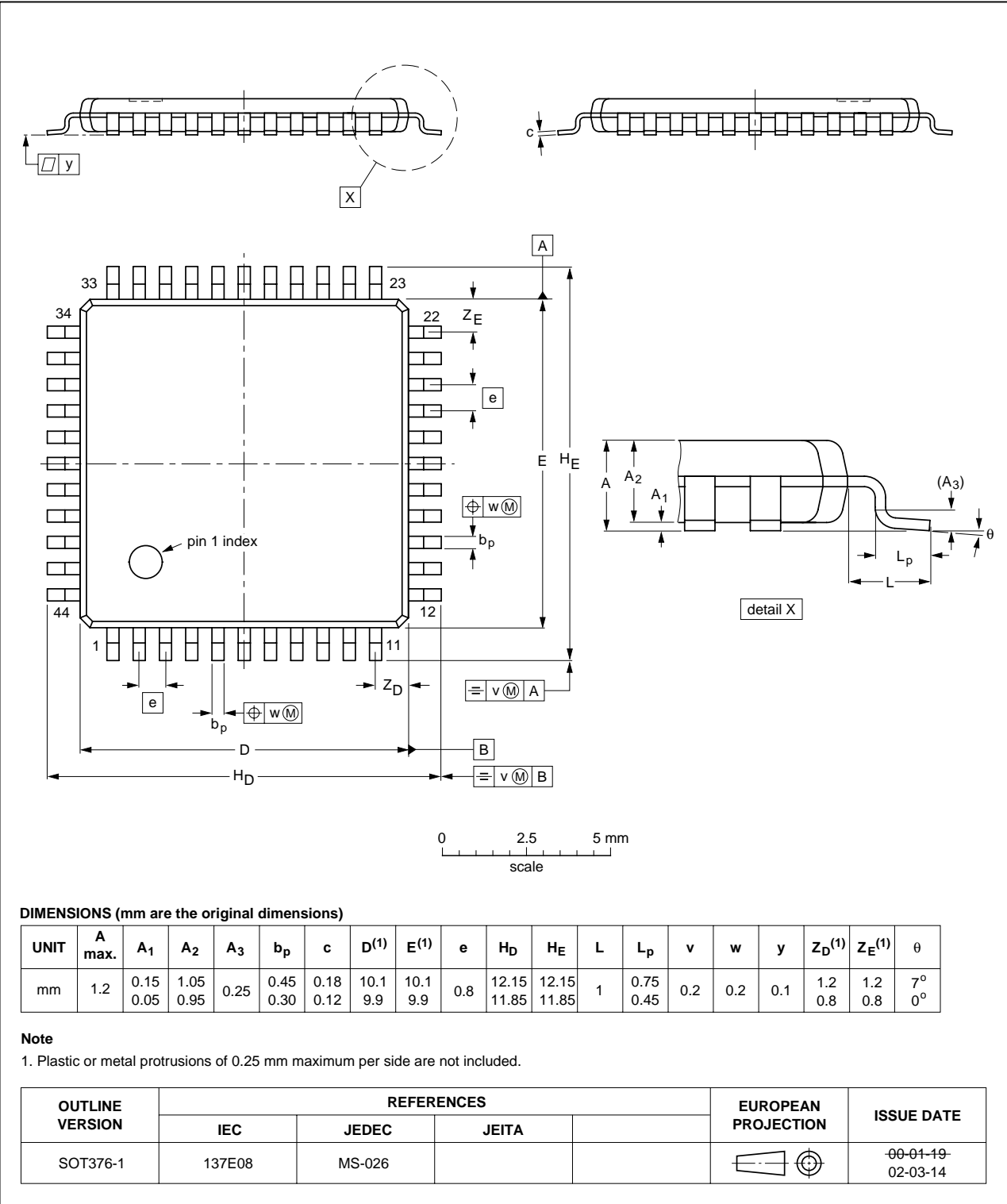


Fig 39. Package outline SOT376-1 (TQFP44)