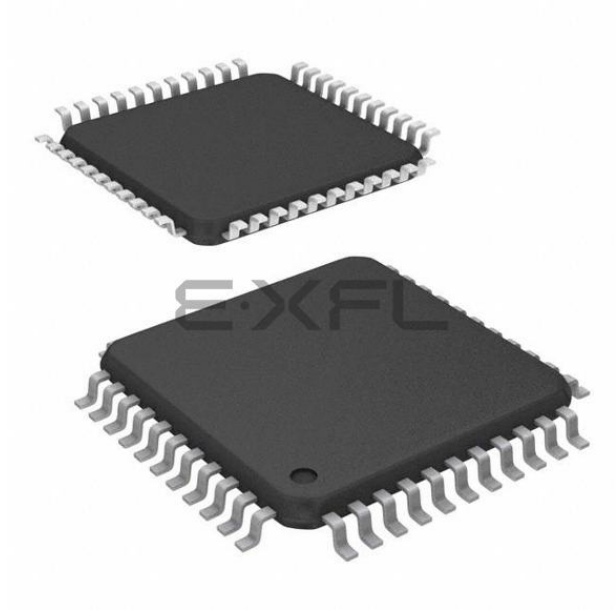

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lv51rd2bbc-557

- Brownout detection
- Low power modes
  - Power-down mode with external interrupt wake-up
  - Idle mode
- PLCC44 and TQFP44 packages

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89LV51RB2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LV51RC2FBC	TQFP44	plastic thin quad flat package; 44 leads; body 10 × 10 × 1.0 mm	SOT376-1
P89LV51RD2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LV51RD2BBC	TQFP44	plastic thin quad flat package; 44 leads; body 10 × 10 × 1.0 mm	SOT376-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LV51RB2BA	16 kB	0 °C to +70 °C	0 MHz to 40 MHz
P89LV51RC2FBC	32 kB	–40 °C to +85 °C	
P89LV51RD2FA	64 kB	–40 °C to +85 °C	
P89LV51RD2BBC	64 kB	0 °C to +70 °C	

Table 3. P89LV51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin		Type	Description
	TQFP44	PLCC44		
ALE/$\overline{PROG}$	27	33	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input ($\overline{PROG}$) for flash programming. Normally the ALE[1] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[2] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if bit AO is set to '1', ALE is disabled.
n.c.	6, 17, 28, 39	1, 12, 23, 34	I/O	not connected
XTAL1	15	21	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	14	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	38	44	I	**Power supply**
V_{SS}	16	22	I	**Ground**

[1] ALE loading issue: When ALE pin experiences higher loading (> 30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to connect a pull-up resistor of 3 kΩ to 50 kΩ from pin ALE to V_{DD}.

[2] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

Table 4. Special function registers

** Indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0
ACC*	Accumulator	E0H								
AUXR	Auxiliary function register	8EH	-	-	-	-	-	-	EXTRAM	AO
AUXR1	Auxiliary function register 1	A2H	-	-	-	-	GF2	0	-	DPS
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0
B*	B register	F0H								
CCAP0H	Module 0 Capture HIGH	FAH								
CCAP1H	Module 1 Capture HIGH	FBH								
CCAP2H	Module 2 Capture HIGH	FCH								
CCAP3H	Module 3 Capture HIGH	FDH								
CCAP4H	Module 4 Capture HIGH	FEH								
CCAP0L	Module 0 Capture LOW	EAH								
CCAP1L	Module 1 Capture LOW	EBH								
CCAP2L	Module 2 Capture LOW	ECH								
CCAP3L	Module 3 Capture LOW	EDH								
CCAP4L	Module 4 Capture LOW	EEH								
CCAPM0	Module 0 Mode	DAH	-	ECOM_0	CAPP_0	CAPN_0	MAT_0	TOG_0	PWM_0	ECCF_0
CCAPM1	Module 1 Mode	DBH	-	ECOM_1	CAPP_1	CAPN_1	MAT_1	TOG_1	PWM_1	ECCF_1
CCAPM2	Module 2 Mode	DCH	-	ECOM_2	CAPP_2	CAPN_2	MAT_2	TOG_2	PWM_2	ECCF_2
CCAPM3	Module 3 Mode	DDH	-	ECOM_3	CAPP_3	CAPN_3	MAT_3	TOG_3	PWM_3	ECCF_3
CCAPM4	Module 4 Mode	DEH	-	ECOM_4	CAPP_4	CAPN_4	MAT_4	TOG_4	PWM_4	ECCF_4
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8
CCON*	PCA Counter Control	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
CH	PCA Counter HIGH	F9H								
CL	PCA Counter LOW	E9H								
CMOD	PCA Counter Mode	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
DPTR	Data Pointer (2 B)									
DPH	Data Pointer HIGH	83H								
DPL	Data Pointer LOW	82H								

Table 4. Special function registers *…continued*

** Indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
FST	Flash Status Register	B6	-	SB	-	-	EDC	-	-	-
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**
IEN0*	Interrupt Enable 0	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**
IEN1*	Interrupt Enable 1	E8H	-	-	-	-	EBO	-	-	-
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**
IP0*	Interrupt Priority	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0
IP0H	Interrupt Priority 0 HIGH	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**
IP1*	Interrupt Priority 1	F8H	-	-	-	PBO	-	-	-	-
IP1H	Interrupt Priority 1 HIGH	F7H	-	-	-	PBOH	-	-	-	-
FCF		B1H	-	-	-	-	-	-	SWR	BSEL
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**
P1*	Port 1	90H	CEX4/ SPICLK	CEX3/ MISO	CEX2/ MOSI	CEX1/$\overline{SS}$	CEX0	ECI	T2EX	T2
		Bit address	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD
PCON	Power Control Register	87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P
RCAP2H	Timer2 Capture HIGH	CBH								
RCAP2L	Timer2 Capture LOW	CAH								
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**
SCON*	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	Serial Port Data Buffer Register	99H								

6.2 Memory organization

The device has separate address spaces for program and data memory.

6.2.1 Flash program memory bank selection

There are two internal flash memory blocks in the device. Block 0 has 16/32/64 kB and is organized as 128/256/512 sectors, each sector consists of 128 B. Block 1 contains the IAP/ISP routines and may be enabled such that it overlays the first 8 kB of the user code memory. The overlay function is controlled by the combination of the Software Reset Bit (SWR) at FCF.1 and the Bank Select Bit (BSEL) at FCF.0. The combination of these bits and the memory source used for instructions is shown in Table 5.

Table 5. Code memory bank selection

SWR (FCF.1)	BSEL (FCF.0)	Addresses from 0000H to 1FFFH	Addresses above 1FFFH
0	0	boot code (in block 1)	user code (in block 0)
0	1	user code (in block 0)	
1	0		
1	1		

Access to the IAP routines in block 1 may be enabled by clearing the BSEL bit (FCF.0), provided that the SWR bit (FCF.1) is cleared. Following a power-on sequence, the boot code is automatically executed and attempts to autobaud to a host. If no autobaud occurs within approximately 400 ms and the SoftICE flag is not set, control will be passed to the user code. A software reset is used to accomplish this control transfer and as a result the SWR bit will remain set. **Therefore the user's code will need to clear the SWR bit in order to access the IAP routines in block 1.** However, caution must be taken when dynamically changing the BSEL bit. Since this will cause different physical memory to be mapped to the logical program address space, the user must avoid clearing the BSEL bit when executing user code within the address range 0000H to 1FFFH.

6.2.2 Power-on reset code execution

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins high. Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the 1 kB of on-chip RAM while the device is running, however, the contents of the on-chip RAM during power up are indeterminate.

When power is applied to the device, the RST pin must be held high long enough for the oscillator to start up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 4. Note that if an RC circuit is used, provision should be made to ensure the V_{DD} rise time does not exceed 1 ms and the oscillator start-up time does not exceed 10 ms.

For a low frequency oscillator with slow start-up time the reset signal must be extended in order to account for the slow start-up time. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location, which may cause corruption in the Flash code. The power-on detection is designed to

Table 12. ISP hex record formats

Record type	Command/data function
00	Program User Code Memory :nnaaaa00dd..ddcc Where: nn = number of bytes to program aaaa = address dd..dd = data bytes cc = checksum Example: :10000000010203040500607080 9cc
01	End of File (EOF), no operation :xxxxxx01cc Where: xxxxxx = required field but value is a ‘don’t care’ cc = checksum Example: :00000001FF
02	Set SoftICE mode Following the next reset the device will enter the SoftICE mode. Will erase user code memory, and erase device serial number. :00000002cc Where: xxxxxx = required field but value is a ‘don’t care’ cc = checksum Example: :00000002FE

Table 12. ISP hex record formats *…continued*

Record type	Command/data function
09	Write serial number :nnxxxx09ss..sscc Where: xxxxxx = required field but value is a ‘don’t care’ 09 = write serial number function ss..ss = serial number contents cc = checksum Example: :03000009010203EE (write serial number = 010203)
0A	Display serial number :xxxxxx0Acc Where: xxxxxx = required field but value is a ‘don’t care’ 0A = display serial number function cc = checksum Example: :0000000AF6
0B	Reset and run user code :xxxxxx0Bcc Where: xxxxxx = required field but value is a ‘don’t care’ 0B = reset and run user code cc = checksum Example: :0000000BF5

6.3.5 Using the serial number

This device has the option of storing a 31 B serial number along with the length of the serial number (for a total of 32 B) in a non-volatile memory space. When ISP mode is entered, the serial number length is evaluated to determine if the serial number is in use. If the length of the serial number is programmed to either 00H or FFH, the serial number is considered not in use. If the serial number is in use, reading, programming, or erasing of the user code memory or the serial number is blocked until the user transmits a ‘verify serial number’ record containing a serial number and length that matches the serial number and length previously stored in the device. The user can reset the serial number to all zeros and set the length to zero by sending the ‘reset serial number' record. In addition, the ‘reset serial number’ record will also erase all user code.

6.3.6 IAP method

Several IAP calls are available for use by an application program to permit selective erasing, reading and programming of flash sectors, security bit, configuration bytes, and device id. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller’s registers before making a call to PGM_MTP at 1FF0H. The IAP calls are shown in Table 13.

Table 13. IAP function calls *...continued*

IAP function	IAP call parameters
Read Security Bit, Double Clock, SoftICE	**Input parameters:** ACC = 07H **Return parameter(s):** ACC = 000 S/N-match 0 SB 0 DBL_CLK
Read Security Bit, Double Clock, SoftICE	**Input parameters:** ACC = 07H **Return parameter(s):** ACC = 00 SoftICE S/N-match 0 SB 0 DBL_CLK
Erase sector	**Input parameters:** R1 = 08H DPH = sector address high byte DPL = sector address low byte **Return parameter(s):** ACC = 00 = pass ACC = !00 = fail

6.4 Timers/counters 0 and 1

The two 16-bit Timer/counter registers: Timer 0 and Timer 1 can be configured to operate either as timers or event counters (see Table 14 and Table 15).

In the ‘Timer’ function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of six oscillator periods, the count rate is $\frac{1}{6}$ of the oscillator frequency.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once every machine cycle.

When the samples show a HIGH in one cycle and a LOW in the next cycle, the count is incremented. The new count value appears in the register in the machine cycle following the one in which the transition was detected. Since it takes two machine cycles (12 oscillator periods) for 1-to-0 transition to be recognized, the maximum count rate is $\frac{1}{12}$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle. In addition to the ‘Timer’ or ‘Counter’ selection, Timer 0 and Timer 1 have four operating modes from which to select.

The ‘Timer’ or ‘Counter’ function is selected by control bits C/T in the special function register TMOD. These two timer/counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both timers/counters. Mode 3 is different. The four operating modes are described in the following text.

Table 14. TMOD - Timer/counter mode control register (address 89H) bit allocation

Not bit addressable; reset value: 0000 0000B; reset source(s): any source.

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

Table 21. T2CON - Timer/counter 2 control register (address C8H) bit descriptions

Bit	Symbol	Description
4	TCLK	Transmit clock flag. When set, causes the UART to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	Start/stop control for Timer 2. A logic '1' enables the timer to run.
1	C/$\overline{T}$2	Timer or counter select. (Timer 2) 0 = internal timer (f_{osc} / 6) 1 = external event counter (falling edge triggered; external clock's maximum rate = f_{osc} /12
0	CP/$\overline{RL}$2	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 22. T2MOD - Timer 2 mode control register (address C9H) bit allocation

Not bit addressable; Reset value: XX00 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T2OE	DCEN

Table 23. T2MOD - Timer 2 mode control register (address C9H) bit descriptions

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to '0' by user programs.
1	T2OE	Timer 2 Output Enable bit. Used in programmable clock-out mode only.
0	DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

6.5.1 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2 in T2CON) which upon overflowing sets bit TF2, the Timer 2 overflow bit.

The capture mode is illustrated in Figure 11.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF.

6.6.8 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed so that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in a way that the 9th bit is ‘1’ in an address byte and ‘0’ in the data byte. With SM2 = 1, no slave will be interrupted by a data byte, i.e. the received 9th bit is ‘0’. However, an address byte having the 9th bit set to ‘1’ will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed or not. The addressed slave will clear its SM2 bit and prepare to receive the data (still 9 bits long) that follow. The slaves that weren’t being addressed leave their SM2 bits set and ignore the subsequent data bytes.

SM2 has no effect in mode 0, and in mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. When the UART receives data in mode 1 and SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.6.9 Automatic address recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled for the UART by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the ‘Given’ address or the ‘Broadcast' address. The 9 bit mode requires that the 9th information bit is a ‘1’ to indicate that the received information is an address and not data.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two Special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are ‘don’t care’. The SADEN mask can be logically ANDed with the SADDR to create the ‘Given’ address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others.

This device uses the methods presented in Figure 15 to determine if a ‘Given’ or ‘Broadcast’ address has been received or not.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Example 1, slave 0:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1001} \\ \text{Given} = 1100\ 0\text{XX}0 \end{array} \quad (6)$$

Example 2, slave 1:

$$\begin{array}{l} \text{SADDR} = 1110\ 0000 \\ \underline{\text{SADEN} = 1111\ 1010} \\ \text{Given} = 1110\ 0\text{X}0\text{X} \end{array} \quad (7)$$

Example 3, slave 2:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1100} \\ \text{Given} = 1100\ 00\text{XX} \end{array} \quad (8)$$

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all 'don't cares' as well as a Broadcast address of all 'don't cares'. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

6.7 SPI

6.7.1 SPI features

- Master or slave operation
- 10 MHz bit frequency (maximum)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write collision flag protection (WCOL)
- Wake-up from Idle mode (slave mode only)

6.7.2 SPI description

The SPI allows high-speed synchronous data transfer between the P89LV51RB2/RC2/RD2 and peripheral devices or between several P89LV51RB2/RC2/RD2 devices. Figure 16 shows the correspondence between master

Table 29. SPCTL - SPI control register (address D5H) bit descriptions *...continued*

Bit	Symbol	Description
2	CPHA	Clock Phase control bit. 1 = shift triggered on the trailing edge of the clock; 0 = shift triggered on the leading edge of the clock.
1	PSC1	SPI Clock Rate Select bit 1. Along with PSC0 controls the SPICLK rate of the device when a master. PSC1 and PSC0 have no effect on the slave. See Table 30.
0	PSC0	SPI Clock Rate Select bit 0. Along with PSC1 controls the SPICLK rate of the device when a master. PSC1 and PSC0 have no effect on the slave. See Table 30.

Table 30. SPCTL - SPI control register (address D5H) clock rate selection

PSC1	PSC0	SPICLK = f_{osc} divided by
0	0	4
0	1	16
1	0	64
1	1	128

Table 31. SPCFG - SPI status register (address AAH) bit allocation

Bit addressable; reset source(s): any reset; reset value: 0000 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIF	WCOL	-	-	-	-	-	-

Table 32. SPCFG - SPI status register (address AAH) bit descriptions

Bit	Symbol	Description
7	SPIF	SPI interrupt flag. Upon completion of data transfer, this bit is set to '1'. If SPIE = 1 and ES = 1, an interrupt is then generated. This bit is cleared by software.
6	WCOL	Write Collision Flag. Set if the SPI data register is written to during data transfer. This bit is cleared by software.
5 to 0	-	Reserved for future use. Should be set to '0' by user programs.

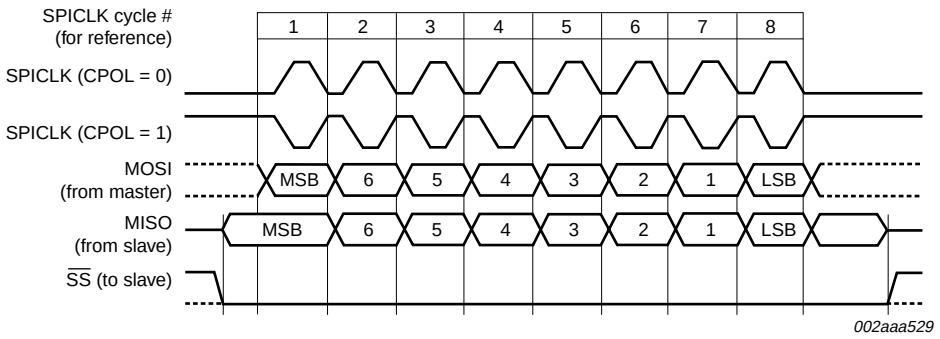


Fig 17. SPI transfer format with CPHA = 0

In the CMOD SFR there are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during Idle mode, WDTE which enables or disables the Watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The watchdog timer function is implemented in module 4 of PCA.

The CCON SFR contains the run control bit (CR) for the PCA and the flags for the PCA timer (CF) and each module (CCF4:0). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software. All the modules share one interrupt vector. The PCA interrupt system is shown in Figure 21.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. The registers contain the bits that control the mode that each module operates in.

The ECCFn bit (from CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on the module) enables the CCFn flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module (see Figure 21).

PWM (CCAPMn.1) enables the pulse width modulation mode.

The TOGn bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.

The match bit MATn (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPNn (CCAPMn.4) and CAPPn (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPPn bit enables the positive edge. If both bits are set, both edges will be enabled and a capture will occur for either transition.

The last bit in the register ECOMn (CCAPMn.6) when set enables the comparator function.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

Table 41. CCAPMn - PCA modules compare/capture register (address CCAPM0: 0DAH, CCAPM1: 0DBH, CCAPM2: 0DCH, CCAPM3: 0DDH, CCAPM4: 0DEH) bit descriptions *...continued*

Bit	Symbol	Description
3	MATn	Match. When MATn = 1 a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
2	TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
1	PWMn	Pulse Width Modulation mode. PWMn = 1 enables the CEXn pin to be used as a pulse-width modulated output.
0	ECCFn	Enable CCF Interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

Table 42. PCA module modes (CCAPMn register)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module function
0	0	0	0	0	0	0	no operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative-edge trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by any transition on CEXn
1	0	0	1	0	0	X	16-bit software timer
1	0	0	1	1	0	X	16-bit high-speed output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	Watchdog timer

6.9.1 PCA capture mode

To use one of the PCA modules in the capture mode (Figure 22) either one or both of the CCAPM bits CAPNn and CAPPn for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH).

6.10 Security bit

The Security Bit protects against software piracy and prevents the contents of the flash from being read by unauthorized parties in Parallel Programmer mode. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory.

When the Security Bit is activated, all parallel programming commands except for Chip-Erase are ignored (thus the device cannot be read). However, ISP reading, writing, or erasing of the user's code can still be performed if the serial number and length has not been programmed. **Therefore, when a user requests to program the Security Bit, the programmer should prompt the user and program a serial number into the device.**

6.11 Interrupt priority and polling sequence

The device supports eight interrupt sources under a four level priority scheme. Table 43 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. (See Figure 26).

Table 43. Interrupt polling sequence

Description	Interrupt flag	Vector address	Interrupt enable bit	Interrupt priority bit	Service priority	Wake-up power-down
External interrupt 0	IE0	0003H	EX0	PX0/H	1 (highest)	yes
Brownout	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
External interrupt 1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	7	no
T2	TF2, EXF2	002BH	ET2	PT2/H	8	no

Table 51. IP0H - Interrupt priority 0 high register (address B7H) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	PPCH	PCA interrupt priority HIGH bit.
5	PT2H	Timer 2 interrupt priority HIGH bit.
4	PSH	Serial Port interrupt priority HIGH bit.
3	PT1H	Timer 1 interrupt priority HIGH bit.
2	PX1H	External interrupt 1 priority HIGH bit.
1	PT0H	Timer 0 interrupt priority HIGH bit.
0	PX0H	External interrupt 0 priority HIGH bit.

Table 52. IP1 - Interrupt priority 1 register (address F8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	PBO	-	-	-	-

Table 53. IP1 - Interrupt priority 1 register (address F8H) bit descriptions

Bit	Symbol	Description
7 to 5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	PBO	Brownout interrupt priority bit.
3 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

Table 54. IP1H - Interrupt priority 1 high register (address F7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	PBOH	-	-	-	-

Table 55. IP1H - Interrupt priority 1 high register (address F7H) bit descriptions

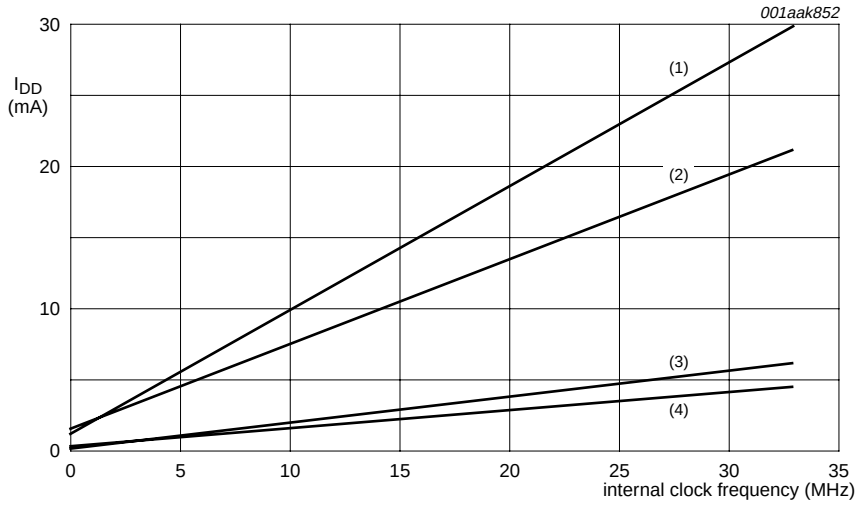
Bit	Symbol	Description
7 to 5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	PBOH	Brownout interrupt priority bit.
3 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

6.12 Power-saving modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are Idle and Power-down, see Table 56.

6.12.1 Idle mode

Idle mode is entered by setting the IDL bit in the PCON register. In Idle mode, the Program Counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.



(1) Maximum $I_{DD(oper)}$

(2) Maximum $I_{DD(idle)}$

(3) Typical $I_{DD(oper)}$

(4) Typical $I_{DD(idle)}$

Fig 28. Supply current versus frequency

9.1 Explanation of symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The characters are described below:

A — Address

C — Clock

D — Input data

H — Logic level HIGH

I — Instruction (program memory contents)

L — Logic level LOW or ALE

P — $\overline{\text{PSEN}}$

Q — Output data

R — $\overline{\text{RD}}$ signal

T — Time

V — Valid

W — $\overline{\text{WR}}$ signal

X — No longer a valid logic level

Z — High impedance (Float)

Example:

t_{AVLL} = Address valid to ALE LOW time

t_{LLPL} = ALE LOW to $\overline{\text{PSEN}}$ LOW time

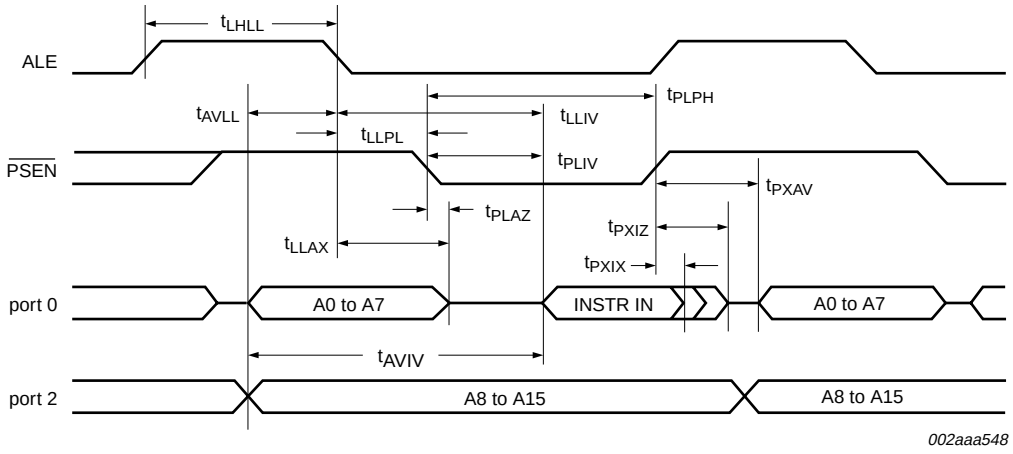


Fig 29. External program memory read cycle

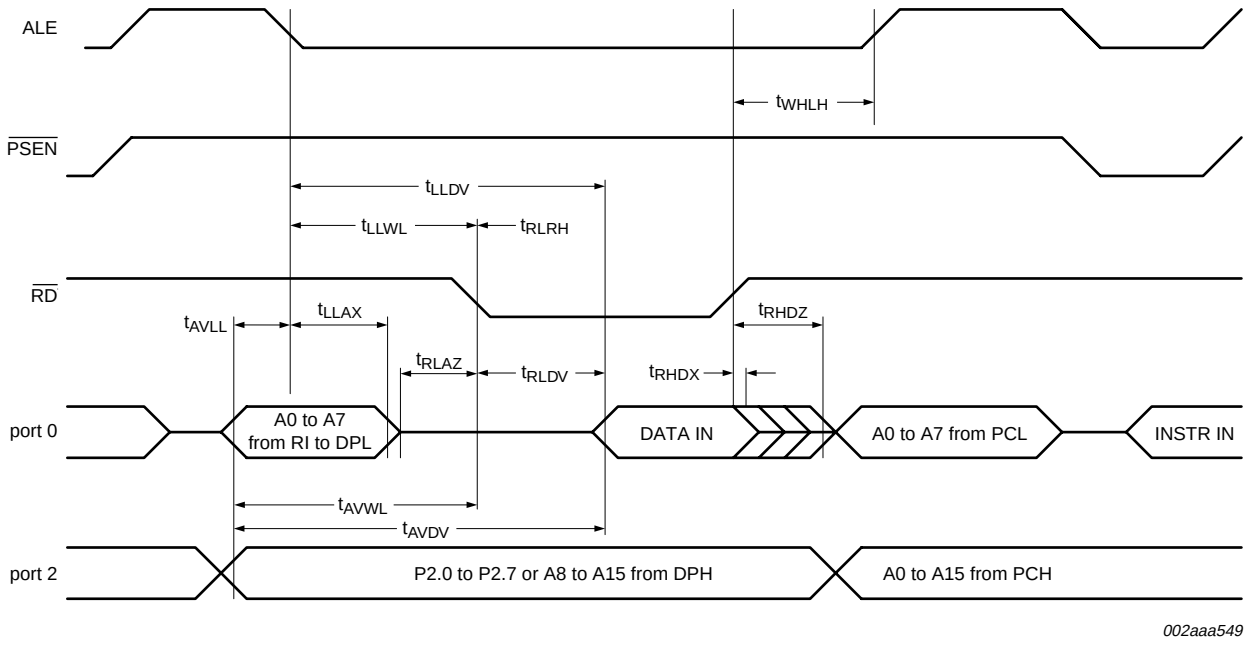


Fig 30. External data memory read cycle

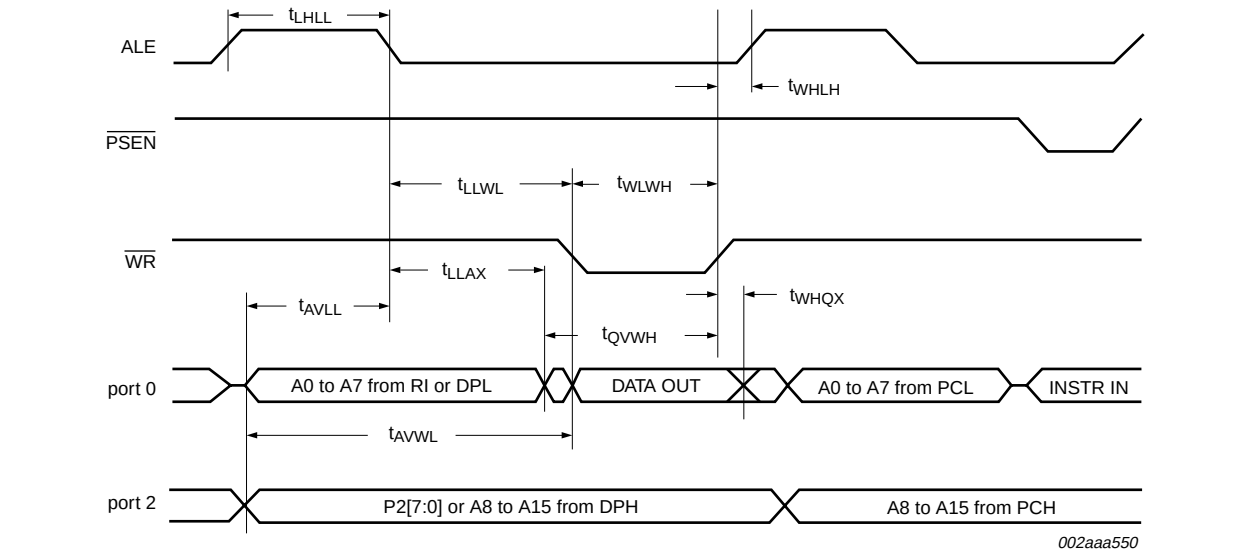


Fig 31. External data memory write cycle

13. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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