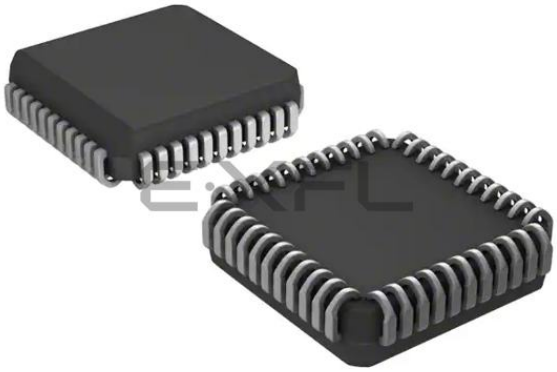

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lv51rd2fa-512

Table 4. Special function registers

** Indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0
ACC*	Accumulator	E0H								
AUXR	Auxiliary function register	8EH	-	-	-	-	-	-	EXTRAM	AO
AUXR1	Auxiliary function register 1	A2H	-	-	-	-	GF2	0	-	DPS
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0
B*	B register	F0H								
CCAP0H	Module 0 Capture HIGH	FAH								
CCAP1H	Module 1 Capture HIGH	FBH								
CCAP2H	Module 2 Capture HIGH	FCH								
CCAP3H	Module 3 Capture HIGH	FDH								
CCAP4H	Module 4 Capture HIGH	FEH								
CCAP0L	Module 0 Capture LOW	EAH								
CCAP1L	Module 1 Capture LOW	EBH								
CCAP2L	Module 2 Capture LOW	ECH								
CCAP3L	Module 3 Capture LOW	EDH								
CCAP4L	Module 4 Capture LOW	EEH								
CCAPM0	Module 0 Mode	DAH	-	ECOM_0	CAPP_0	CAPN_0	MAT_0	TOG_0	PWM_0	ECCF_0
CCAPM1	Module 1 Mode	DBH	-	ECOM_1	CAPP_1	CAPN_1	MAT_1	TOG_1	PWM_1	ECCF_1
CCAPM2	Module 2 Mode	DCH	-	ECOM_2	CAPP_2	CAPN_2	MAT_2	TOG_2	PWM_2	ECCF_2
CCAPM3	Module 3 Mode	DDH	-	ECOM_3	CAPP_3	CAPN_3	MAT_3	TOG_3	PWM_3	ECCF_3
CCAPM4	Module 4 Mode	DEH	-	ECOM_4	CAPP_4	CAPN_4	MAT_4	TOG_4	PWM_4	ECCF_4
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8
CCON*	PCA Counter Control	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
CH	PCA Counter HIGH	F9H								
CL	PCA Counter LOW	E9H								
CMOD	PCA Counter Mode	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
DPTR	Data Pointer (2 B)									
DPH	Data Pointer HIGH	83H								
DPL	Data Pointer LOW	82H								

Table 4. Special function registers *…continued*

** Indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
SADDR	Serial Port Address Register	A9H								
SADEN	Serial Port Address Enable	B9H								
		Bit address	**87**[1]	**86**[1]	**85**[1]	**84**[1]	**83**[1]	**82**[1]	**81**[1]	**80**[1]
SPCTL	SPI Control Register	D5H	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	PSC1	PSC0
SPCFG	SPI Configuration Register	AAH	SPIF	WCOL	-	-	-	-	-	-
SPDAT	SPI Data	86H								
SP	Stack Pointer	81H								
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**
TCON*	Timer Control Register	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Bit address	**CF**	**CE**	**CD**	**CC**	**CB**	**CA**	**C9**	**C8**
T2CON*	Timer2 Control Register	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/RL2
T2MOD	Timer2 Mode Control	C9H	-	-	ENT2	-	-	-	T2OE	DCEN
TH0	Timer 0 HIGH	8CH								
TH1	Timer 1 HIGH	8DH								
TH2	Timer 2 HIGH	CDH								
TL0	Timer 0 LOW	8AH								
TL1	Timer 1 LOW	8BH								
TL2	Timer 2 LOW	CCH								
TMOD	Timer 0 and 1 Mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0
WDTC	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT
WDTD	Watchdog Timer Data/Reload	85H								

[1] Unimplemented bits in SFRs (labeled '-') are 'X's (unknown) at all times. Unless otherwise specified, '1's should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

Since the upper 128 B occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

Table 7. AUXR - Auxiliary register (address 8EH) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXTRAM	AO

Table 8. AUXR - Auxiliary register (address 8EH) bit descriptions

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to '0' by user programs.
1	EXTRAM	Internal/External RAM access using MOVX-@Ri/@DPTR. When '0', core attempts to access internal XRAM with address specified in MOVX instruction. If address supplied with this instruction exceeds on-chip available XRAM, off-chip XRAM is going to be selected and accessed. When '1', every MOVX-@Ri/@DPTR instruction targets external data memory by default.
0	AO	ALE off: disables/enables ALE. AO = 0 results in ALE emitted at a constant rate of $\frac{1}{2}$ the oscillator frequency. In case of AO = 1, ALE is active only during a MOVX or MOVC.

When instructions access addresses in the upper 128 B (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in '#data' is written to RAM location 90H rather than port 1.

Direct access:

MOV90H, #data; write data to P1

Data in '#data' is written to port 1. Instructions that write directly to the address, write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 B of memory is physically located on the chip and logically occupies the first 768 B of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 ($\overline{WR}$), P3.7 ($\overline{RD}$), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM access (indirect addressing only):

MOVX@DPTR, A DPTR contains 0A0H

Table 12. ISP hex record formats *…continued*

Record type	Command/data function
03	Miscellaneous Write functions :nnxxxx03ffssddcc Where: nn = number of bytes in the record xxxx = required field but value is a 'don't care' ff = subfunction code ss = selection code dd = data (if needed) cc = checksum Subfunction code = 01 (Erase block 0) ff = 01 Subfunction code = 05 (Program security bit, Double Clock) ff = 05 ss = 01 program security bit ss = 05 program double clock bit Subfunction code = 08 (Erase sector, 128 B) ff = 08 ss = high byte of sector address (A15:8) dd = low byte of sector address (A7, A6:0]= 0) Example: :0300000308E000F2 (erase sector at E000H)
04	Display Device Data or Blank Check :05xxxx04sssseeeeffcc Where 05 = number of bytes in the record xxxx = required field but value is a 'don't care' 04 = function code for display or blank check ssss = starting address, MSB first eeee = ending address, MSB first ff = subfunction 00 = display data 01 = blank check cc = checksum Subfunction codes: Example: :0500000400001FFF00D9 (display from 0000H to 1FFFH)

Table 15. TMOD - Timer/counter mode control register (address 89H) bit descriptions

Bit	Symbol	Description
	T1/T0	Bits controlling Timer1/Timer0
	GATE	Gating control when set. Timer/counter 'x' is enabled only while 'INTx' $\overline{\text{INTx}}$ pin is HIGH and 'TRx' control pin is set. When cleared, Timer 'x' is enabled whenever 'TRx' control bit is set.
	C/$\overline{\text{T}}$	Gating Timer or Counter Selector cleared for Timer operation (input from internal system clock). Set for Counter operation (input from 'Tx' input pin).

Table 16. TMOD - Timer/counter mode control register (address 89H) M1/M0 operating mode

M1	M0	Operating mode	
0	0	0	8048 timer 'TLx' serves as 5-bit prescaler
0	1	1	16-bit Timer/counter 'THx' and 'TLx' are cascaded; there is no prescaler.
1	0	2	8-bit auto-reload Timer/counter 'THx' holds a value which is to be reloaded into 'TLx' each time it overflows.
1	1	3	(Timer 0) TL0 is an 8-bit Timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/counter 1 stopped.

Table 17. TCON - Timer/counter control register (address 88H) bit allocation

Bit addressable; reset value: 0000 0000B; reset source(s): any reset.

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 18. TCON - Timer/counter control register (address 88H) bit descriptions

Bit	Symbol	Description
7	TF1	Timer 1 overflow flag. Set by hardware on Timer/counter overflow. Cleared by hardware when the processor vectors to Timer 1 Interrupt routine, or by software.
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/counter 1 on/off.
5	TF0	Timer 0 overflow flag. Set by hardware on Timer/counter overflow. Cleared by hardware when the processor vectors to Timer 0 Interrupt routine, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/counter 0 on/off.
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/low level is detected. Cleared by hardware when the interrupt is processed, or by software.

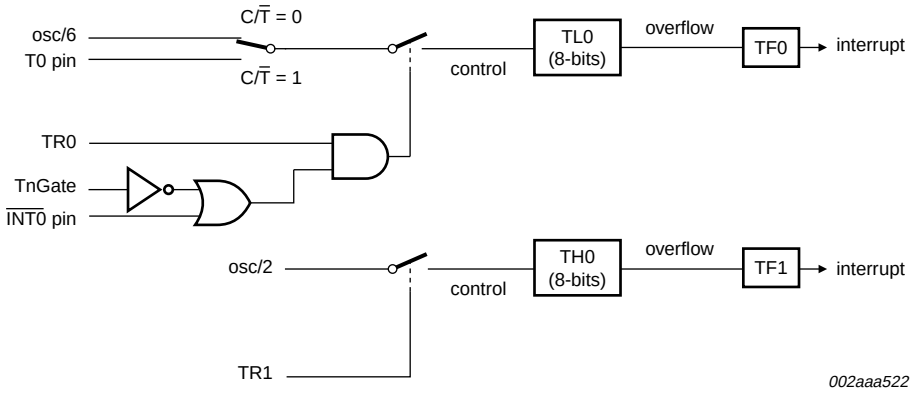


Fig 10. Timer/counter 0 mode 3 (two 8-bit counters)

6.5 Timer 2

Timer 2 is a 16-bit Timer/counter which can operate as either an event timer or an event counter, as selected by C/$\overline{T}$2 in the special function register T2CON. Timer 2 has four operating modes: Capture, Auto-reload (up or down counting), Clock-out, and Baud Rate Generator which are selected according to Table 19 using T2CON (Table 20 and Table 21) and T2MOD (Table 22 and Table 23).

Table 19. Timer 2 operating mode

RCLK + TCLK	CP/$\overline{RL}$2	TR2	T2OE	Mode
0	0	1	0	16-bit auto reload
0	1	1	0	16-bit capture
0	0	1	1	programmable clock-out
1	X	1	0	baud rate generator
X	X	0	X	off

Table 20. T2CON - Timer/counter 2 control register (address C8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2

Table 21. T2CON - Timer/counter 2 control register (address C8H) bit descriptions

Bit	Symbol	Description
7	TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1 or when Timer 2 is in Clock-out mode.
6	EXF2	Timer 2 external flag is set when Timer 2 is in capture, reload or baud-rate mode, EXEN2 = 1 and a negative transition on T2EX occurs. If Timer 2 interrupt is enabled, EXF2 = 1 causes the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
5	RCLK	Receive clock flag. When set, causes the UART to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

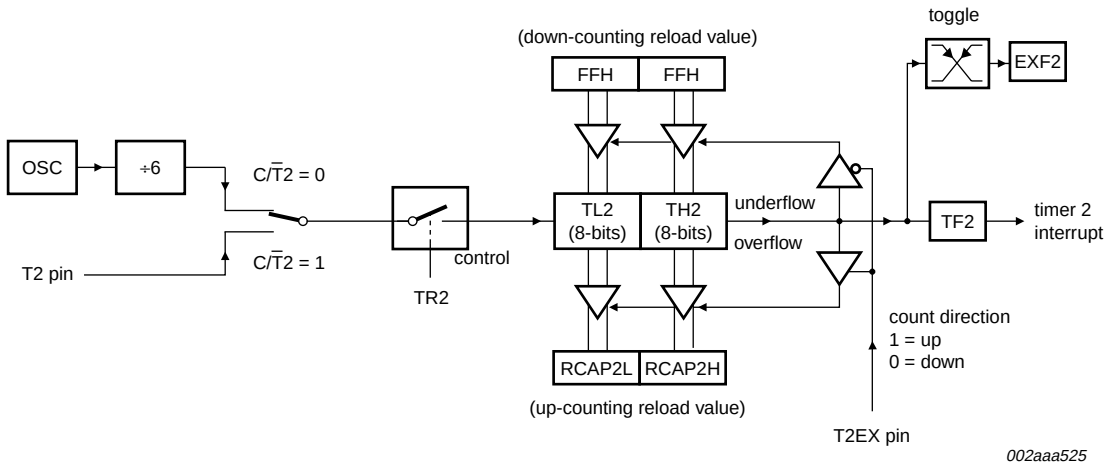


Fig 13. Timer 2 in Auto Reload mode (DCEN = 1)

A logic 0 applied at pin T2EX causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2. The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1.0). This pin, besides being a I/O pin, has two additional functions. It can be programmed:

- To input the external clock for Timer/counter 2, or
- To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the Timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{Oscillator\ Frequency}{2 \times (65536 \angle (RCAP2H, RCAP2L))} \quad (2)$$

Where (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART transmit and receive baud rates to be derived from either Timer 1 or Timer 2 (See Section 6.6 “UART” on page 37 for details). When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When

not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. Under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers. Table 24 shows commonly used baud rates and how they can be obtained from Timer 2.

6.5.5 Summary of baud rate equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

Baud rate = Timer 2 overflow rate / 16

If Timer 2 is being clocked internally, the baud rate is:

Baud rate = f_{osc} / (16 × (65536 − (RCAP2H, RCAP2L)))

Where f_{osc} = oscillator frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

RCAP2H, RCAP2L = 65536 − f_{osc} / (16 × baud rate)

Table 24. Timer 2 generated commonly used baud rates

Rate	Oscillator frequency	Timer 2	
		RCAP2H	RCAP2L
750 kBd	12 MHz	FF	FF
19.2 kBd	12 MHz	FF	D9
9.6 kBd	12 MHz	FF	B2
4.8 kBd	12 MHz	FF	64
2.4 kBd	12 MHz	FE	C8
600 Bd	12 MHz	FB	1E
220 Bd	12 MHz	F2	AF
600 Bd	6 MHz	FD	8F
220 Bd	6 MHz	F9	57

6.6 UART

The UART operates in all standard modes. Enhancements over the standard 80C51 UART include Framing Error detection, and automatic address recognition.

6.6.1 Mode 0

Serial data enters and exits through RXD, and TXD outputs the shift clock. Only 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{6}$ of the CPU clock frequency. The UART is configured to operate in this mode and outputs serial clock on TXD line no matter whether it sends or receives data on the RXD line.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF.

6.6.8 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed so that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in a way that the 9th bit is ‘1’ in an address byte and ‘0’ in the data byte. With SM2 = 1, no slave will be interrupted by a data byte, i.e. the received 9th bit is ‘0’. However, an address byte having the 9th bit set to ‘1’ will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed or not. The addressed slave will clear its SM2 bit and prepare to receive the data (still 9 bits long) that follow. The slaves that weren’t being addressed leave their SM2 bits set and ignore the subsequent data bytes.

SM2 has no effect in mode 0, and in mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. When the UART receives data in mode 1 and SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.6.9 Automatic address recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled for the UART by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the ‘Given’ address or the ‘Broadcast' address. The 9 bit mode requires that the 9th information bit is a ‘1’ to indicate that the received information is an address and not data.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two Special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are ‘don’t care’. The SADEN mask can be logically ANDed with the SADDR to create the ‘Given’ address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others.

This device uses the methods presented in Figure 15 to determine if a ‘Given’ or ‘Broadcast’ address has been received or not.

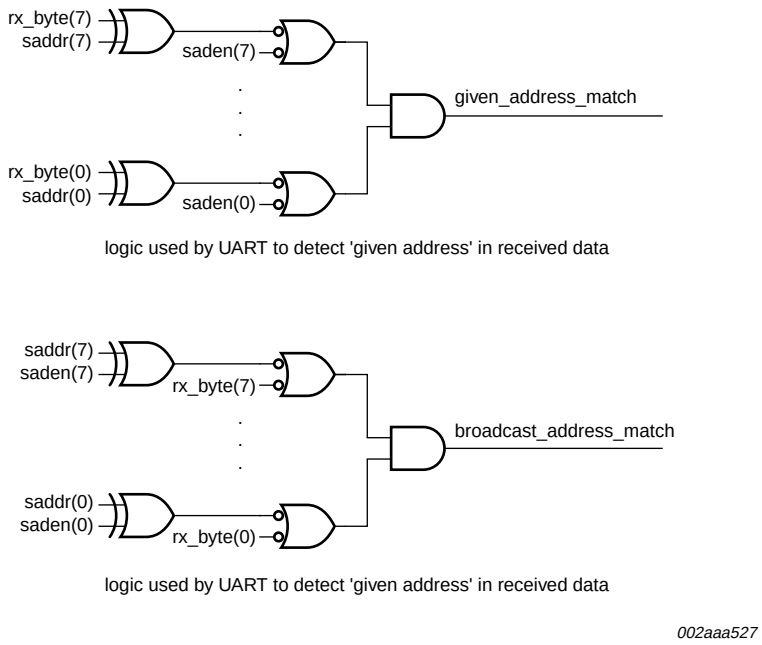


Fig 15. Schemes used by the UART to detect ‘given’ and ‘broadcast’ addresses when multiprocessor communications is enabled

The following examples help to show the versatility of this scheme.

Example 1, slave 0:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1101} \\ \text{Given} = 1100\ 00\text{X}0 \end{array} \quad (4)$$

Example 2, slave 1:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1110} \\ \text{Given} = 1100\ 000\text{X} \end{array} \quad (5)$$

In the above example value SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a ‘0’ in bit 0 and it ignores bit 1. Slave 1 requires a ‘0’ in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a ‘0’ in bit 1. A unique address for slave 1 would be 1100 0001 since a ‘1’ in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In the CMOD SFR there are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during Idle mode, WDTE which enables or disables the Watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The watchdog timer function is implemented in module 4 of PCA.

The CCON SFR contains the run control bit (CR) for the PCA and the flags for the PCA timer (CF) and each module (CCF4:0). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software. All the modules share one interrupt vector. The PCA interrupt system is shown in Figure 21.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. The registers contain the bits that control the mode that each module operates in.

The ECCFn bit (from CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on the module) enables the CCFn flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module (see Figure 21).

PWM (CCAPMn.1) enables the pulse width modulation mode.

The TOGn bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.

The match bit MATn (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPNn (CCAPMn.4) and CAPPn (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPPn bit enables the positive edge. If both bits are set, both edges will be enabled and a capture will occur for either transition.

The last bit in the register ECOMn (CCAPMn.6) when set enables the comparator function.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

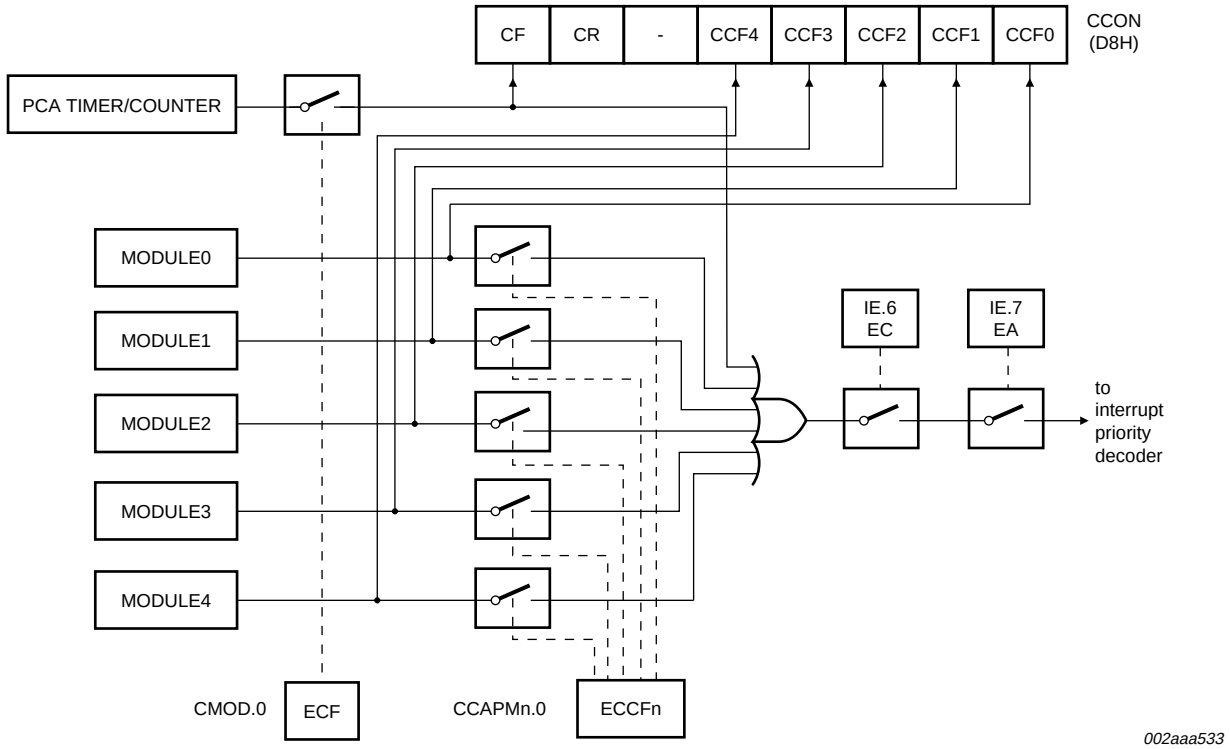


Fig 21. PCA interrupt system

Table 35. CMOD - PCA counter mode register (address D9H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Table 36. CMOD - PCA counter mode register (address D9H) bit descriptions

Bit	Symbol	Description
7	CIDL	Counter Idle Control: CIDL = 0 programs the PCA Counter to continue functioning during Idle mode. CIDL = 1 programs it to be gated off during idle.
6	WDTE	Watchdog Timer Enable: WDTE = 0 disables watchdog timer function on module 4. WDTE = 1 enables it.
5 to 3	-	Reserved for future use. Should be set to '0' by user programs.
2 to 1	CPS1, CPS0	PCA Count Pulse Select (see Table 37 below).
0	ECF	PCA Enable Counter Overflow Interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function.

6.10 Security bit

The Security Bit protects against software piracy and prevents the contents of the flash from being read by unauthorized parties in Parallel Programmer mode. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory.

When the Security Bit is activated, all parallel programming commands except for Chip-Erase are ignored (thus the device cannot be read). However, ISP reading, writing, or erasing of the user's code can still be performed if the serial number and length has not been programmed. **Therefore, when a user requests to program the Security Bit, the programmer should prompt the user and program a serial number into the device.**

6.11 Interrupt priority and polling sequence

The device supports eight interrupt sources under a four level priority scheme. Table 43 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. (See Figure 26).

Table 43. Interrupt polling sequence

Description	Interrupt flag	Vector address	Interrupt enable bit	Interrupt priority bit	Service priority	Wake-up power-down
External interrupt 0	IE0	0003H	EX0	PX0/H	1 (highest)	yes
Brownout	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
External interrupt 1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	7	no
T2	TF2, EXF2	002BH	ET2	PT2/H	8	no

Table 45. IEN0 - Interrupt enable register 0 (address A8H) bit descriptions

Bit	Symbol	Description
7	EA	Interrupt Enable Bit: EA = 1 interrupt(s) can be serviced, EA = 0 interrupt servicing disabled.
6	EC	PCA Interrupt Enable bit.
5	ET2	Timer 2 Interrupt Enable.
4	ES	Serial Port Interrupt Enable.
3	ET1	Timer 1 Overflow Interrupt Enable.
2	EX1	External Interrupt 1 Enable.
1	ET0	Timer 0 Overflow Interrupt Enable.
0	EX0	External Interrupt 0 Enable.

Table 46. IEN1 - Interrupt enable register 1 (address E8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	EBO	-	-	-

Table 47. IEN1 - Interrupt enable register 1 (address E8H) bit descriptions

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Should be set to ‘0’ by user programs.
3	EBO	Brownout Interrupt Enable. 1 = enable, 0 = disable.
2 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

Table 48. IP0 - Interrupt priority 0 low register (address B8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Table 49. IP0 - Interrupt priority 0 low register (address B8H) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	PPC	PCA interrupt priority LOW bit.
5	PT2	Timer 2 interrupt priority LOW bit.
4	PS	Serial Port interrupt priority LOW bit.
3	PT1	Timer 1 interrupt priority LOW bit.
2	PX1	External interrupt 1 priority LOW bit.
1	PT0	Timer 0 interrupt priority LOW bit.
0	PX0	External interrupt 0 priority LOW bit.

Table 50. IP0H - Interrupt priority 0 high register (address B7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 58. Clock doubling features

Device	Standard mode (X1)		Clock double mode (X2)	
	Clocks per machine cycle	Maximum external clock frequency (MHz)	Clocks per machine cycle	Maximum external clock frequency (MHz)
P89LV51RB2/RC2/RD2	12	33	6	16

Table 59. FST - Flash status register (address B6) bit allocation

Not Bit addressable; reset value: xxxx x0xxB.

Bit	7	6	5	4	3	2	1	0
Symbol	-	SB	-	-	EDC	-	-	-

Table 60. FST - Flash status register (address B6) bit descriptions

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	SB	Security bit.
5 to 4	-	Reserved for future use. Should be set to ‘0’ by user programs.
3	EDC	Enable double clock.
2 to 0	-	Reserved for future use. Should be set to ‘0’ by user programs.

Table 62. Static characteristics *...continued*

T_{amb} = 0 °C to +70 °C or −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	HIGH-level output voltage	V_{DD} = 2.7 V; ports 1, 2, 3, ALE, $\overline{PSEN}$	[5]			
		I_{OH} = −10 µA		V_{DD} − 0.3	-	V
		I_{OH} = −30 µA		V_{DD} − 0.7	-	V
		I_{OH} = −60 µA		V_{DD} − 1.5	-	V
		V_{DD} = 2.7 V; port 0 in External Bus mode				
		I_{OH} = −200 µA		V_{DD} − 0.3	-	V
		I_{OH} = −3.2 mA		V_{DD} − 0.7	-	V
V_{bo}	brownout trip voltage			2.35	2.55	V
I_{IL}	LOW-level input current	V_I = 0.4 V; ports 1, 2, 3		-	−75	µA
I_{THL}	HIGH-LOW transition current	V_I = 2 V; ports 1, 2, 3	[6]	-	−650	µA
I_{LI}	input leakage current	0.45 V < V_I < V_{DD} − 0.3 V; port 0		-	±10	µA
R_{pd}	pull-down resistance	on pin RST		-	225	kΩ
C_{iss}	input capacitance	1 MHz; T_{amb} = 25 °C	[7]	-	15	pF
$I_{DD(oper)}$	operating supply current	f_{osc} = 12 MHz		-	11.5	mA
		f_{osc} = 33 MHz		-	30	mA
$I_{DD(idle)}$	Idle mode supply current	f_{osc} = 12 MHz		-	8.5	mA
		f_{osc} = 33 MHz		-	21	mA
$I_{DD(pd)}$	Power-down mode supply current	minimum V_{DD} = 2 V				
		T_{amb} = 0 °C to +70 °C		-	45	µA
		T_{amb} = −40 °C to +85 °C		-	55	µA

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per 8-bit port: 26 mA

b) Maximum I_{OL} total for all outputs: 71 mA

c) If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[3] Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

[4] Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[5] Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD} − 0.7 V specification when the address bits are stabilizing.

[6] Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_I is approximately 2 V.

[7] Pin capacitance is characterized but not tested. Pin $\overline{EA}$ = 25 pF (max).

9. Dynamic characteristics

Table 63. Dynamic characteristics

Over operating conditions: load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF; T_{amb} = 0 °C to +70 °C or −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V at 33 MHz; V_{SS} = 0 V.[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	X1 mode	0	-	33	MHz
		X2 mode	0	-	16	MHz
		IAP	0.25	-	33	MHz
t_{LHLL}	ALE pulse width		$2T_{cy(clk)} - 15$	-	-	ns
t_{AVLL}	address valid to ALE LOW time		$T_{cy(clk)} - 25$	-	-	ns
t_{LLAX}	address hold after ALE LOW time		$T_{cy(clk)} - 25$	-	-	ns
t_{LLIV}	ALE LOW to valid instruction in time		-	-	$4T_{cy(clk)} - 65$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW time		$T_{cy(clk)} - 25$	-	-	ns
t_{PLPH}	$\overline{PSEN}$ pulse width		$T_{cy(clk)} - 25$	-	-	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in time		-	-	$3T_{cy(clk)} - 55$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$ time		0	-	-	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$ time		-	-	$T_{cy(clk)} - 5$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid time		$T_{cy(clk)} - 8$	-	-	ns
t_{AVIV}	address to valid instruction in time		-	-	$5T_{cy(clk)} - 80$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float time		-	-	10	ns
t_{RLRH}	$\overline{RD}$ LOW pulse width		$6T_{cy(clk)} - 40$	-	-	ns
t_{WLWH}	$\overline{WR}$ LOW pulse width		$6T_{cy(clk)} - 40$	-	-	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in time		-	-	$5T_{cy(clk)} - 90$	ns
t_{RHDX}	data hold after $\overline{RD}$ time		0	-	-	ns
t_{RHDZ}	data float after $\overline{RD}$ time		-	-	$2T_{cy(clk)} - 25$	ns
t_{LLDV}	ALE LOW to valid data in time		-	-	$8T_{cy(clk)} - 90$	ns
t_{AVDV}	address to valid data in time		-	-	$9T_{cy(clk)} - 90$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW time		$3T_{cy(clk)} - 25$	-	$3T_{cy(clk)} + 25$	ns
t_{AVWL}	address to $\overline{RD}$ or $\overline{WR}$ LOW time		$4T_{cy(clk)} - 75$	-	-	ns
t_{WHQX}	data hold after $\overline{WR}$ time		$T_{cy(clk)} - 27$	-	-	ns
t_{QVWH}	data output valid to $\overline{WR}$ HIGH time		$7T_{cy(clk)} - 70$	-	-	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float time		-	-	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH time		$T_{cy(clk)} - 25$	-	$T_{cy(clk)} + 25$	ns

[1] $T_{cy(clk)} = 1 / f_{osc}$.

[2] Calculated values are for 6-clock mode only.

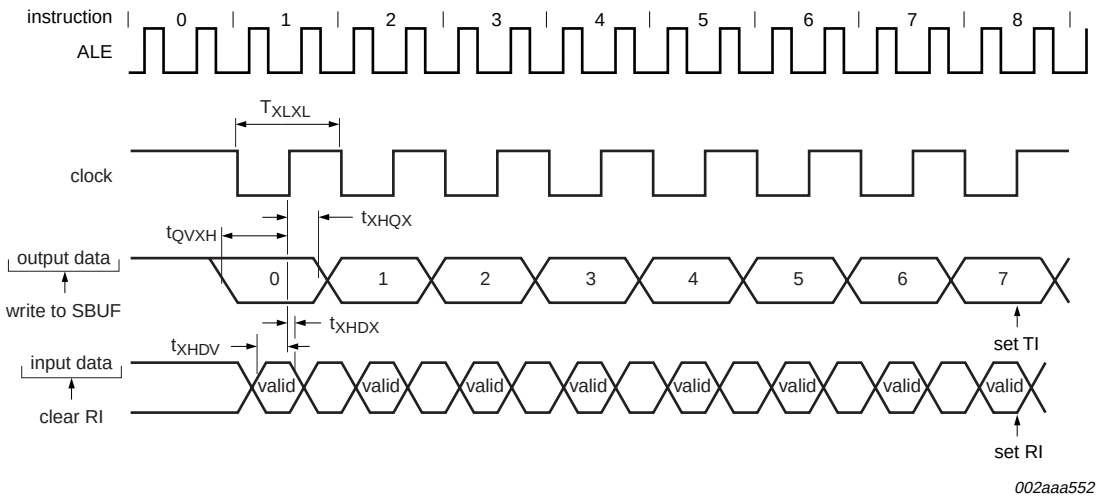


Fig 33. Shift register mode timing waveforms

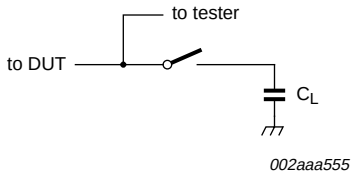
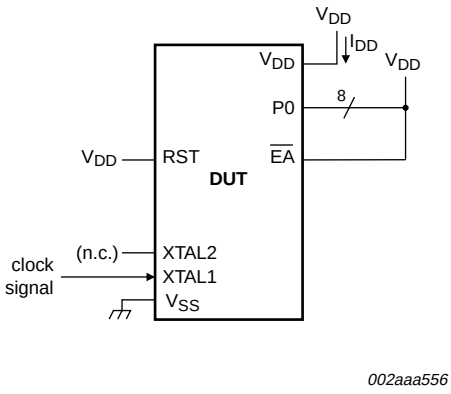


Fig 34. Test load example

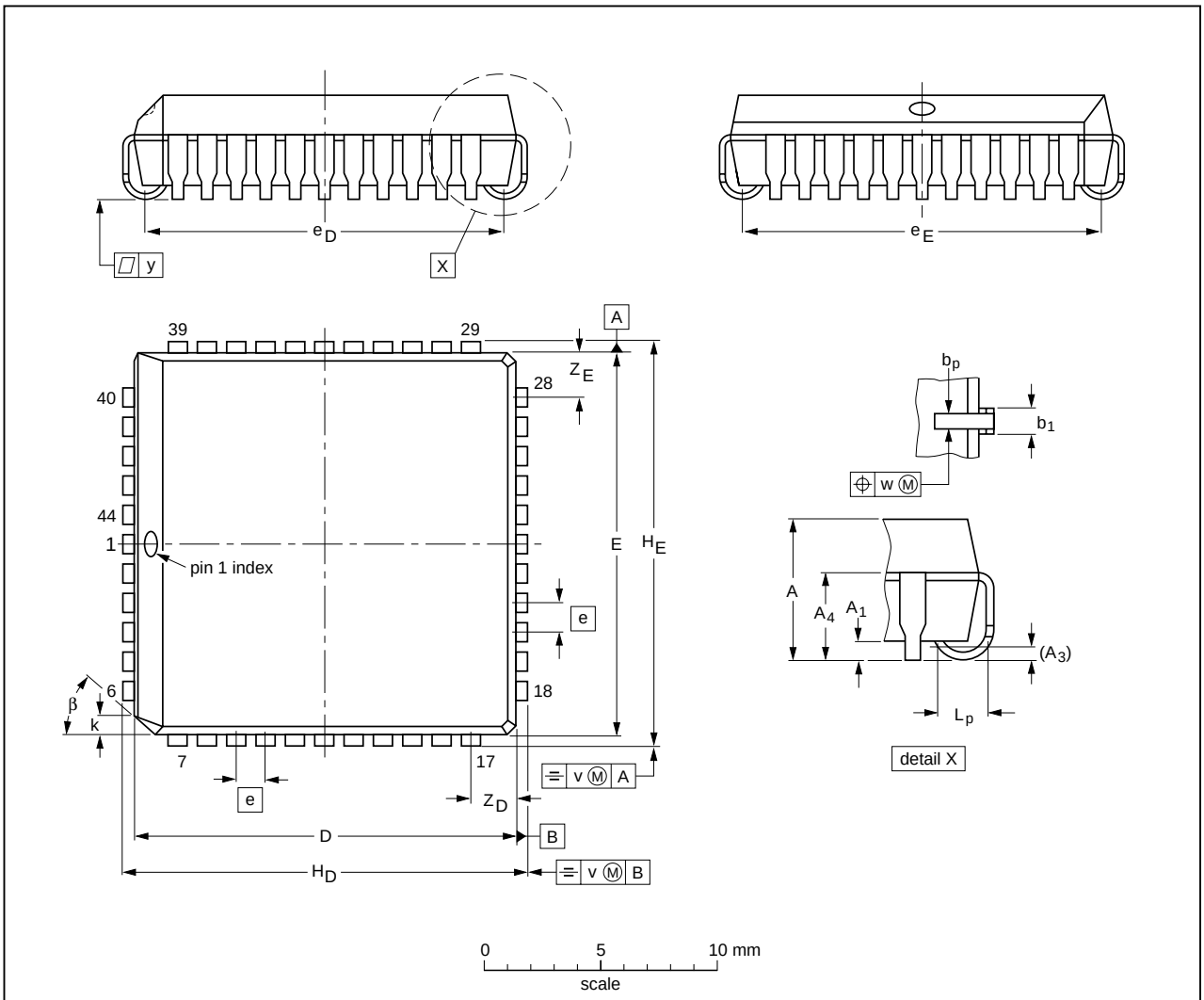


All other pins disconnected

Fig 35. I_{DD} test condition, Active mode

10. Package outline

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 38. Package outline SOT187-2 (PLCC44)

12. Revision history

Table 67. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LV51RB2_RC2_RD2_5	20091215	Product data sheet	-	P89LV51RB2_RC2_RD2-04
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 3: Removed sentence “However, Security lock level 4 will disable $\overline{EA}$...” for $\overline{EA}$ description. • Table 37: Second row, changed “f_{osc} / 6” to “f_{osc} / 2”. • Figure 30: Updated figure. • Figure 31: Updated figure.			
P89LV51RB2_RC2_RD2-04 (9397 750 14342)	20041202	Product data	-	P89LV51RB2_RC2_RD2-03
P89LV51RB2_RC2_RD2-03 (9397 750 14101)	20041011	Product data	-	P89LV51RB2_RC2_RD2-02
P89LV51RB2_RC2_RD2-02 (9397 750 11783)	20031113	Product data	-	P89LV51RB2_RC2_RD2-01
P89LV51RB2_RC2_RD2-01 (9397 750 11669)	20030630	Product data	ECN 853-2432 30075 dated 27 June 2003	-