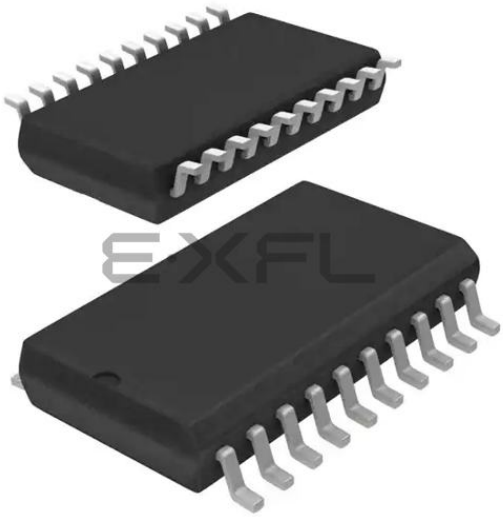

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 4x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc769hd-512

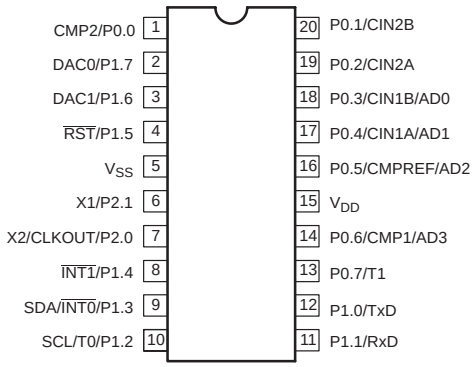
Low power, low price, low pin count (20 pin) microcontroller with 4 kB OTP 8-bit A/D, and DAC

P87LPC769

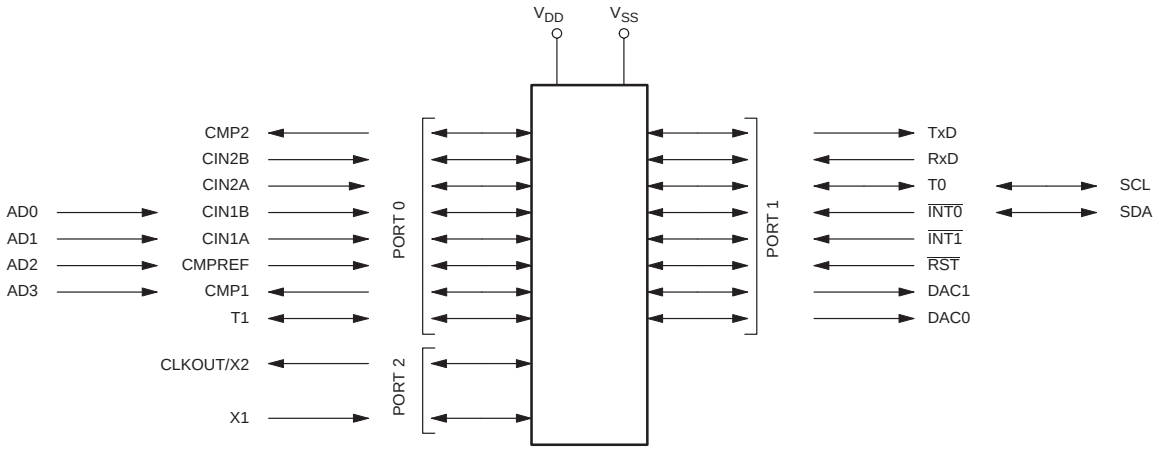
ORDERING INFORMATION

Part Number	Temperature Range °C and Package	Frequency	Drawing Number
P87LPC769HD	–40 to +125, Plastic Small Outline Package	20 MHz (5 V), 10 MHz (3 V)	SOT163–1

PIN CONFIGURATION, 20-PIN SO PACKAGE



LOGIC SYMBOL



SPECIAL FUNCTION REGISTERS

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
			E7	E6	E5	E4	E3	E2	E1	E0	
ACC*	Accumulator	E0h									00h
			C7	C6	C5	C4	C3	C2	C1	C0	
ADCON#*	A/D Control	C0h	ENADC	ENDAC1	ENDAC0	ADCI	ADCS	RCCLK	AADR1	AADR0	00h
AUXR1#	Auxiliary Function Register	A2h	KBF	BOD	BOI	–	SRST	0	–	DPS	02h[1]
			F7	F6	F5	F4	F3	F2	F1	F0	
B*	B register	F0h									00h
CMP1#	Comparator 1 control register	ACh	–	–	CE1	CP1	CN1	OE1	CO1	CMF1	00h[1]
CMP2#	Comparator 2 control register	ADh	–	–	CE2	CP2	CN2	OE2	CO2	CMF2	00h[1]
DAC0#	A/D Result/DAC0 output value	C5h									00h
DAC1#	DAC1 output value	C6h									00h
DIVM#	CPU clock divide-by-M control	95h									00h
DPTR:	Data pointer (2 bytes)										
DPH	Data pointer high byte	83h									00h
DPL	Data pointer low byte	82h									00h
			CF	CE	CD	CC	CB	CA	C9	C8	
I2CFG#*	I^2C configuration register	C8h/RD	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0	00h[1]
		C8h/WR	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0	
			DF	DE	DD	DC	DB	DA	D9	D8	
I2CON#*	I^2C control register	D8h/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–	80h[1]
		D8h/WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I2DAT#	I^2C data register	D9h/RD	RDAT	0	0	0	0	0	0	0	80h
		D9h/WR	XDAT	x	x	x	x	x	x	x	
			AF	AE	AD	AC	AB	AA	A9	A8	
IEN0*	Interrupt enable 0	A8h	EA	EWD	EBO	ES	ET1	EX1	ET0	EX0	00h
			EF	EE	ED	EC	EB	EA	E9	E8	
IEN1#*	Interrupt enable 1	E8h	ETI	–	EC1	EAD	–	EC2	EKB	EI2	00h[1]
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*	Interrupt priority 0	B8h	–	PWD	PBO	PS	PT1	PX1	PT0	PX0	00h[1]
IP0H#	Interrupt priority 0 high byte	B7h	–	PWDH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	00h[1]
			FF	FE	FD	FC	FB	FA	F9	F8	
IP1*	Interrupt priority 1	F8h	PTI	–	PC1	PAD	–	PC2	PKB	PI2	00h[1]
IP1H#	Interrupt priority 1 high byte	F7h	PTIH	–	PC1H	PADH	–	PC2H	PKBH	PI2H	00h[1]
KBI#	Keyboard Interrupt	86h									00h
			87	86	85	84	83	82	81	80	
P0*	Port 0	80h	T1	CMP1	CMPREF	CIN1A	CIN1B	CIN2A	CIN2B	CMP2	Note 2
			97	96	95	94	93	92	91	90	
P1*	Port 1	90h	DAC0	DAC1	$\overline{RST}$	$\overline{INT1}$	$\overline{INT0}$	T0	RxD	TxD	Note 2
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0h	–	–	–	–	–	–	X1	X2	Note 2
P0M1#	Port 0 output mode 1	84h	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	00h
P0M2#	Port 0 output mode 2	85h	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00H

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
P1M1#	Port 1 output mode 1	91h	(P1M1.7)	(P1M1.6)	–	(P1M1.4)	–	–	(P1M1.1)	(P1M1.0)	00h[1]
P1M2#	Port 1 output mode 2	92h	(P1M2.7)	(P1M2.6)	–	(P1M2.4)	–	–	(P1M2.1)	(P1M2.0)	00h[1]
P2M1#	Port 2 output mode 1	A4h	P2S	P1S	P0S	ENCLK	T1OE	T0OE	(P2M1.1)	(P2M1.0)	00h
P2M2#	Port 2 output mode 2	A5h	–	–	–	–	–	–	(P2M2.1)	(P2M2.0)	00h[1]
PCON	Power control register	87h	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	Note 3
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00h
PT0AD#	Port 0 digital input disable	F6h									00h
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial port control	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00h
SBUF	Serial port data buffer register	99h									xxh
SADDR#	Serial port address register	A9h									00h
SADEN#	Serial port address enable	B9h									00h
SP	Stack pointer	81h									07h
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer 0 and 1 control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TH0	Timer 0 high byte	8Ch									00h
TH1	Timer 1 high byte	8Dh									00h
TL0	Timer 0 low byte	8Ah									00h
TL1	Timer 1 low byte	8Bh									00h
TMOD	Timer 0 and 1 mode	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
WDCON#	Watchdog control register	A7h	–	–	WDOVF	WDRUN	WDCLK	WDS2	WDS1	WDS0	Note 4
WDRST#	Watchdog reset register	A6h									xxh

NOTES:
* SFRs are bit addressable.
# SFRs are modified from or added to the 80C51 SFRs.
1. Unimplemented bits in SFRs are X (unknown) at all times. Ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset value shown in the table for these bits is 0.
2. I/O port values at reset are determined by the PRHI bit in the UCFG1 configuration byte.
3. The PCON reset value is x x BOF POF–0 0 0 0b. The BOF and POF flags are not affected by reset. The POF flag is set by hardware upon power up. The BOF flag is set by the occurrence of a brownout reset/interrupt and upon power up.
4. The WDCON reset value is xx11 0000b for a Watchdog reset, xx01 0000b for all other reset causes if the watchdog is enabled, and xx00 0000b for all other reset causes if the watchdog is disabled.

RC clock frequency of 4.5 MHz (6 MHz - 25%). Minimum times for RCCLK = 1 use an RC clock frequency of 7.5 MHz (6 MHz + 25%). Nominal time assume an ideal RC clock frequency of 6 MHz and an average of 3.5 machine cycles at the CPU clock rate.

Table 1. Example A/D Conversion Times

CPU Clock Rate	RCCLK = 0	RCCLK = 1		
		minimum	nominal	maximum
32 kHz	NA	563.4 µs	659 µs	757 µs
1 MHz	186 µs	32.4 µs	39.3 µs	48.9 µs
4 MHz	46.5 µs	18.9 µs	23.6 µs	30.1 µs

Note: Do not clock ADC from the RC oscillator when MCU clock is greater than 4 MHz.

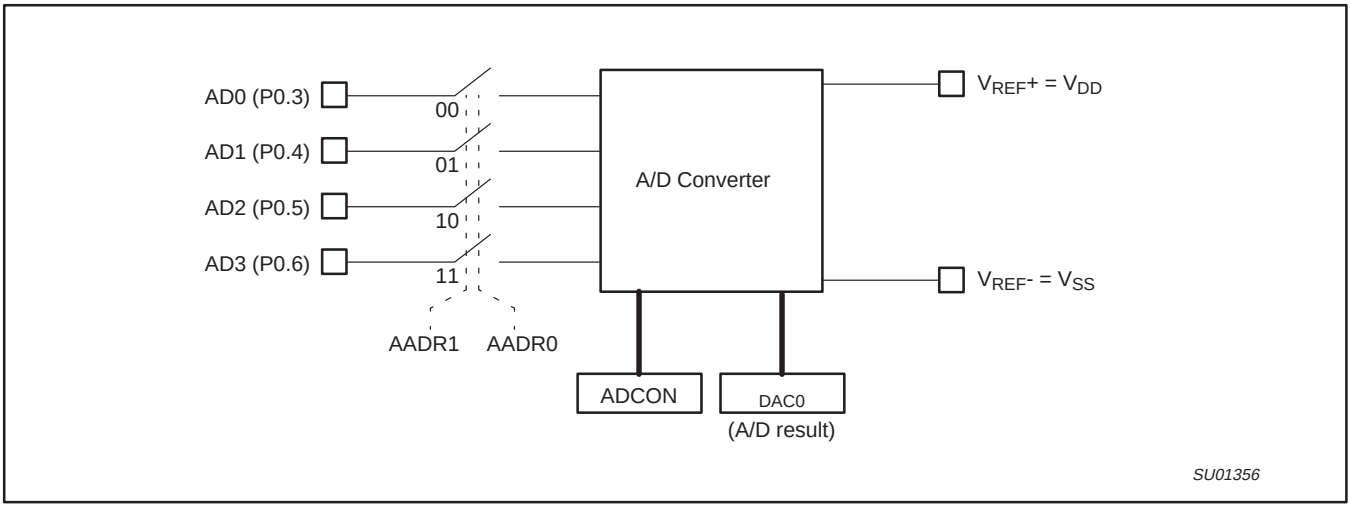


Figure 3. A/D Converter Connections

The A/D in Power Down and Idle Modes

While using the CPU clock as the A/D clock source, the Idle mode may be used to conserve power and/or to minimize system noise during the conversion. CPU operation will resume and Idle mode terminate automatically when a conversion is complete if the A/D interrupt is active. In Idle mode, noise from the CPU itself is eliminated, but noise from the oscillator and any other on-chip peripherals that are running will remain.

The CPU may be put into Power Down mode when the A/D is clocked by the on-chip RC oscillator (RCCLK=1). This mode gives the best possible A/D accuracy by eliminating most on-chip noise sources.

If the Power Down mode is entered while the A/D is running from the CPU clock (RCCLK=0), the A/D will abort operation and will not wake up the CPU. The contents of DAC0 will be invalid when operation does resume.

When an A/D conversion is started, Power Down or Idle mode must be activated within two machine cycles in order to have the most accurate A/D result. These two machine cycles are counted at the CPU clock rate. When using the A/D with either Power Down or Idle mode, care must be taken to insure that the CPU is not restarted by another interrupt until the A/D conversion is complete. The possible causes of wakeup are different in Power Down and Idle modes.

A/D accuracy is also affected by noise generated elsewhere in the application, power supply noise, and power supply regulation. Since the P87LPC769 power pins are also used as the A/D reference and supply, the power supply has a very direct affect on the accuracy of A/D readings. Using the A/D without Power Down mode while the clock is divided through the use of CLKR or DIVM has an adverse effect on A/D accuracy.

Code Examples for the A/D

The first piece of sample code shows an example of port configuration for use with the A/D. This example sets up the pins so that all four A/D channels may be used. Port configuration for analog functions is described in the section Analog Functions.

```
; Set up port pins for A/D conversion, without affecting other pins.
   mov    PT0AD,#78h          ; Disable digital inputs on A/D input pins.
   anl    P0M2,#87h           ; Disable digital outputs on A/D input pins.
   orl    P0M1,#78h           ; Disable digital outputs on A/D input pins.
```

Following is an example of using the A/D with interrupts. The routine ADStart begins an A/D conversion using the A/D channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization.

The interrupt handler routine reads the conversion value and returns it in memory address ADResult. The interrupt should be enabled prior to starting the conversion.

```
; Start A/D conversion.
ADStart:
   orl    ADCON,A             ; Add in the new channel number.
   setb   ADCS                ; Start an A/D conversion.
;  orl    PCON,#01h           ; The CPU could be put into Idle mode here.
;  orl    PCON,#02h           ; The CPU could be put into Power Down mode here if RCCLK = 1.
   ret

; A/D interrupt handler.
ADInt:
   push   ACC                 ; Save accumulator.
   mov    A,DAC0              ; Get A/D result,
   mov    ADResult,A          ;   and save it in memory.
   clr    ADCI                ; Clear the A/D completion flag.
   anl    ADCON,#0fch         ; Clear the A/D channel number.
   pop    ACC                 ; Restore accumulator.
   reti
```

Following is an example of using the A/D with polling. An A/D conversion is started using the channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization. The conversion result is returned in the accumulator.

```
ADRead:
   orl    ADCON,A             ; Add in the new channel number.
   setb   ADCS                ; Start A/D conversion.
ADChk:
   jnb    ADCI,ADChk          ; Wait for ADCI to be set.
   mov    A,DAC0              ; Get A/D result.
   clr    ADCI                ; Clear the A/D completion flag.
   anl    ADCON,#0fch         ; Clear the A/D channel number.
   ret
```

Digital to Analog Converter (DAC) Outputs

The P87LPC769 provides a two channel, 8-bit DAC function. DAC0 is also a part of the A/D Converter and it should not be enabled while the A/D is active. Digital outputs must be disabled on the DAC output pins while the corresponding DAC is enabled, as described in the section Analog Functions.

The DACs use the power supply as the references: V_{DD} as the upper reference and V_{SS} as the lower reference. The DAC output is generated by a tap from a resistor ladder and is not buffered. The maximum resistance to V_{DD} or V_{SS} from a DAC output is 10kΩ. Care must be taken with the loading of the DAC outputs in order to avoid distortion of the output voltage. DAC accuracy is affected by noise generated on-chip and elsewhere in the application. Since the P87LPC769 power pins are used for the DAC references, the power supply also affects the accuracy of the DAC outputs.

The ideal DAC output may be calculated as follows:

$$\text{Result} = (\text{DAC Value} + 0.5) \times \frac{V_{DD} - V_{SS}}{256}$$

where DAC value is the contents of the relevant DAC register: DAC0 or DAC1.

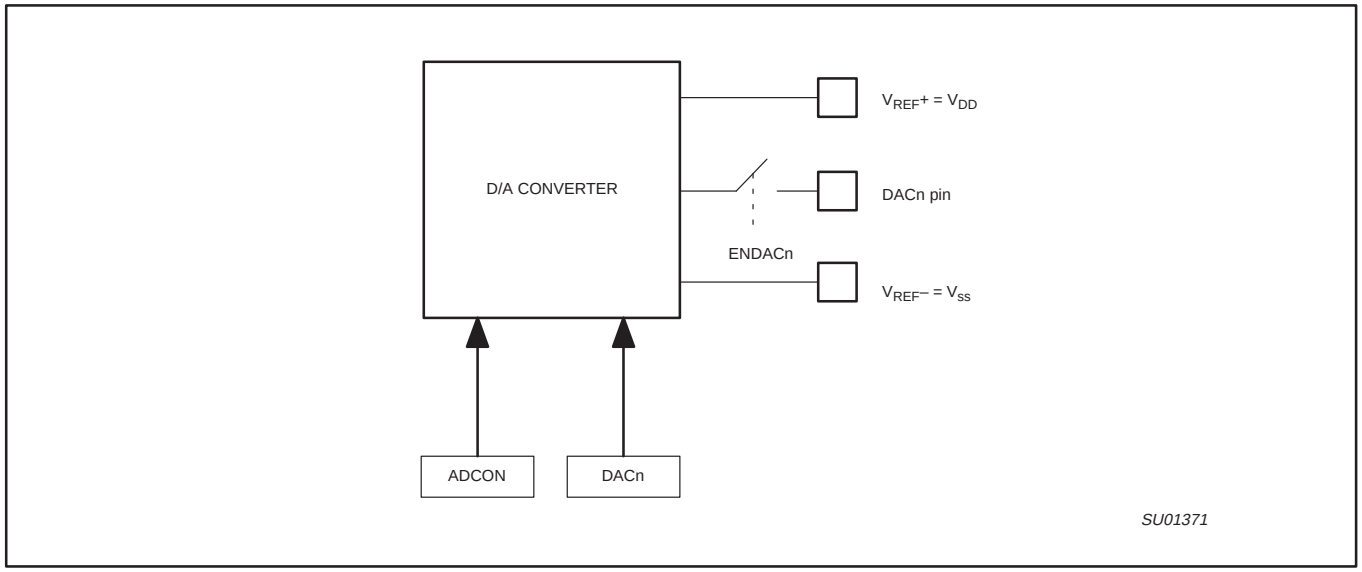


Figure 4. DAC Block Diagram

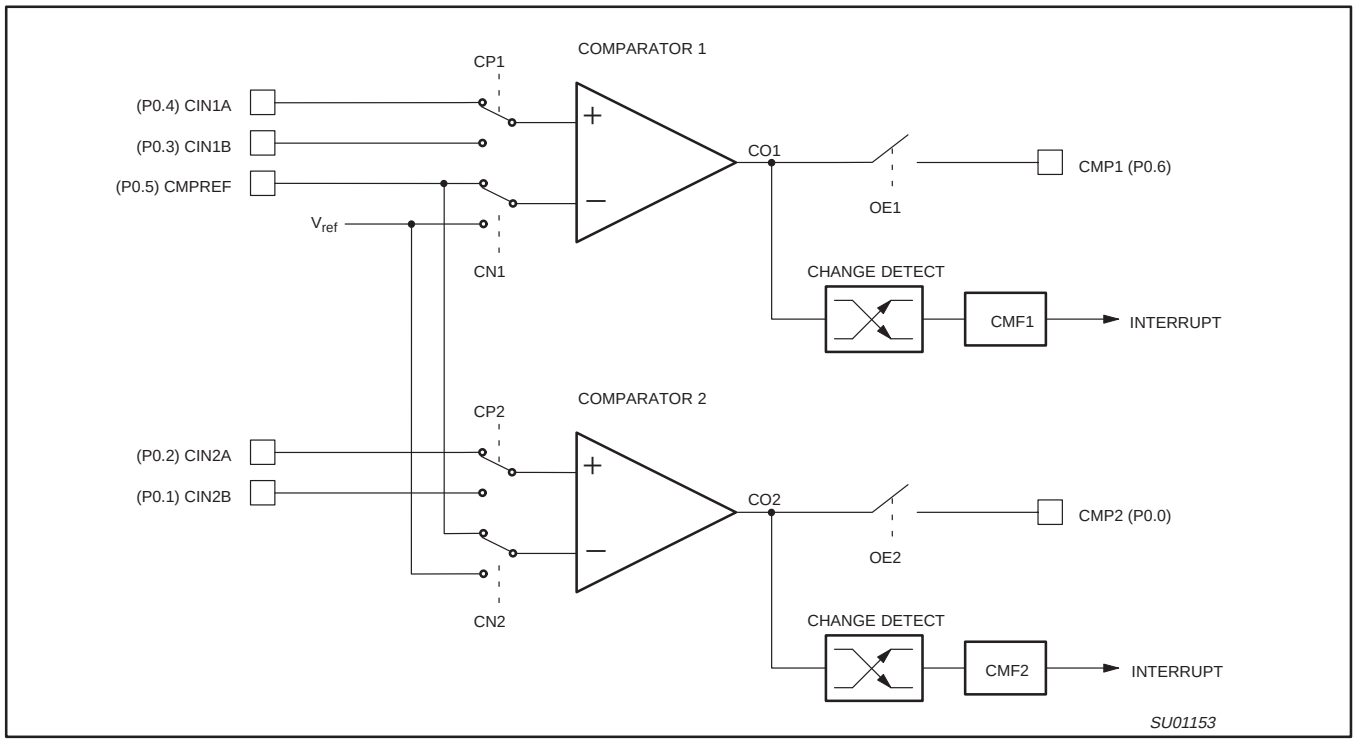


Figure 6. Comparator Input and Output Connections

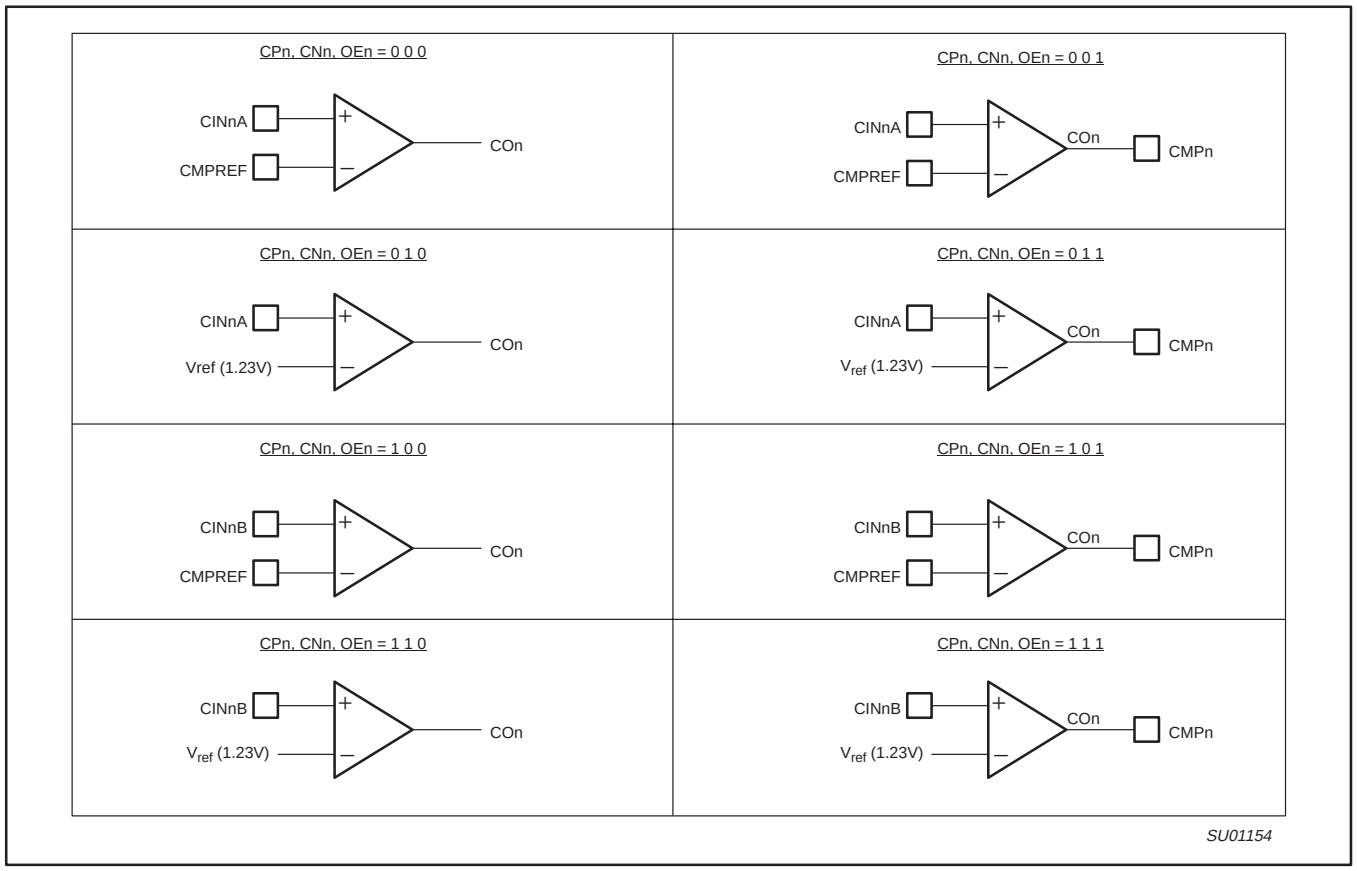


Figure 7. Comparator Configurations

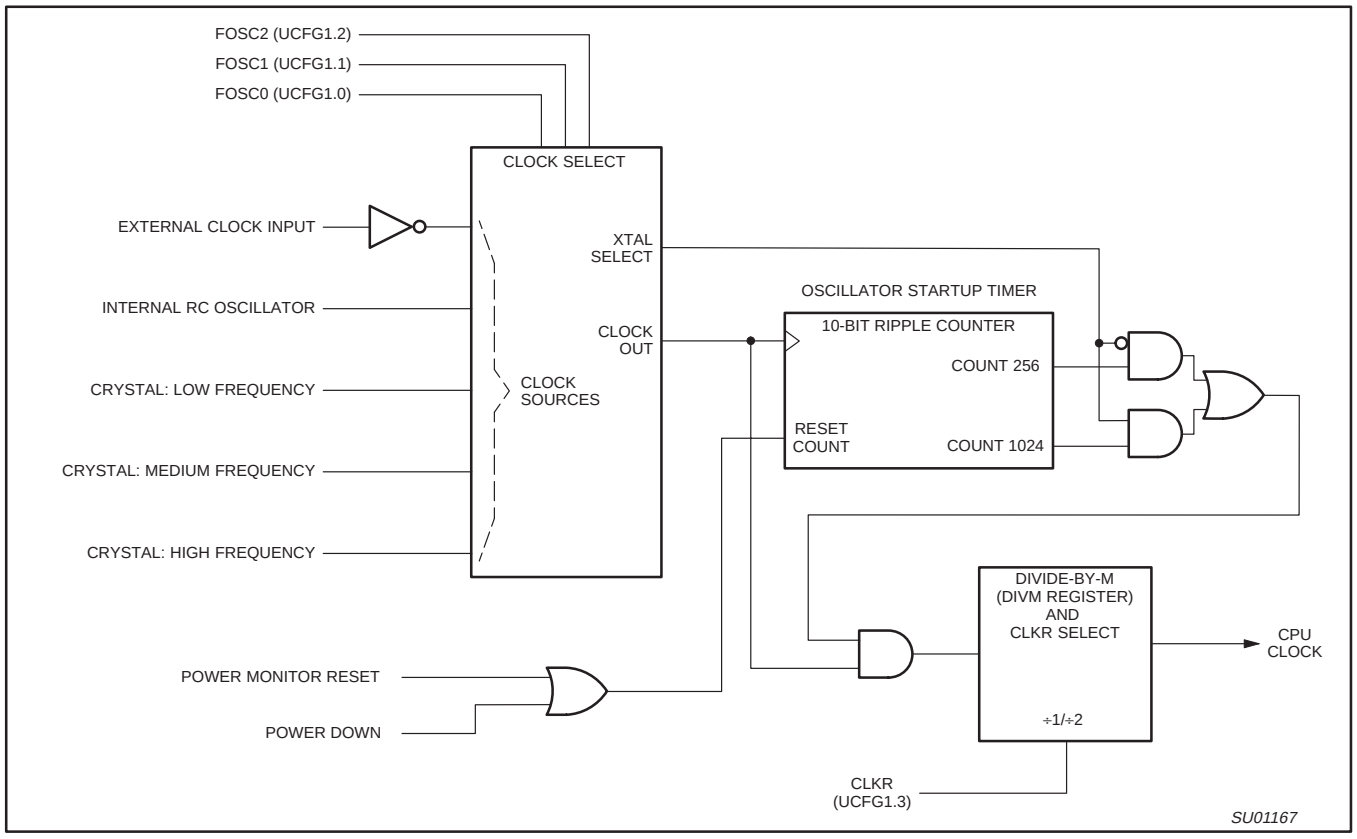


Figure 21. Block Diagram of Oscillator Control

CPU Clock Modification: CLKR and DIVM

For backward compatibility, the CLKR configuration bit allows setting the P87LPC769 instruction and peripheral timing to match standard 80C51 timing by dividing the CPU clock by two. Default timing for the P87LPC769 is 6 CPU clocks per machine cycle while standard 80C51 timing is 12 clocks per machine cycle. This division also applies to peripheral timing, allowing 80C51 code that is oscillator frequency and/or timer rate dependent. The CLKR bit is located in the EPROM configuration register UCFG1, described under EPROM Characteristics

In addition to this, the CPU clock may be divided down from the oscillator rate by a programmable divider, under program control. This function is controlled by the DIVM register. If the DIVM register is set to zero (the default value), the CPU will be clocked by either the unmodified oscillator rate, or that rate divided by two, as determined by the previously described CLKR function.

When the DIVM register is set to some value N (between 1 and 255), the CPU clock is divided by 2 * (N + 1). Clock division values from 4 through 512 are thus possible. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption, in a manner similar to Idle mode. By dividing the clock, the CPU can retain the ability to respond to events other than those that can cause interrupts (i.e. events that allow exiting the Idle mode) by executing its normal program at a lower rate. This can allow bypassing the oscillator startup time in cases where Power Down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

Power Monitoring Functions

The P87LPC769 incorporates power monitoring functions designed to prevent incorrect operation during initial power up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-On Detect and Brownout Detect.

Brownout Detection

The Brownout Detect function allows preventing the processor from failing in an unpredictable manner if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt by setting the BOI bit in the AUXR1 register (AUXR1.5).

The P87LPC769 has a Brownout level of 3.8 V. When V_{DD} drops below the selected voltage, the brownout detector triggers and remains active until V_{DD} is returns to a level above the Brownout Detect voltage. When Brownout Detect causes a processor reset, that reset remains active as long as V_{DD} remains below the Brownout Detect voltage. When Brownout Detect generates an interrupt, that interrupt occurs once as V_{DD} crosses from above to below the Brownout Detect voltage. For the interrupt to be processed, the interrupt system and the BOI interrupt must both be enabled (via the EA and EBO bits in IEN0).

When Brownout Detect is activated, the BOF flag in the PCON register is set so that the cause of processor reset may be determined by software. This flag will remain set until cleared by software.

For correct activation of Brownout Detect, the V_{DD} fall time must be no faster than 50 mV/µs. When V_{DD} is restored, is should not rise faster than 2 mV/µs in order to insure a proper reset.

The brownout voltage (BOV) bit in the EPROM configuration register UCFG1 must be programmed to a zero.

If the Brownout Detect function is not required in an application, it may be disabled, thus saving power. Brownout Detect is disabled by setting the control bit BOD in the AUXR1 register (AUXR1.6).

Power On Detection

The Power On Detect has a function similar to the Brownout Detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout Detect can work. When this feature is activated, the POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain set until cleared by software.

Power Reduction Modes

The P87LPC769 supports Idle and Power Down modes of power reduction.

Idle Mode

The Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or Reset may terminate Idle mode. Idle mode is entered by setting the IDL bit in the PCON register (see Figure 22).

Power Down Mode

The Power Down mode stops the oscillator in order to absolutely minimize power consumption. Power Down mode is entered by setting the PD bit in the PCON register (see Figure 22).

The processor can be made to exit Power Down mode via Reset or one of the interrupt sources shown in Table 5. This will occur if the interrupt is enabled and its priority is higher than any interrupt currently in progress.

In Power Down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power Down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is recommended to wake up the processor via Reset in this case. V_{DD} must be raised to within the operating range before the Power Down mode is exited. Since the watchdog timer has a separate oscillator, it may reset the processor upon overflow if it is running during Power Down.

Note that if the Brownout Detect reset is enabled, the processor will be put into reset as soon as V_{DD} drops below the brownout voltage. If Brownout Detect is configured as an interrupt and is enabled, it will wake up the processor from Power Down mode when V_{DD} drops below the brownout voltage.

When the processor wakes up from Power Down mode, it will start the oscillator immediately and begin execution when the oscillator is stable. Oscillator stability is determined by counting 1024 CPU clocks after start-up when one of the crystal oscillator configurations is used, or 256 clocks after start-up for the internal RC or external clock input configurations.

Some chip functions continue to operate and draw power during Power Down mode, increasing the total power used during Power Down. These include the Brownout Detect, Watchdog Timer, Comparators, and A/D converter.

PCON Address: 87h

Not Bit Addressable

Reset Value:
- 30h for a Power On reset
- 20h for a Brownout reset
- 00h for other reset sources

7	6	5	4	3	2	1	0
SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL

BIT	SYMBOL	FUNCTION
PCON.7	SMOD1	When set, this bit doubles the UART baud rate for modes 1, 2, and 3.
PCON.6	SMOD0	This bit selects the function of bit 7 of the SCON SFR. When 0, SCON.7 is the SM0 bit. When 1, SCON.7 is the FE (Framing Error) flag. See Figure 26 for additional information.
PCON.5	BOF	Brown Out Flag. Set automatically when a brownout reset or interrupt has occurred. Also set at power on. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.4	POF	Power On Flag. Set automatically when a power-on reset has occurred. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.3	GF1	General purpose flag 1. May be read or written by user software, but has no effect on operation.
PCON.2	GF0	General purpose flag 0. May be read or written by user software, but has no effect on operation.
PCON.1	PD	Power Down control bit. Setting this bit activates Power Down mode operation. Cleared when the Power Down mode is terminated (see text).
PCON.0	IDL	Idle mode control bit. Setting this bit activates Idle mode operation. Cleared when the Idle mode is terminated (see text).

SU01168

Figure 22. Power Control Register (PCON)

Timer/Counters

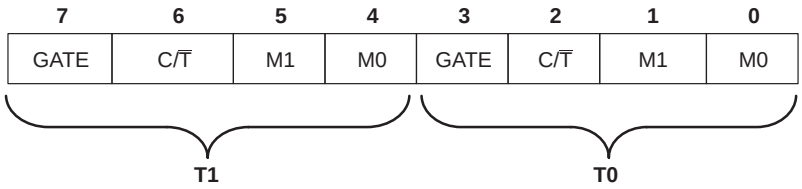
The P87LPC769 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters (see Figure 25). An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency. Refer to the section Enhanced CPU for a description of the CPU clock.

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The “Timer” or “Counter” function is selected by control bits C/T in the Special Function Register TMOD. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

TMOD Address: 89h Reset Value: 00h
Not Bit Addressable



BIT	SYMBOL	FUNCTION
TMOD.7	GATE	Gating control for Timer 1. When set, Timer/Counter is enabled only while the $\overline{INT1}$ pin is high and the TR1 control pin is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
TMOD.6	C/$\overline{T}$	Timer or Counter Selector for Timer 1. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T1 input pin).
TMOD.5, 4	M1, M0	Mode Select for Timer 1 (see table below).
TMOD.3	GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is high and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
TMOD.2	C/$\overline{T}$	Timer or Counter Selector for Timer 0. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T0 input pin).
TMOD.1, 0	M1, M0	Mode Select for Timer 0 (see table below).
	M1, M0	Timer Mode
	0 0	8048 Timer “TLn” serves as 5-bit prescaler.
	0 1	16-bit Timer/Counter “THn” and “TLn” are cascaded; there is no prescaler.
	1 0	8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows.
	1 1	Timer 0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by the Timer 1 control bits (see text). Timer 1 in this mode is stopped.

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Figure 25. Timer/Counter Mode Control Register (TMOD)

Mode 1
Mode 1 is the same as Mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 28

Mode 2
Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 29. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

Mode 3
When Timer 1 is in Mode 3 it is stopped. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 on Timer 0 is shown in Figure 30. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the “Timer 1” interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in Mode 3, an P87LPC769 can look like it has three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

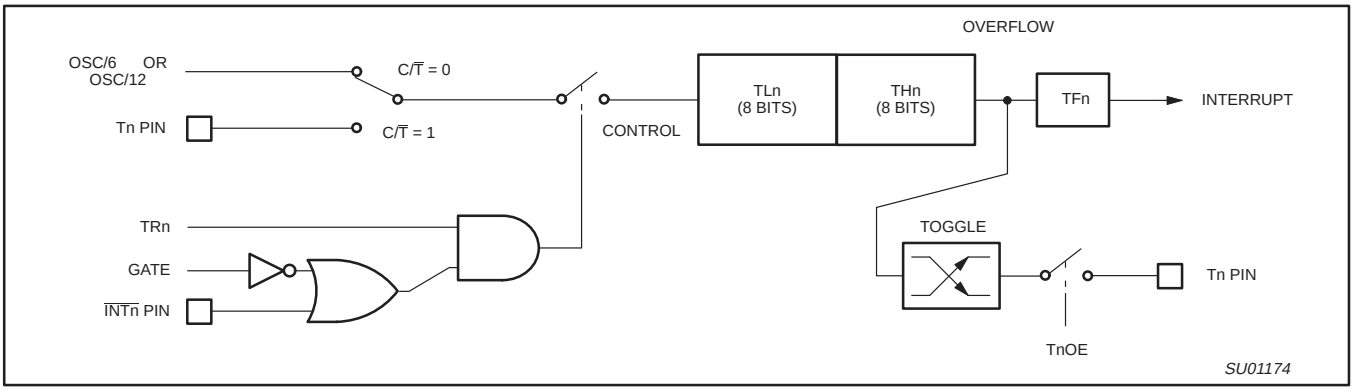

Figure 28. Timer/Counter 0 or 1 in Mode 1 (16-Bit Counter)

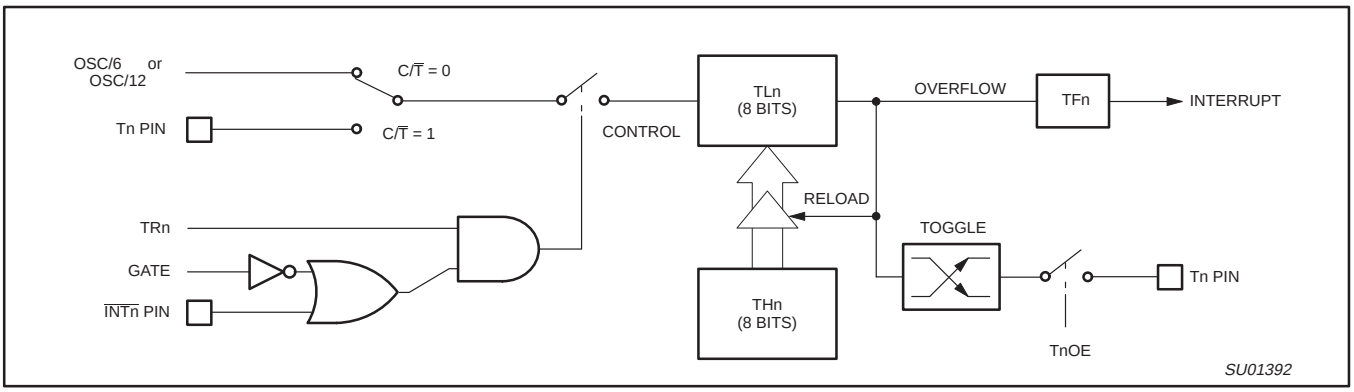

Figure 29. Timer/Counter 0 or 1 in Mode 2 (8-Bit Auto-Reload)

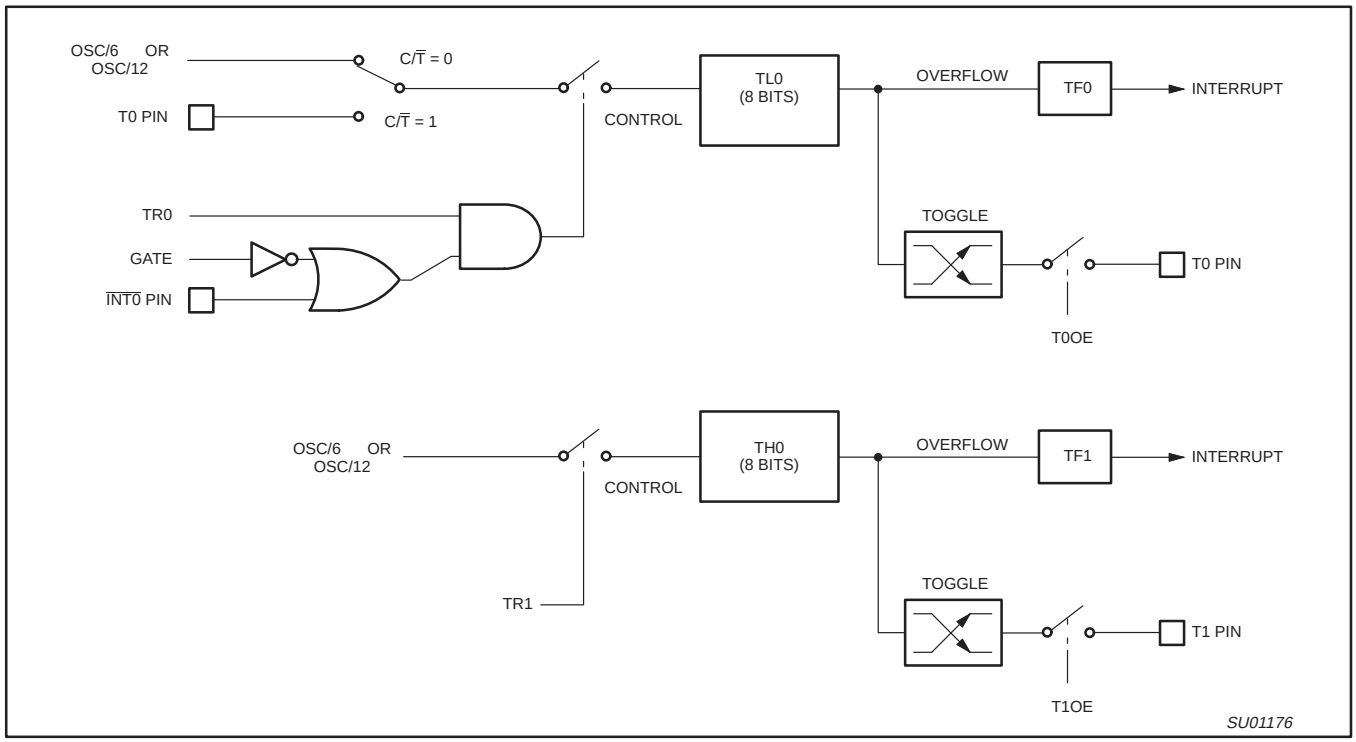

Figure 30. Timer/Counter 0 Mode 3 (Two 8-Bit Counters)

Timer Overflow Toggle Output
Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits T0OE and T1OE in the P2M1 register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

UART

The P87LPC769 includes an enhanced 80C51 UART. The baud rate source for the UART is timer 1 for modes 1 and 3, while the rate is fixed in modes 0 and 2. Because CPU clocking is different on the P87LPC769 than on the standard 80C51, baud rate calculation is somewhat different. Enhancements over the standard 80C51 UART include Framing Error detection and automatic address recognition.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the SBUF register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, the first byte will be lost. The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can be operated in 4 modes:

Mode 0
Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at 1/6 of the CPU clock frequency.

Mode 1
10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate.

Mode 2
11 bits are transmitted (through TxD) or received (through RxD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

Mode 3
11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Serial Port Control Register (SCON)

The serial port control and status register is the Special Function Register SCON, shown in Figure 31. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

The Framing Error bit (FE) allows detection of missing stop bits in the received data stream. The FE bit shares the bit position SCON.7 with the SM0 bit. Which bit appears in SCON at any particular time is determined by the SMOD0 bit in the PCON register. If SMOD0 = 0, SCON.7 is the SM0 bit. If SMOD0 = 1, SCON.7 is the FE bit. Once set, the FE bit remains set until it is cleared by software. This allows detection of framing errors for a group of characters without the need for monitoring it for every character individually.

SCON Address: 98h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

BIT	SYMBOL	FUNCTION
SCON.7	FE	Framing Error. This bit is set by the UART receiver when an invalid stop bit is detected. Must be cleared by software. The SMOD0 bit in the PCON register must be 1 for this bit to be accessible. See SM0 bit below.
SCON.7	SM0	With SM1, defines the serial port mode. The SMOD0 bit in the PCON register must be 0 for this bit to be accessible. See FE bit above.
SCON. 6	SM1	With SM0, defines the serial port mode (see table below).

SM0, SM1	UART Mode	Baud Rate
0 0	0: shift register	CPU clock/6
0 1	1: 8-bit UART	Variable (see text)
1 0	2: 9-bit UART	CPU clock/32 or CPU clock/16
1 1	3: 9-bit UART	Variable (see text)

SCON.5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.
SCON.4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
SCON.3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
SCON.2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
SCON.1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
SCON.0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

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Figure 31. Serial Port Control Register (SCON)

More About UART Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/6 the CPU clock frequency. Figure 32 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P1.1 and also enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after “write to SBUF.” Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 t o the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P1.1 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About UART Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the P87LPC769 the baud rate is determined by the Timer 1 overflow rate. Figure 33 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.: 1. R1 = 0, and 2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

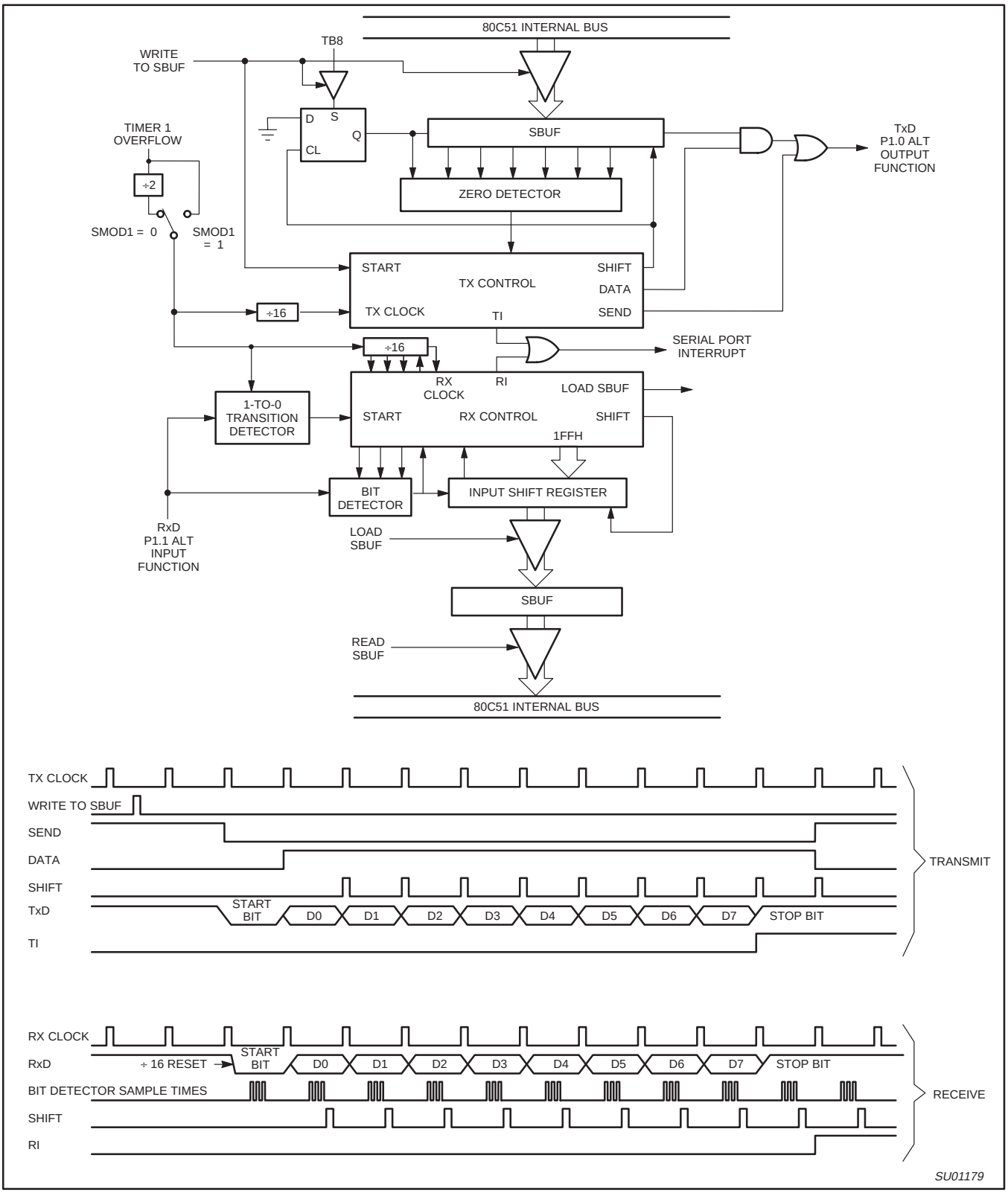

Figure 33. Serial Port Mode 1

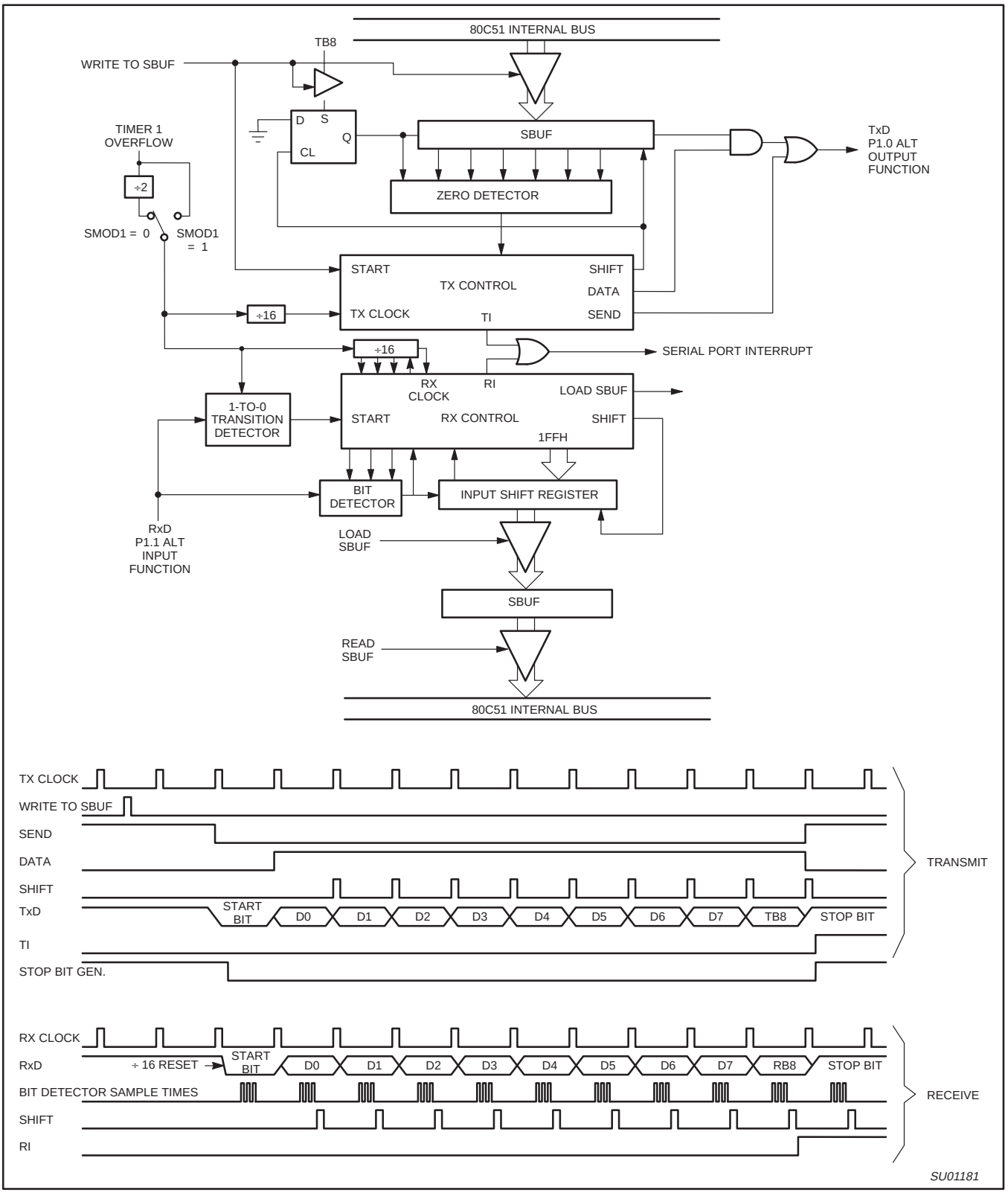

Figure 35. Serial Port Mode 3

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0 SADDR = 1100 0000
SADEN = 1111 1101
Given = 1100 00X0

Slave 1 SADDR = 1100 0000
SADEN = 1111 1110
Given = 1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0

Slave 1 SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X

Slave 2 SADDR = 1110 0000
SADEN = 1111 1100
Given = 1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don’t-cares. In most cases, interpreting the don’t-cares as ones, the broadcast address will be FF hexadecimal. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all “don’t cares” as well as a Broadcast address of all “don’t cares”. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

Watchdog Timer

When enabled via the WDTE configuration bit, the watchdog timer is operated from an independent, fully on-chip oscillator in order to provide the greatest possible dependability. When the watchdog feature is enabled, the timer must be fed regularly by software in order to prevent it from resetting the CPU, and it cannot be turned off. When disabled as a watchdog timer (via the WDTE bit in the UCFG1 configuration register), it may be used as an interval timer and may generate an interrupt. The watchdog timer is shown in Figure 36.

The watchdog timeout time is selectable from one of eight values, nominal times range from 16 milliseconds to 2.1 seconds. The frequency tolerance of the independent watchdog RC oscillator is ±37%. The timeout selections and other control bits are shown in Figure 37. When the watchdog function is enabled, the WDCON register may be written once during chip initialization in order to set the watchdog timeout time. The recommended method of initializing the WDCON register is to first feed the watchdog, then write to WDCON to configure the WDS2–0 bits. Using this method, the watchdog initialization may be done any time within 10 milliseconds after startup without a watchdog overflow occurring before the initialization can be completed.

Since the watchdog timer oscillator is fully on-chip and independent of any external oscillator circuit used by the CPU, it intrinsically serves as an oscillator fail detection function. If the watchdog feature is enabled and the CPU oscillator fails for any reason, the watchdog timer will time out and reset the CPU.

When the watchdog function is enabled, the timer is deactivated temporarily when a chip reset occurs from another source, such as a power on reset, brownout reset, or external reset.

Watchdog Feed Sequence

If the watchdog timer is running, it must be fed before it times out in order to prevent a chip reset from occurring. The watchdog feed sequence consists of first writing the value 1Eh, then the value E1h to the WDRST register. An example of a watchdog feed sequence is shown below.

```
WDFeed:
   mov   WDRST,#1eh   ; First part of watchdog feed sequence.
   mov   WDRST,#0e1h  ; Second part of watchdog feed sequence.
```

The two writes to WDRST do not have to occur in consecutive instructions. An incorrect watchdog feed sequence does not cause any immediate response from the watchdog timer, which will still time out at the originally scheduled time if a correct feed sequence does not occur prior to that time.

After a chip reset, the user program has a limited time in which to either feed the watchdog timer or change the timeout period. When a low CPU clock frequency is used in the application, the number of instructions that can be executed before the watchdog overflows may be quite small.

Watchdog Reset

If a watchdog reset occurs, the internal reset is active for approximately one microsecond. If the CPU clock was still running, code execution will begin immediately after that. If the processor was in Power Down mode, the watchdog reset will start the oscillator and code execution will resume after the oscillator is stable.

EPROM Characteristics

Programming of the EPROM on the P87LPC769 is accomplished with a serial programming method. Commands, addresses, and data are transmitted to and from the device on two pins after programming mode is entered. Serial programming allows easy implementation of in-circuit programming of the P87LPC769 in an application board. Details of the programming algorithm may be found in a separate document that is available on the Philips web site at:
http://www.semiconductors.philips.com/mcu/support/progspecs/

The P87LPC769 contains three signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes designate the device as an P87LPC769 manufactured by Philips. The signature bytes may be read by the user program at addresses FC30h, FC31h and FC60h with the MOVC instruction, using the DPTR register for addressing.

A special user data area is also available for access via the MOVC instruction at addresses FCE0h through FCFFh. This "customer code" space is programmed in the same manner as the main code EPROM and may be used to store a serial number, manufacturing date, or other application information.

32-Byte Customer Code Space

A small supplemental EPROM space is reserved for use by the customer in order to identify code revisions, store checksums, add a serial number to each device, or any other desired use. This area exists in the code memory space from addresses FCE0h through FCFFh. Code execution from this space is not supported, but it may be read as data through the use of the MOVC instruction with the appropriate addresses. The memory may be programmed at the same time as the rest of the code memory and UCFG bytes are programmed.

System Configuration Bytes

A number of user configurable features of the P87LPC769 must be defined at power up and therefore cannot be set by the program after start of execution. Those features are configured through the use of two EPROM bytes that are programmed in the same manner as the EPROM program space. The contents of the two configuration bytes, UCFG1 and UCFG2, are shown in Figures 39 and 40. The values of these bytes may be read by the program through the use of the MOVX instruction at the addresses shown in the figure.

UCFG1 Address: FD00h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
WDTE	RPD	PRHI	BOV	CLKR	FOSC2	FOSC1	FOSC0

BIT	SYMBOL	FUNCTION
UCFG1.7	WDTE	Watchdog timer enable. When programmed (0), disables the watchdog timer. The timer may still be used to generate an interrupt.
UCFG1.6	RPD	Reset pin disable. When 1 disables the reset function of pin P1.5, allowing it to be used as an input only port pin.
UCFG1.5	PRHI	Port reset high. When 1, ports reset to a high state. When 0, ports reset to a low state.
UCFG1.4	BOV	This bit should always be programmed to a zero.
UCFG1.3	CLKR	Clock rate select. When 0, the CPU clock rate is divided by 2. This results in machine cycles taking 12 CPU clocks to complete as in the standard 80C51. For full backward compatibility, this division applies to peripheral timing as well.
UCFG1.2–0	FOSC2–FSOC0	CPU oscillator type select. See Oscillator section for additional information. Combinations other than those shown below should not be used. They are reserved for future use.
	FOSC2–FOSC0	Oscillator Configuration
	1 1 1	External clock input on X1 (default setting for an unprogrammed part).
	0 1 1	Internal RC oscillator, 6 MHz ±25%.
	0 1 0	Low frequency crystal, 20 kHz to 100 kHz.
	0 0 1	Medium frequency crystal or resonator, 100 kHz to 4 MHz.
	0 0 0	High frequency crystal or resonator, 4 MHz to 20 MHz.

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Figure 39. EPROM System Configuration Byte 1 (UCFG1)

UCFG2 Address: FD01h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
SB2	SB1	—	—	—	—	—	—

BIT	SYMBOL	FUNCTION
UCFG2.7, 6	SB2, SB1	EPROM security bits. See table entitled, “EPROM Security Bits” for details.
UCFG2.5–0	—	Reserved for future use.

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Figure 40. EPROM System Configuration Byte 2 (UCFG2)

Security Bits
When neither of the security bits are programmed, the code in the EPROM can be verified. When only security bit 1 is programmed, all further programming of the EPROM is disabled. At that point, only security bit 2 may still be programmed. When both security bits are programmed, EPROM verify is also disabled.

Table 12. EPROM Security Bits

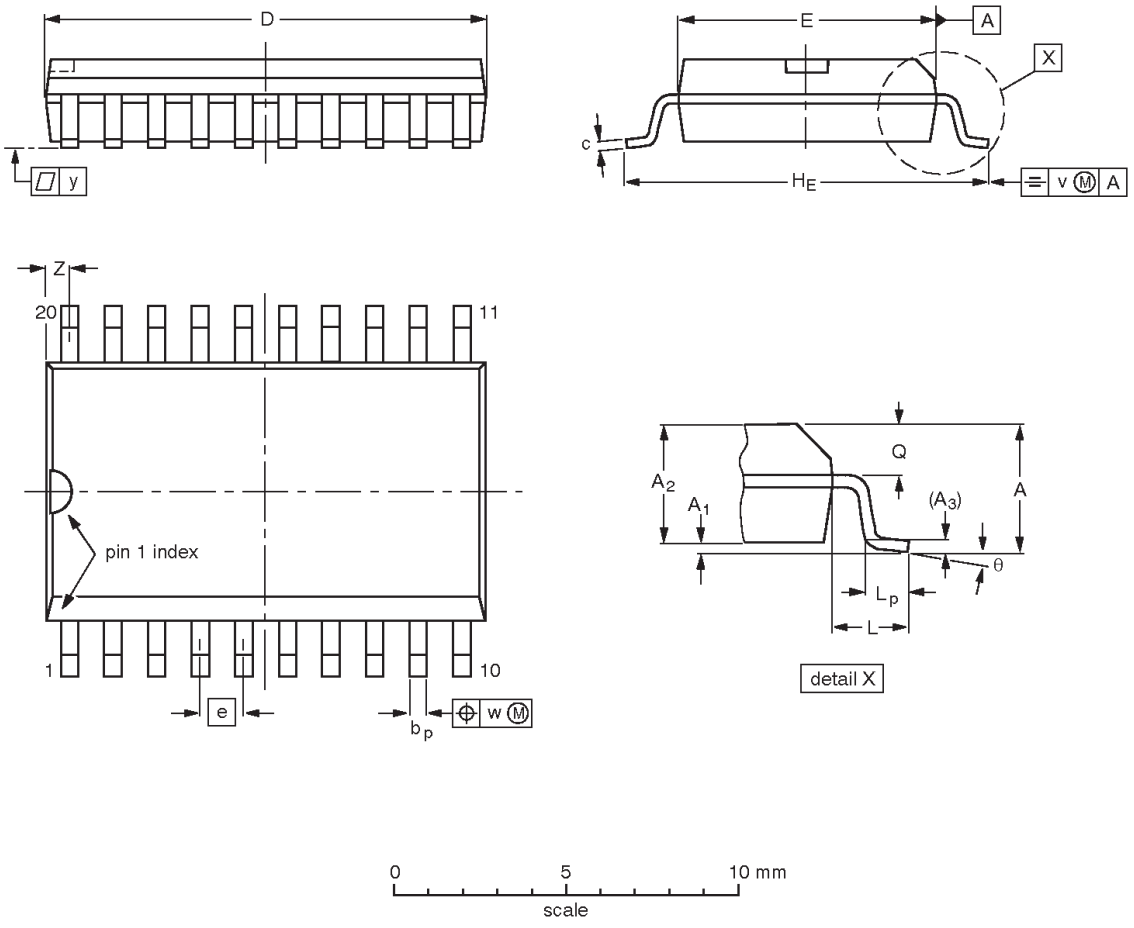
SB2	SB1	Protection Description
1	1	Both security bits unprogrammed. No program security features enabled. EPROM is programmable and verifiable.
1	0	Only security bit 1 programmed. Further EPROM programming is disabled. Security bit 2 may still be programmed.
0	1	Only security bit 2 programmed. This combination is not supported.
0	0	Both security bits programmed. All EPROM verification and programming are disabled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{RST}/V_{PP}$ pin to V_{SS}	0 to +11.0	V
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5V	V
Maximum I_{OL} per I/O pin	20	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27