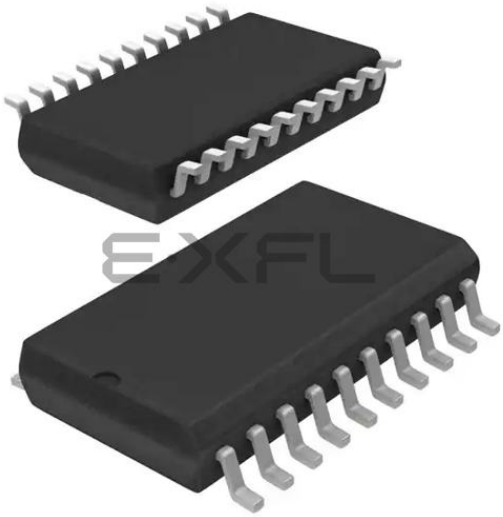

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 4x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc769hd-518

ADCON Address: C0h

Bit addressable

Reset Value: 00h

7	6	5	4	3	2	1	0
ENADC	ENDAC1	ENDAC0	ADCI	ADCS	RCCLK	AADR1	AADR0

BIT	SYMBOL	FUNCTION
ADCON.7	ENADC	When ENADC = 1, the A/D is enabled and conversions may take place. Must be set 10 microseconds before a conversion is started. ENADC cannot be cleared while ADCS or ADCI are 1.
ADCON.6	ENDAC1	When ENDAC=1, DAC1 is enabled to provide an analog output voltage. Refer to the section Digital to Analog Converter (DAC) Outputs for details.
ADCON.5	ENDAC0	When ENDAC=1, DAC0 is enabled to provide an analog output voltage. Writable while ADCS and ADCI are 0. Refer to the section Digital to Analog Converter (DAC) Outputs for details. ENADC and ENDAC0 should not be set at the same time.
ADCON.4	ADCI	A/D conversion complete/interrupt flag. This flag is set when an A/D conversion is completed. This bit will cause a hardware interrupt if enabled and of sufficient priority. Must be cleared by software.
ADCON.3	ADCS	A/D start. Setting this bit by software starts the conversion of the selected A/D input. ADCS remains set while the A/D conversion is in progress and is cleared automatically upon completion. While ADCS or ADCI are one, new start commands are ignored.
	ADCI, ADCS	A/D Status
	0 0	A/D not busy, a conversion can be started.
	0 1	A/D busy, the start of a new conversion is blocked.
	1 0	An A/D conversion is complete. ADCI must be cleared prior to starting a new conversion.
	1 1	An A/D conversion is complete. ADCI must be cleared prior to starting a new conversion. This state exists for one machine cycle as an A/D conversion is completed.
ADCON.2	RCCLK	When RCCLK = 0, the CPU clock is used as the A/D clock. When RCCLK = 1, the internal RC oscillator is used as the A/D clock. This bit is writable while ADCS and ADCI are 0.
ADCON.1, 0	AADR1,0	Along with AADR0, selects the A/D channel to be converted. These bits can only be written while ADCS and ADCI are 0.
	AADR1, AADR0	A/D Input Selected
	0 0	AD0 (P0.3).
	0 1	AD1 (P0.4).
	1 0	AD2 (P0.5).
	1 1	AD3 (P0.6).

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Figure 2. A/D Control Register (ADCON)

A/D Timing

The A/D may be clocked in one of two ways. The default is to use the CPU clock as the A/D clock source. When used in this manner, the A/D completes a conversion in 31 machine cycles. The A/D may be operated up to the maximum CPU clock rate of 20 MHz, giving a conversion time of 9.3 μs. The formula for calculating A/D conversion time when the CPU clock runs the A/D is: 186 μs / CPU clock rate (in MHZ). To obtain accurate A/D conversion results, the CPU clock must be at least 1 MHz.

The A/D may also be clocked by the on-chip RC oscillator, even if the RC oscillator is not used as the CPU clock. This is accomplished by setting the RCCLK bit in ADCON. This arrangement has several advantages. First, the A/D conversion time is faster at lower CPU clock rates. Also, the CPU may be run at speeds below 1 MHz without affecting A/D accuracy. Finally, the Power Down mode may be used to completely shut down the CPU and its oscillator, along with other peripheral functions, in order to obtain the best possible A/D accuracy. This should not be used if the MCU uses an external clock source greater than 4 MHz.

When the A/D is operated from the RCCLK while the CPU is running from another clock source, 3 or 4 machine cycles are used to synchronize A/D operation. The time can range from a minimum of 3 machine cycles (at the CPU clock rate) + 108 RC clocks to a maximum of 4 machine cycles (at the CPU clock rate) + 112 RC clocks.

Example A/D conversion times at various CPU clock rates are shown in Table 1. In Table 1, maximum times for RCCLK = 1 use an

RC clock frequency of 4.5 MHz (6 MHz - 25%). Minimum times for RCCLK = 1 use an RC clock frequency of 7.5 MHz (6 MHz + 25%). Nominal time assume an ideal RC clock frequency of 6 MHz and an average of 3.5 machine cycles at the CPU clock rate.

Table 1. Example A/D Conversion Times

CPU Clock Rate	RCCLK = 0	RCCLK = 1		
		minimum	nominal	maximum
32 kHz	NA	563.4 µs	659 µs	757 µs
1 MHz	186 µs	32.4 µs	39.3 µs	48.9 µs
4 MHz	46.5 µs	18.9 µs	23.6 µs	30.1 µs

Note: Do not clock ADC from the RC oscillator when MCU clock is greater than 4 MHz.

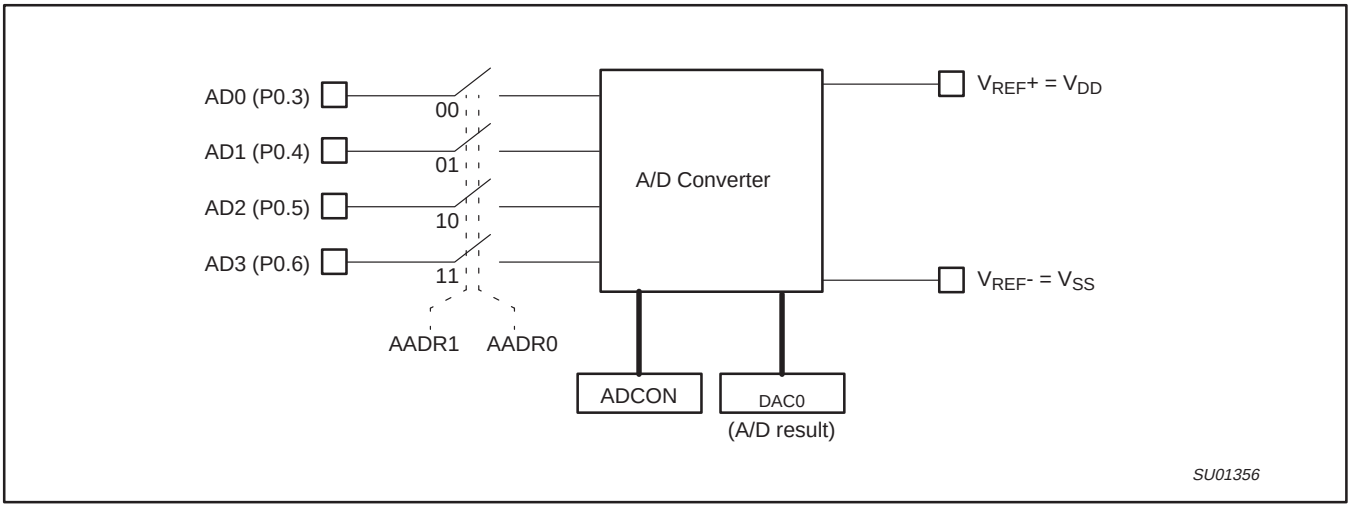

Figure 3. A/D Converter Connections

The A/D in Power Down and Idle Modes

While using the CPU clock as the A/D clock source, the Idle mode may be used to conserve power and/or to minimize system noise during the conversion. CPU operation will resume and Idle mode terminate automatically when a conversion is complete if the A/D interrupt is active. In Idle mode, noise from the CPU itself is eliminated, but noise from the oscillator and any other on-chip peripherals that are running will remain.

The CPU may be put into Power Down mode when the A/D is clocked by the on-chip RC oscillator (RCCLK=1). This mode gives the best possible A/D accuracy by eliminating most on-chip noise sources.

If the Power Down mode is entered while the A/D is running from the CPU clock (RCCLK=0), the A/D will abort operation and will not wake up the CPU. The contents of DAC0 will be invalid when operation does resume.

When an A/D conversion is started, Power Down or Idle mode must be activated within two machine cycles in order to have the most accurate A/D result. These two machine cycles are counted at the CPU clock rate. When using the A/D with either Power Down or Idle mode, care must be taken to insure that the CPU is not restarted by another interrupt until the A/D conversion is complete. The possible causes of wakeup are different in Power Down and Idle modes.

A/D accuracy is also affected by noise generated elsewhere in the application, power supply noise, and power supply regulation. Since the P87LPC769 power pins are also used as the A/D reference and supply, the power supply has a very direct affect on the accuracy of A/D readings. Using the A/D without Power Down mode while the clock is divided through the use of CLKR or DIVM has an adverse effect on A/D accuracy.

Code Examples for the A/D

The first piece of sample code shows an example of port configuration for use with the A/D. This example sets up the pins so that all four A/D channels may be used. Port configuration for analog functions is described in the section Analog Functions.

```
; Set up port pins for A/D conversion, without affecting other pins.
   mov    PT0AD,#78h          ; Disable digital inputs on A/D input pins.
   anl    P0M2,#87h           ; Disable digital outputs on A/D input pins.
   orl    P0M1,#78h           ; Disable digital outputs on A/D input pins.
```

Following is an example of using the A/D with interrupts. The routine ADStart begins an A/D conversion using the A/D channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization.

The interrupt handler routine reads the conversion value and returns it in memory address ADResult. The interrupt should be enabled prior to starting the conversion.

```
; Start A/D conversion.
ADStart:
   orl    ADCON,A             ; Add in the new channel number.
   setb   ADCS                ; Start an A/D conversion.
;  orl    PCON,#01h           ; The CPU could be put into Idle mode here.
;  orl    PCON,#02h           ; The CPU could be put into Power Down mode here if RCCLK = 1.
   ret

; A/D interrupt handler.
ADInt:
   push   ACC                 ; Save accumulator.
   mov    A,DAC0              ; Get A/D result,
   mov    ADResult,A          ;   and save it in memory.
   clr    ADCI                ; Clear the A/D completion flag.
   anl    ADCON,#0fch         ; Clear the A/D channel number.
   pop    ACC                 ; Restore accumulator.
   reti
```

Following is an example of using the A/D with polling. An A/D conversion is started using the channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization. The conversion result is returned in the accumulator.

```
ADRead:
   orl    ADCON,A             ; Add in the new channel number.
   setb   ADCS                ; Start A/D conversion.
ADChk:
   jnb    ADCI,ADChk          ; Wait for ADCI to be set.
   mov    A,DAC0              ; Get A/D result.
   clr    ADCI                ; Clear the A/D completion flag.
   anl    ADCON,#0fch         ; Clear the A/D channel number.
   ret
```

Analog Comparators

Two analog comparators are provided on the P87LPC769. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

Comparator Configuration

Each comparator has a control register, CMP1 for comparator 1 and CMP2 for comparator 2. The control registers are identical and are shown in Figure 5.

The overall connections to both comparators are shown in Figure 6. There are eight possible configurations for each comparator, as determined by the control bits in the corresponding CMPn register: CPn, CNn, and OEn. These configurations are shown in Figure 7.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

CMPn Address: ACh for CMP1, ADh for CMP2 Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
—	—	CEn	CPn	CNn	OEn	COn	CMFn

BIT	SYMBOL	FUNCTION
CMPn.7, 6	—	Reserved for future use. Should not be set to 1 by user programs.
CMPn.5	CEn	Comparator enable. When set by software, the corresponding comparator function is enabled. Comparator output is stable 10 microseconds after CEn is first set.
CMPn.4	CPn	Comparator positive input select. When 0, CINnA is selected as the positive comparator input. When 1, CINnB is selected as the positive comparator input.
CMPn.3	CNn	Comparator negative input select. When 0, the comparator reference pin CMPREF is selected as the negative comparator input. When 1, the internal comparator reference V_{ref} is selected as the negative comparator input.
CMPn.2	OEn	Output enable. When 1, the comparator output is connected to the CMPn pin if the comparator is enabled (CEn = 1). This output is asynchronous to the CPU clock.
CMPn.1	COn	Comparator output, synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CEn = 0).
CMPn.0	CMFn	Comparator interrupt flag. This bit is set by hardware whenever the comparator output COn changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CEn = 0).

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Figure 5. Comparator Control Registers (CMP1 and CMP2)

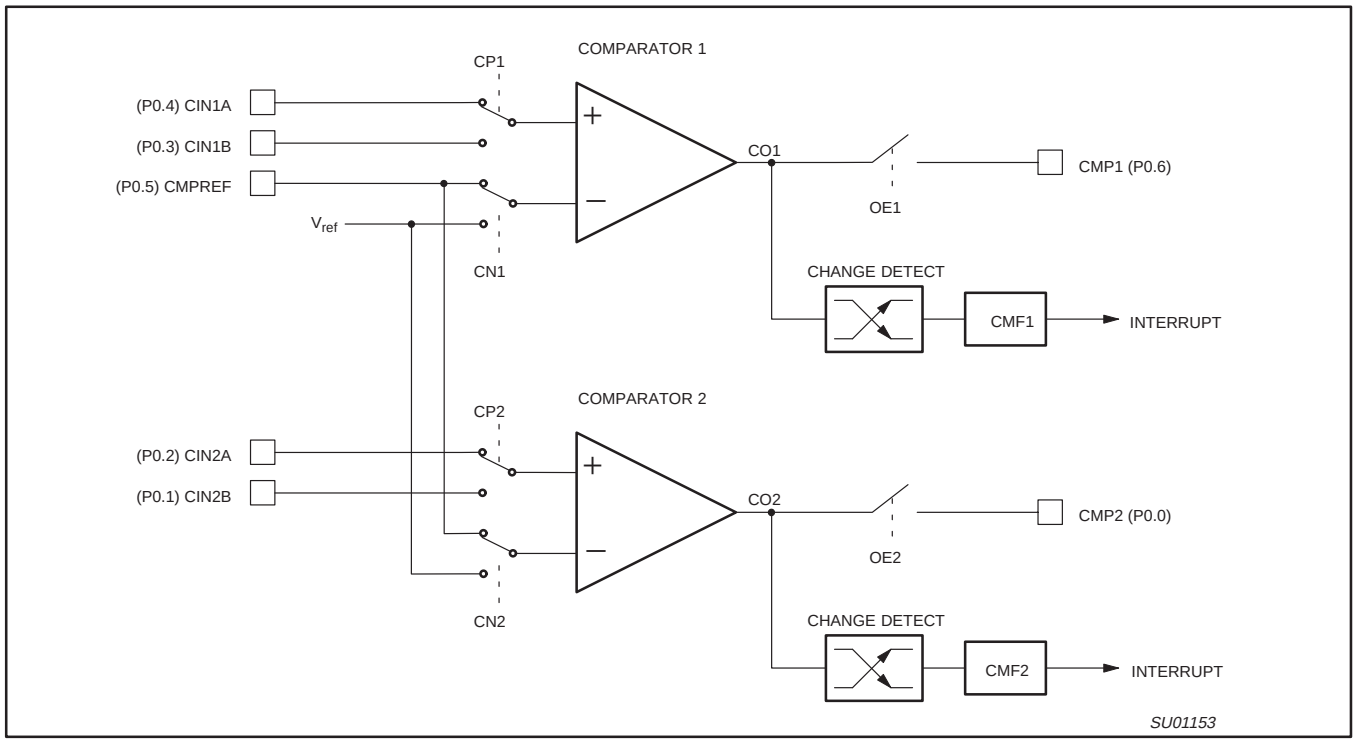

Figure 6. Comparator Input and Output Connections

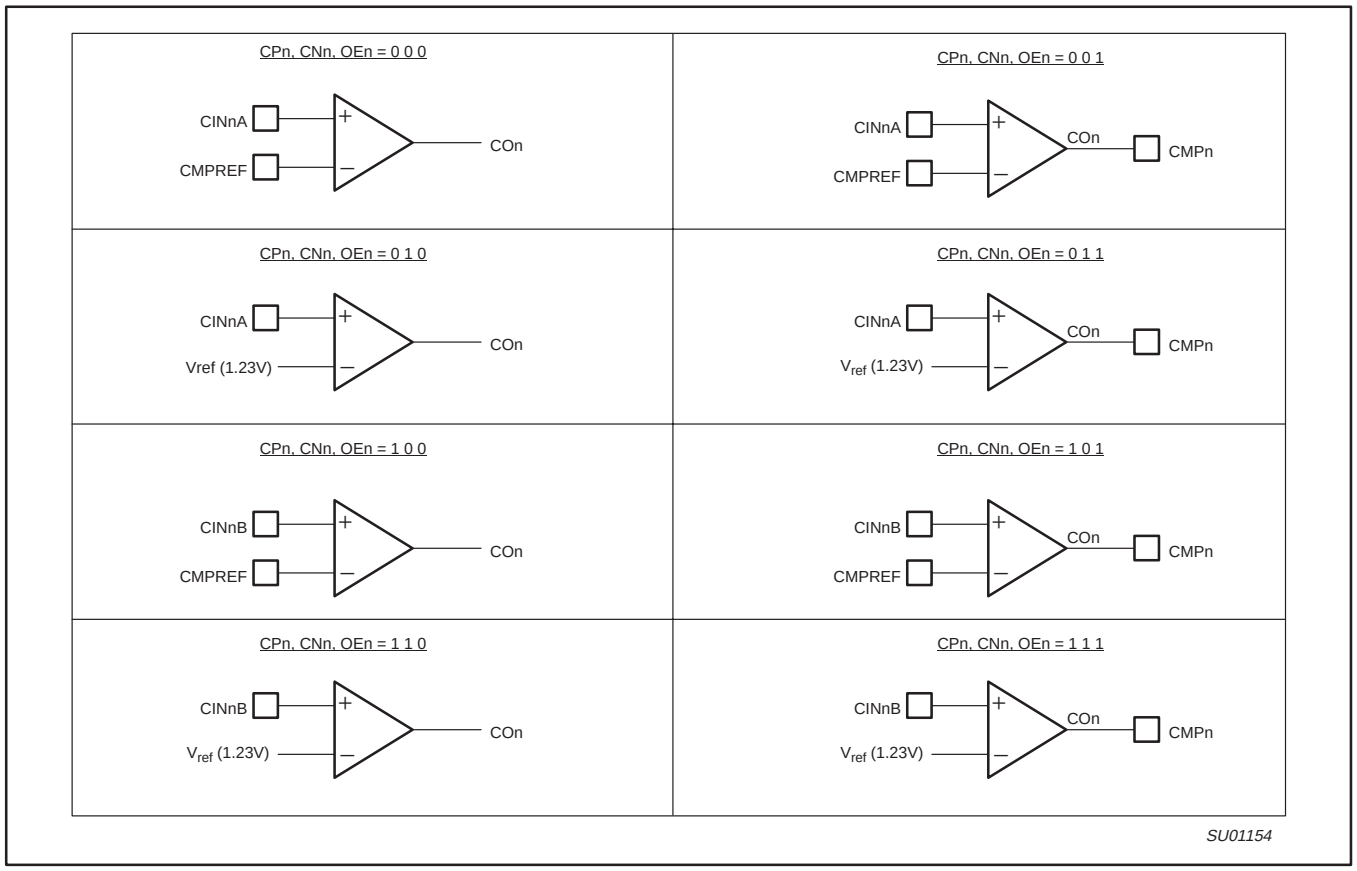

Figure 7. Comparator Configurations

I2CON Address: D8h Reset Value: 81h

Bit Addressable[1]

	7	6	5	4	3	2	1	0
READ	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	—
WRITE	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP

BIT	SYMBOL	FUNCTION
I2CON.7	RDAT	Read: the most recently received data bit.
"	CXA	Write: clears the transmit active flag.
I2CON.6	ATN	Read: ATN = 1 if any of the flags DRDY, ARL, STR, or STP = 1.
"	IDLE	Write: in the I^2C slave mode, writing a 1 to this bit causes the I^2C hardware to ignore the bus until it is needed again.
I2CON.5	DRDY	Read: Data Ready flag, set when there is a rising edge on SCL.
"	CDR	Write: writing a 1 to this bit clears the DRDY flag.
I2CON.4	ARL	Read: Arbitration Loss flag, set when arbitration is lost while in the transmit mode.
"	CARL	Write: writing a 1 to this bit clears the CARL flag.
I2CON.3	STR	Read: Start flag, set when a start condition is detected at a master or non-idle slave.
"	CSTR	Write: writing a 1 to this bit clears the STR flag.
I2CON.2	STP	Read: Stop flag, set when a stop condition is detected at a master or non-idle slave.
"	CSTP	Write: writing a 1 to this bit clears the STP flag.
I2CON.1	MASTER	Read: indicates whether this device is currently as bus master.
"	XSTR	Write: writing a 1 to this bit causes a repeated start condition to be generated.
I2CON.0	—	Read: undefined.
"	XSTP	Write: writing a 1 to this bit causes a stop condition to be generated.

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Figure 9. I^2C Control Register (I2CON)

I2DAT Address: D9h Reset Value: xxh

Not Bit Addressable

	7	6	5	4	3	2	1	0
READ	RDAT	—	—	—	—	—	—	—
WRITE	XDAT	—	—	—	—	—	—	—

BIT	SYMBOL	FUNCTION
I2DAT.7	RDAT	Read: the most recently received data bit, captured from SDA at every rising edge of SCL. Reading I2DAT also clears DRDY and the Transmit Active state.
"	XDAT	Write: sets the data for the next transmitted bit. Writing I2DAT also clears DRDY and sets the Transmit Active state.
I2DAT.6–0	–	Unused.

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Figure 10. I^2C Data Register (I2DAT)

Checking ATN and DRDY

When a program detects ATN = 1, it should next check DRDY. If DRDY = 1, then if it receives the last bit, it should capture the data from RDAT (in I2DAT or I2CON). Next, if the next bit is to be sent, it should be written to I2DAT. One way or another, it should clear DRDY and then return to monitoring ATN. Note that if any of ARL, STR, or STP is set, clearing DRDY will not release SCL to high, so that the I^2C will not go on to the next bit. If a program detects ATN = 1, and DRDY = 0, it should go on to examine ARL, STR, and STP.

External Interrupt Inputs

The P87LPC769 has two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. The two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the $\overline{INTn}$ pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the $\overline{INTn}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the P87LPC769 is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

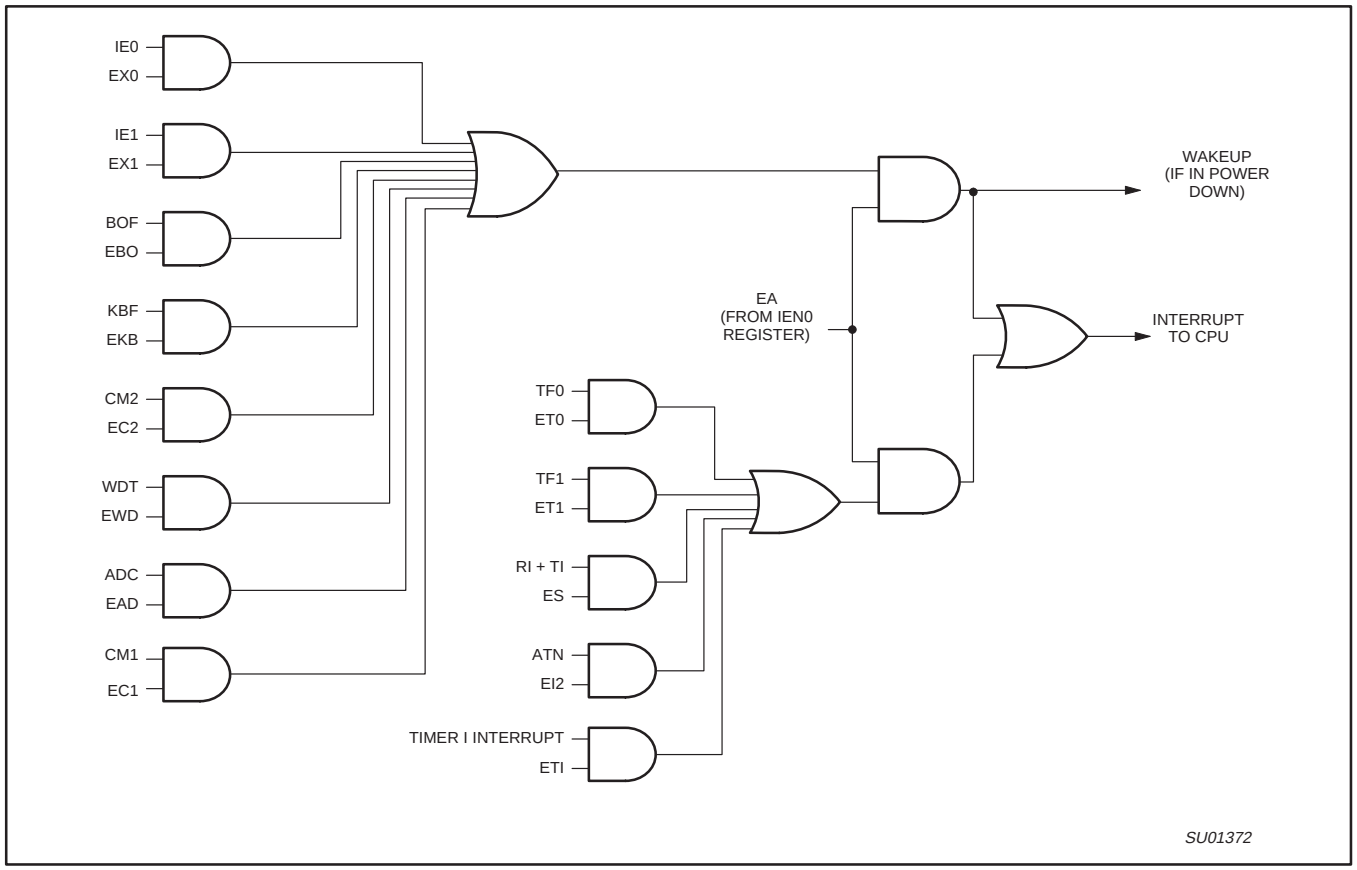

Figure 12. Interrupt Sources, Interrupt Enables, and Power Down Wakeup Sources

I/O Ports

The P87LPC769 has 3 I/O ports, port 0, port 1, and port 2. The exact number of I/O pins available depend upon the oscillator and reset options chosen. At least 15 pins of the P87LPC769 may be used as I/Os when a two-pin external oscillator and an external reset circuit are used. Up to 18 pins may be available if fully on-chip oscillator and reset configurations are chosen.

All but three I/O port pins on the P87LPC769 may be software configured to one of four types on a bit-by-bit basis, as shown in Table 4. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input only. Two configuration registers for each port choose the output type for each port pin.

Table 5. Port Output Configuration Settings

PxM1.y	PxM2.y	Port Output Mode
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

Quasi-Bidirectional Output Configuration

The default port output configuration for standard P87LPC769 I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again.

The quasi-bidirectional port configuration is shown in Figure 13.

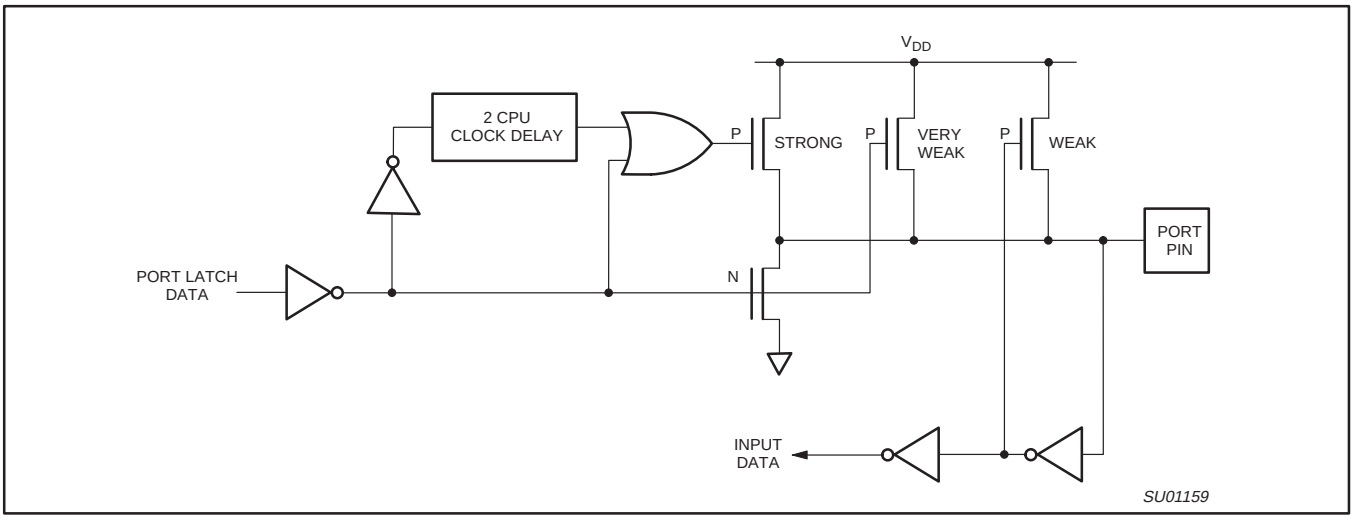

Figure 13. Quasi-Bidirectional Output

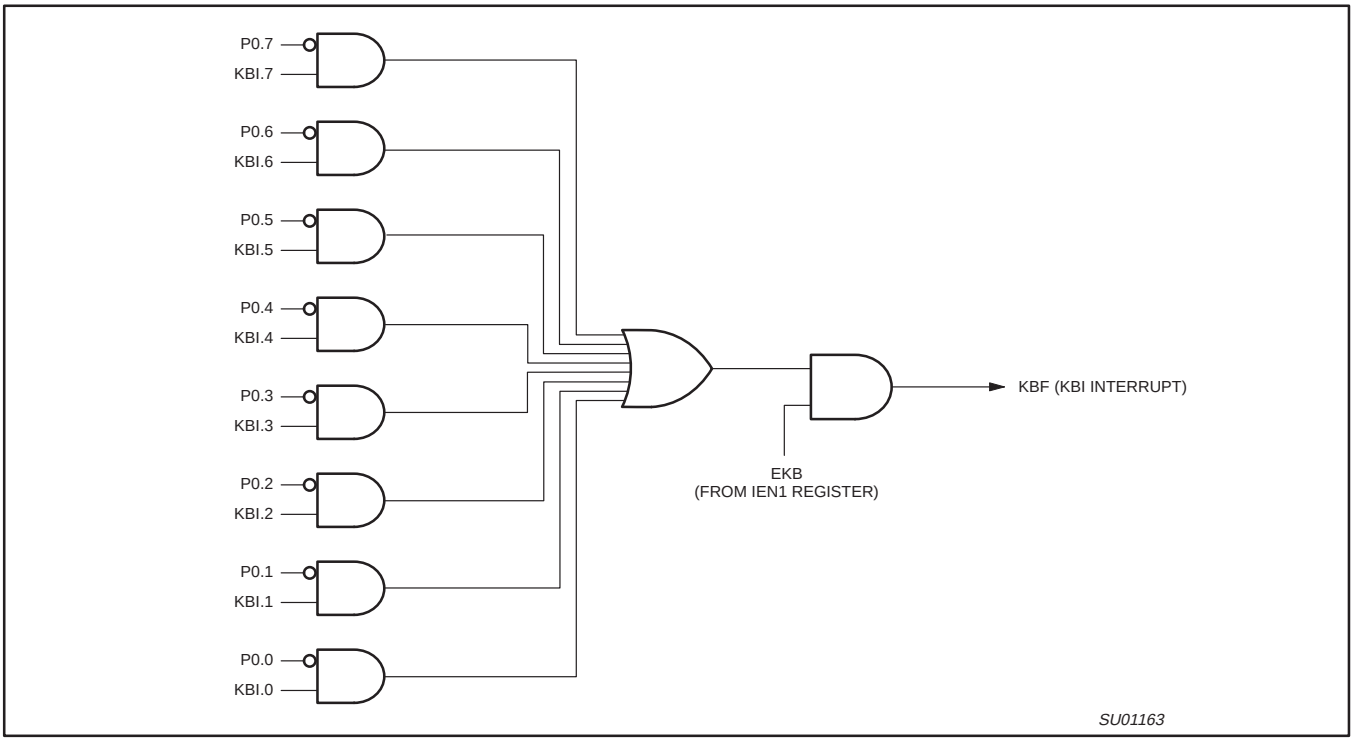

Figure 17. Keyboard Interrupt

KBI Address: 86h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

BIT	SYMBOL	FUNCTION
KBI.7	KBI.7	When set, enables P0.7 as a cause of a Keyboard Interrupt.
KBI.6	KBI.6	When set, enables P0.6 as a cause of a Keyboard Interrupt.
KBI.5	KBI.5	When set, enables P0.5 as a cause of a Keyboard Interrupt.
KBI.4	KBI.4	When set, enables P0.4 as a cause of a Keyboard Interrupt.
KBI.3	KBI.3	When set, enables P0.3 as a cause of a Keyboard Interrupt.
KBI.2	KBI.2	When set, enables P0.2 as a cause of a Keyboard Interrupt.
KBI.1	KBI.1	When set, enables P0.1 as a cause of a Keyboard Interrupt.
KBI.0	KBI.0	When set, enables P0.0 as a cause of a Keyboard Interrupt.

Note: the Keyboard Interrupt must be enabled in order for the settings of the KBI register to be effective. The interrupt flag (KBF) is located at bit 7 of AUXR1.

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Figure 18. Keyboard Interrupt Register (KBI)

Oscillator

The P87LPC769 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 10 MHz; ceramic resonators; and on-chip RC oscillator.

Low Frequency Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 6 shows capacitor values that may be used with a quartz crystal in this mode.

Table 6. Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator Frequency	V_{DD} = 4.5 to 5.5 V		
	Lower Limit	Optimal Value	Upper Limit
20 kHz	33 pF	33 pF	47 pF
32 kHz	33 pF	33 pF	47 pF
100 kHz	15 pF	15 pF	33 pF

Medium Frequency Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 7 shows capacitor values that may be used with a quartz crystal in this mode.

Table 7. Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V_{DD} = 4.5 to 5.5 V		
	Lower Limit	Optimal Value	Upper Limit
100 kHz	33 pF	33 pF	47 pF
1 MHz	15 pF	15 pF	33 pF
4 MHz	15 pF	15 pF	33 pF

High Frequency Oscillator Option

This option supports an external crystal in the range of 4 to 10 MHz. Ceramic resonators are also supported in this configuration.

Table 8 shows capacitor values that may be used with a quartz crystal in this mode.

Table 8. Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator Frequency	V_{DD} = 4.5 to 5.5 V		
	Lower Limit	Optimal Value	Upper Limit
4 MHz	15 pF	33 pF	68 pF
8 MHz	15 pF	33 pF	47 pF

On-Chip RC Oscillator Option

The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. Note that the on-chip oscillator has a ±25% frequency tolerance and for that reason may not be suitable for use in some applications. A clock output on the X2/P2.0 pin may be enabled when the on-chip RC oscillator is used.

External Clock Input Option

In this configuration, the processor clock is input from an external source driving the X1/P2.1 pin. The rate may be from 0 Hz up to 10 MHz. When the external clock input mode is used, the X2/P2.0 pin may be used as a standard port pin. A clock output on the X2/P2.0 pin may be enabled when the external clock input is used.

Clock Output

The P87LPC769 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC769. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is 1/6 of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

For correct activation of Brownout Detect, the V_{DD} fall time must be no faster than 50 mV/µs. When V_{DD} is restored, is should not rise faster than 2 mV/µs in order to insure a proper reset.

The brownout voltage (BOV) bit in the EPROM configuration register UCFG1 must be programmed to a zero.

If the Brownout Detect function is not required in an application, it may be disabled, thus saving power. Brownout Detect is disabled by setting the control bit BOD in the AUXR1 register (AUXR1.6).

Power On Detection

The Power On Detect has a function similar to the Brownout Detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout Detect can work. When this feature is activated, the POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain set until cleared by software.

Power Reduction Modes

The P87LPC769 supports Idle and Power Down modes of power reduction.

Idle Mode

The Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or Reset may terminate Idle mode. Idle mode is entered by setting the IDL bit in the PCON register (see Figure 22).

Power Down Mode

The Power Down mode stops the oscillator in order to absolutely minimize power consumption. Power Down mode is entered by setting the PD bit in the PCON register (see Figure 22).

The processor can be made to exit Power Down mode via Reset or one of the interrupt sources shown in Table 5. This will occur if the interrupt is enabled and its priority is higher than any interrupt currently in progress.

In Power Down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power Down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is recommended to wake up the processor via Reset in this case. V_{DD} must be raised to within the operating range before the Power Down mode is exited. Since the watchdog timer has a separate oscillator, it may reset the processor upon overflow if it is running during Power Down.

Note that if the Brownout Detect reset is enabled, the processor will be put into reset as soon as V_{DD} drops below the brownout voltage. If Brownout Detect is configured as an interrupt and is enabled, it will wake up the processor from Power Down mode when V_{DD} drops below the brownout voltage.

When the processor wakes up from Power Down mode, it will start the oscillator immediately and begin execution when the oscillator is stable. Oscillator stability is determined by counting 1024 CPU clocks after start-up when one of the crystal oscillator configurations is used, or 256 clocks after start-up for the internal RC or external clock input configurations.

Some chip functions continue to operate and draw power during Power Down mode, increasing the total power used during Power Down. These include the Brownout Detect, Watchdog Timer, Comparators, and A/D converter.

PCON Address: 87h

Not Bit Addressable

Reset Value:
- 30h for a Power On reset
- 20h for a Brownout reset
- 00h for other reset sources

7	6	5	4	3	2	1	0
SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL

BIT	SYMBOL	FUNCTION
PCON.7	SMOD1	When set, this bit doubles the UART baud rate for modes 1, 2, and 3.
PCON.6	SMOD0	This bit selects the function of bit 7 of the SCON SFR. When 0, SCON.7 is the SM0 bit. When 1, SCON.7 is the FE (Framing Error) flag. See Figure 26 for additional information.
PCON.5	BOF	Brown Out Flag. Set automatically when a brownout reset or interrupt has occurred. Also set at power on. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.4	POF	Power On Flag. Set automatically when a power-on reset has occurred. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.3	GF1	General purpose flag 1. May be read or written by user software, but has no effect on operation.
PCON.2	GF0	General purpose flag 0. May be read or written by user software, but has no effect on operation.
PCON.1	PD	Power Down control bit. Setting this bit activates Power Down mode operation. Cleared when the Power Down mode is terminated (see text).
PCON.0	IDL	Idle mode control bit. Setting this bit activates Idle mode operation. Cleared when the Idle mode is terminated (see text).

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Figure 22. Power Control Register (PCON)

Timer/Counters

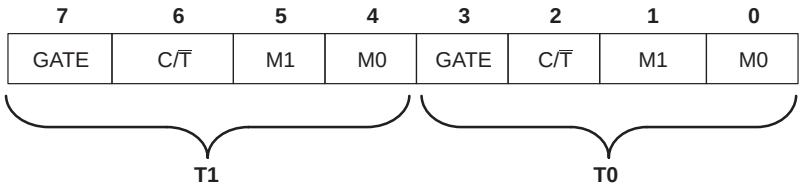
The P87LPC769 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters (see Figure 25). An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency. Refer to the section Enhanced CPU for a description of the CPU clock.

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The “Timer” or “Counter” function is selected by control bits C/T in the Special Function Register TMOD. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

TMOD Address: 89h Reset Value: 00h
Not Bit Addressable



BIT	SYMBOL	FUNCTION
TMOD.7	GATE	Gating control for Timer 1. When set, Timer/Counter is enabled only while the $\overline{INT1}$ pin is high and the TR1 control pin is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
TMOD.6	C/$\overline{T}$	Timer or Counter Selector for Timer 1. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T1 input pin).
TMOD.5, 4	M1, M0	Mode Select for Timer 1 (see table below).
TMOD.3	GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is high and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
TMOD.2	C/$\overline{T}$	Timer or Counter Selector for Timer 0. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T0 input pin).
TMOD.1, 0	M1, M0	Mode Select for Timer 0 (see table below).
	M1, M0	Timer Mode
	0 0	8048 Timer “TLn” serves as 5-bit prescaler.
	0 1	16-bit Timer/Counter “THn” and “TLn” are cascaded; there is no prescaler.
	1 0	8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows.
	1 1	Timer 0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by the Timer 1 control bits (see text). Timer 1 in this mode is stopped.

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Figure 25. Timer/Counter Mode Control Register (TMOD)

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = CPU clock/6. The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is 1/32 of the CPU clock frequency. If SMOD1 = 1, the baud rate is 1/16 of the CPU clock frequency.

$$\text{Mode 2 Baud Rate} = \frac{1 + \text{SMOD1}}{32} \times \text{CPU clock frequency}$$

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD1. The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either “timer” or “counter” operation, and in any of its 3 running modes. In the most typical applications, it is configured for “timer” operation, in the auto-reload mode (high nibble of TMOD = 0010b). In that case the baud rate is given by the formula:

$$\text{Mode 1, 3 Baud Rate} = \frac{\text{CPU clock frequency}/192 \text{ (or 96 if SMOD1} = 1)}{256 - (\text{TH1})}$$

Tables 6 and 7 list various commonly used baud rates and how they can be obtained using Timer 1 as the baud rate generator.

Table 10. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 0

Timer Count	Baud Rate				
	2400	4800	9600	19.2k	38.4k
–1	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728
–2	0.9216	1.8432	* 3.6864	* 7.3728	–
–3	1.3824	2.7648	5.5296	–	–
–4	* 1.8432	* 3.6864	* 7.3728	–	–
–5	2.3040	4.6080	9.2160	–	–
–6	2.7648	5.5296	–	–	–
–7	3.2256	6.4512	–	–	–
–8	* 3.6864	* 7.3728	–	–	–
–9	4.1472	8.2944	–	–	–
–10	4.6080	9.2160	–	–	–

Table 11. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 1

Timer Count	Baud Rate					
	2400	4800	9600	19.2k	38.4k	57.6k
–1	0.2304	0.4608	0.9216	* 1.8432	* 3.6864	5.5296
–2	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	–
–3	0.6912	1.3824	2.7648	5.5296	–	–
–4	0.9216	* 1.8432	* 3.6864	* 7.3728	–	–
–5	1.1520	2.3040	4.6080	9.2160	–	–
–6	1.3824	2.7648	5.5296	–	–	–
–7	1.6128	3.2256	6.4512	–	–	–
–8	* 1.8432	* 3.6864	* 7.3728	–	–	–
–9	2.0736	4.1472	8.2944	–	–	–
–10	2.3040	4.6080	9.2160	–	–	–
–11	2.5344	5.0688	–	–	–	–
–12	2.7648	5.5296	–	–	–	–
–13	2.9952	5.9904	–	–	–	–
–14	3.2256	6.4512	–	–	–	–
–15	3.4560	6.9120	–	–	–	–
–16	* 3.6864	* 7.3728	–	–	–	–
–17	3.9168	7.8336	–	–	–	–
–18	4.1472	8.2944	–	–	–	–
–19	4.3776	8.7552	–	–	–	–
–20	4.6080	9.2160	–	–	–	–
–21	4.8384	9.6768	–	–	–	–

NOTES TO TABLES 10 AND 11:
1. Tables 6 and 7 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates.
2. Table 6 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 7 reflects the SMOD1 bit = 1.
3. The tables show all potential CPU clock frequencies up to 10 MHz that may be used for baud rates. Other CPU clock frequencies that would give only lower baud rates are not shown.
4. Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

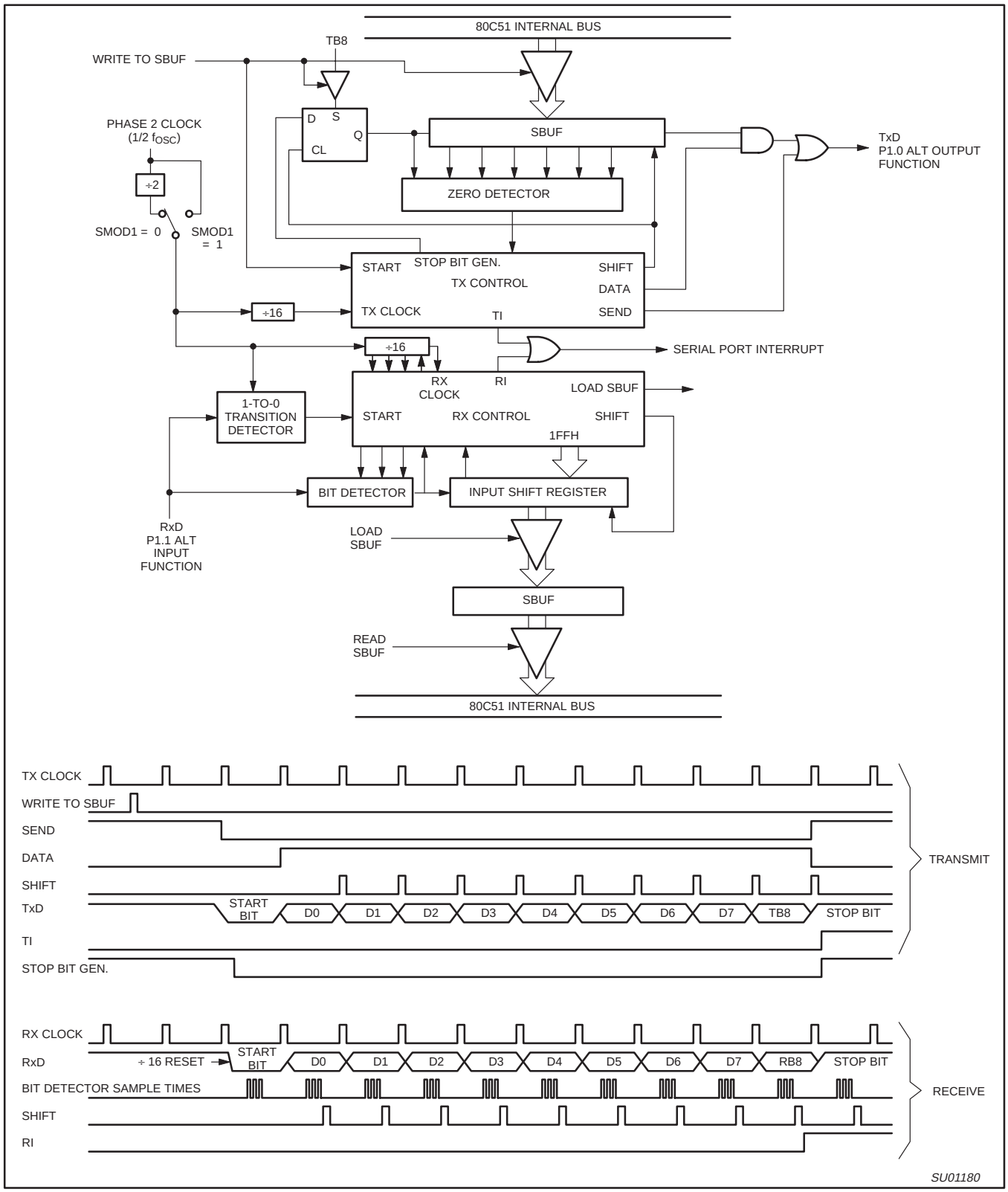

Figure 34. Serial Port Mode 2

Additional Features

The AUXR1 register contains several special purpose control bits that relate to several chip features. AUXR1 is described in Figure 38.

Software Reset

The SRST bit in AUXR1 allows software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. If a value is written to AUXR1 that contains a 1 at bit position 3, all SFRs will be initialized and execution will resume at program address 0000. Care should be taken when writing to AUXR1 to avoid accidental software resets.

Dual Data Pointers

The dual Data Pointer (DPTR) adds to the ways in which the processor can specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. The DPTR that is not currently selected is not accessible to software unless the DPS bit is toggled.

Specific instructions affected by the Data Pointer selection are:

- INC DPTR — Increments the Data Pointer by 1.
- JMP @A+DPTR — Jump indirect relative to DPTR value.
- MOV DPTR, #data16 — Load the Data Pointer with a 16-bit constant.
- MOVC A, @A+DPTR — Move code byte relative to DPTR to the accumulator.
- MOVX A, @DPTR — Move data byte the accumulator to data memory relative to DPTR.
- MOVX @DPTR, A — Move data byte from data memory relative to DPTR to the accumulator.

Also, any instruction that reads or manipulates the DPH and DPL registers (the upper and lower bytes of the current DPTR) will be affected by the setting of DPS. The MOVX instructions have limited application for the P87LPC769 since the part does not have an external data bus. However, they may be used to access EPROM configuration information (see EPROM Characteristics section).

Bit 2 of AUXR1 is permanently wired as a logic 0. This is so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

AUXR1 Address: A2h — Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
KBF	BOD	BOI		SRST	0	—	DPS

BIT	SYMBOL	FUNCTION
AUXR1.7	KBF	Keyboard Interrupt Flag. Set when any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
AUXR1.6	BOD	Brown Out Disable. When set, turns off brownout detection and saves power. See Power Monitoring Functions section for details.
AUXR1.5	BOI	Brown Out Interrupt. When set, prevents brownout detection from causing a chip reset and allows the brownout detect function to be used as an interrupt. See the Power Monitoring Functions section for details.
AUXR1.4	—	Reserved. User code should always write a zero to this bit position.
AUXR1.3	SRST	Software Reset. When set by software, resets the P87LPC769 as if a hardware reset occurred.
AUXR1.2	—	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
AUXR1.1	—	Reserved for future use. Should not be set to 1 by user programs.
AUXR1.0	DPS	Data Pointer Select. Chooses one of two Data Pointers for use by the program. See text for details.

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Figure 38. AUXR1 Register

COMPARATOR ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 V to 6.0 V unless otherwise specified; T_{amb} = –40 °C to +125 °C, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IO}	Offset voltage comparator inputs[1]				±10	mV
V_{CR}	Common mode range comparator inputs		0		V_{DD}–0.3	V
CMRR	Common mode rejection ratio[1]				–50	dB
	Response time			250	500	ns
	Comparator enable to output valid				10	µs
I_{IL}	Input leakage current, comparator	$0 < V_{IN} < V_{DD}$			±10	µA

NOTE:
1. This parameter is guaranteed by characterization, but not tested in production.

A/D CONVERTER DC ELECTRICAL CHARACTERISTICS

Vdd = 2.7 V to 6.0 V unless otherwise specified; Tamb = –40 °C to +125 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
AV_{IN}	Analog input voltage		V_{SS} - 0.2	V_{DD} + 0.2	V
R_{REF}	Resistance between V_{DD} and V_{SS}	A/D enabled	tbd	tbd	kΩ
C_{IA}	Analog input capacitance			15	pF
DL_e	Differential non-linearity[1,2,3]			±1	LSB
IL_e	Integral non-linearity[1,4]			±1	LSB
OS_e	Offset error[1,5]			±2	LSB
G_e	Gain error[1,6]			±1	%
A_e	Absolute voltage error[1,7]			±1	LSB
M_{CTC}	Channel-to-channel matching			±1	LSB
C_t	Crosstalk between inputs of port[8]	0 - 100kHz		-60	dB
-	Input slew rate			100	V/ms
-	Input source impedance			10	kΩ

NOTES:
1. Conditions: V_{SS} = 0V; V_{DD} = 5.12V.
2. The A/D is monotonic, there are no missing codes
3. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. See Figure 41.
4. The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 41.
5. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and the straight line which fits the ideal transfer curve. See Figure 41.
6. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. See Figure 41.
7. The absolute voltage error (A_e) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
8. This should be considered when both analog and digital signals are input simultaneously to A/D pins.
9. Changing the input voltage faster than this may cause erroneous readings.
10. A source impedance higher than this driving an A/D input may result in loss of precision and erroneous readings.

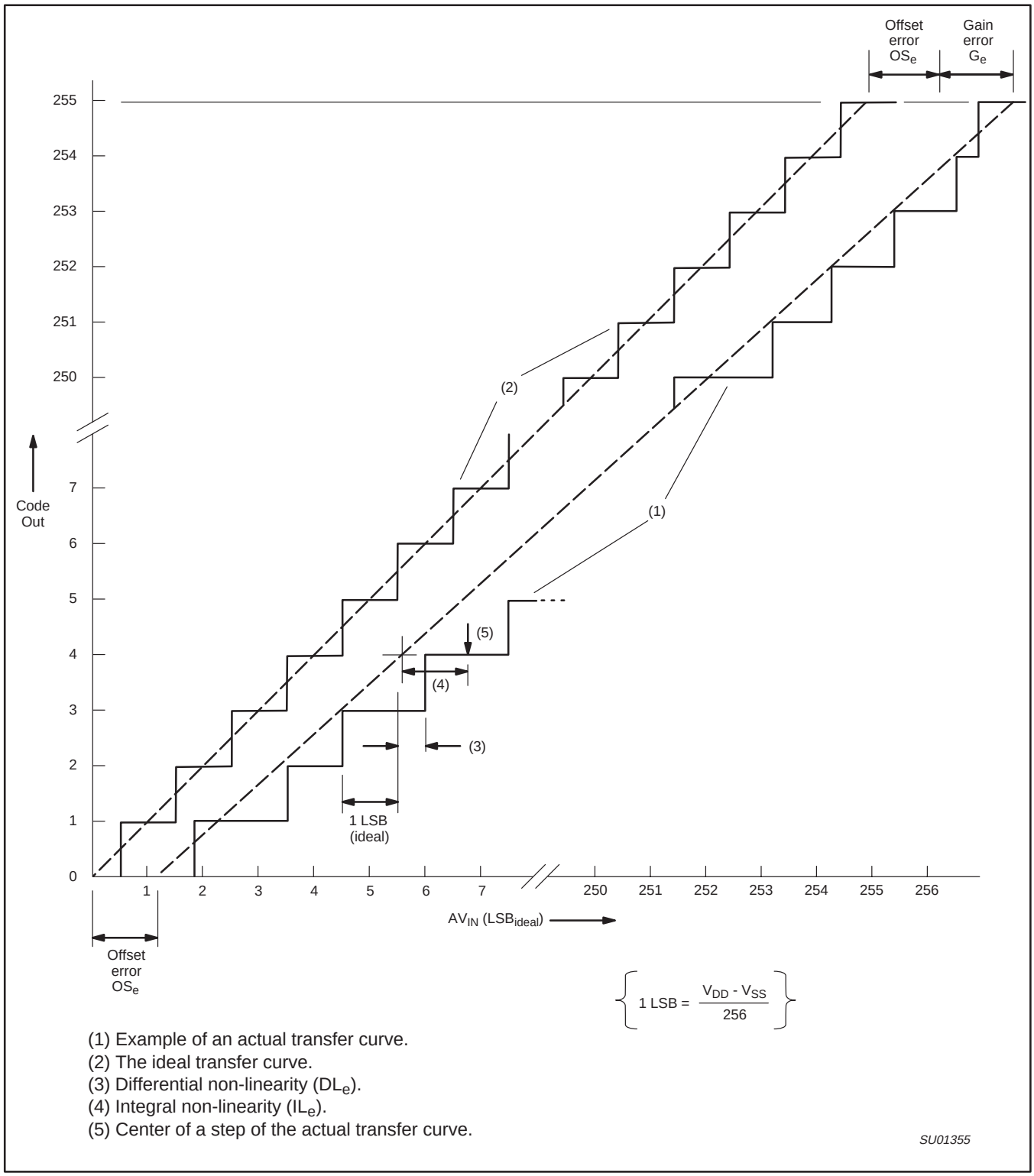

Figure 41. A/D Conversion Characteristics

REVISION HISTORY

Date	CPCN	Description
2002 Mar 12	9397 750 09559	– Added revision history – Interrupt section: BOF is the Interrupt Flag for Brownout Detect (not BOD) – Updated Reset section
2001 Jan 11	9397 750 07923	Previous release

Low power, low price, low pin count (20 pin) microcontroller with 4 kB OTP 8-bit A/D, and DAC

P87LPC769

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