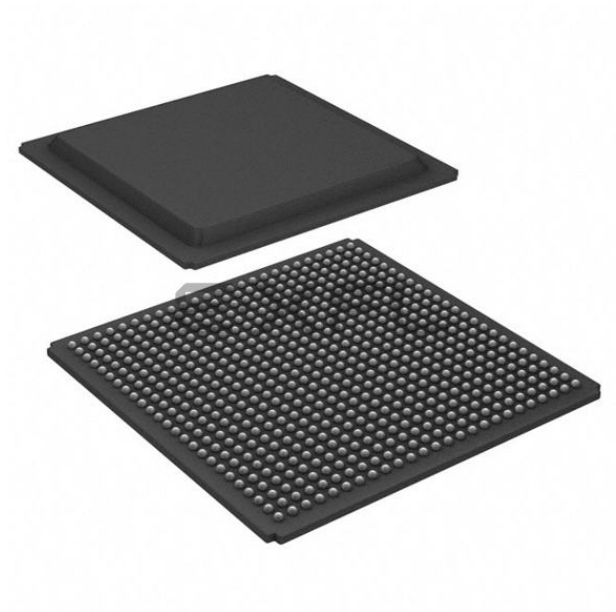

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	768kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	625-BBGA
Supplier Device Package	625-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts101sab1-100

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REVISION HISTORY

5/09—Rev. B to Rev. C

Added parameter value (I_{DD_A} max) in Operating Conditions 20

Updated footnotes in 484-Ball PBGA (B-484) 43

Updated footnotes in 625-Ball PBGA (B-625) 44

Added surface-mount design info in Surface-Mount Design 44

Updated models in Ordering Guide 45

The ADSP-TS101S, in most cases, has a two-cycle arithmetic execution pipeline that is fully interlocked, so whenever a computation result is unavailable for another operation dependent on it, the DSP automatically inserts one or more stall cycles as needed. Efficient programming with dependency-free instructions can eliminate most computational and memory transfer data dependencies.

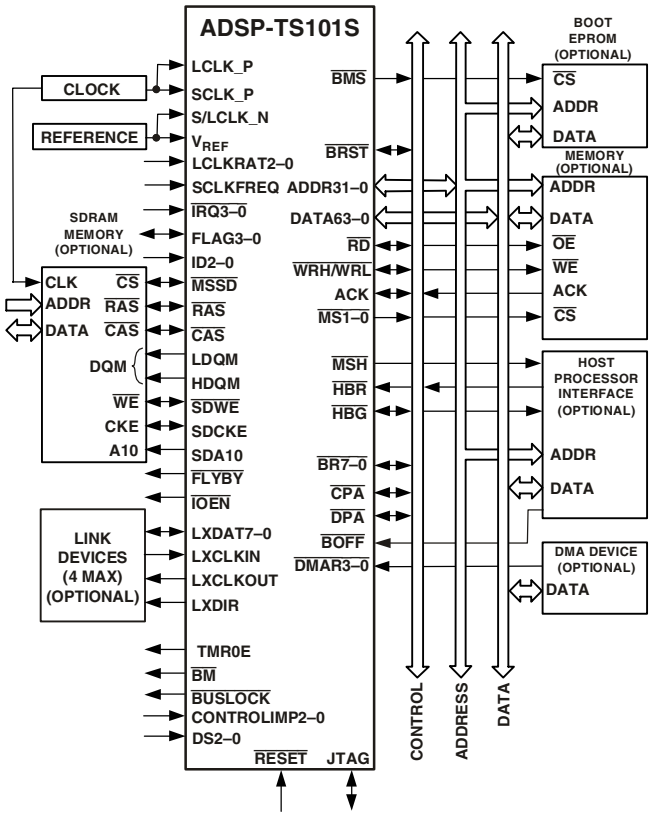

Figure 2. Single-Processor System with External SDRAM

In addition, the ADSP-TS101S supports SIMD operations two ways—SIMD compute blocks and SIMD computations. The programmer can direct both compute blocks to operate on the same data (broadcast distribution) or on different data (merged distribution). In addition, each compute block can execute four 16-bit or eight 8-bit SIMD computations in parallel.

DUAL COMPUTE BLOCKS

The ADSP-TS101S has compute blocks that can execute computations either independently or together as a SIMD engine. The DSP can issue up to two compute instructions per compute block each cycle, instructing the ALU, multiplier, or shifter to perform independent, simultaneous operations.

The compute blocks are referred to as X and Y in assembly syntax, and each block contains three computational units—an ALU, a multiplier, a 64-bit shifter, and a 32-word register file.

- Register file—each compute block has a multiported 32-word, fully orthogonal register file used for transferring data between the computation units and data buses and for storing intermediate results. Instructions can access the registers in the register file individually (word aligned), or in sets of two (dual aligned) or four (quad aligned).
- ALU—the ALU performs a standard set of arithmetic operations in both fixed- and floating-point formats. It also performs logic operations.
- Multiplier—the multiplier performs both fixed- and floating-point multiplication and fixed-point multiply and accumulate.
- Shifter—the 64-bit shifter performs logical and arithmetic shifts, bit and bit stream manipulation, and field deposit and extraction operations.
- Accelerator—128-bit unit for trellis decoding (for example, Viterbi and turbo decoders) and complex correlations for communication applications.

Using these features, the compute blocks can:

- Provide 8 MACs per cycle peak and 7.1 MACs per cycle sustained 16-bit performance and provide 2 MACs per cycle peak and 1.8 MACs per cycle sustained 32-bit performance (based on FIR)
- Execute six single-precision, floating-point or execute 24 fixed-point (16-bit) operations per cycle, providing 1,800 MFLOPS or 7.3 GOPS performance
- Perform two complex 16-bit MACs per cycle
- Execute eight trellis butterflies in one cycle

DATA ALIGNMENT BUFFER (DAB)

The DAB is a quad word FIFO that enables loading of quad word data from nonaligned addresses. Normally, load instructions must be aligned to their data size so that quad words are loaded from a quad-aligned address. Using the DAB significantly improves the efficiency of some applications, such as FIR filters.

DUAL INTEGER ALUS (IALUS)

The ADSP-TS101S has two IALUs that provide powerful address generation capabilities and perform many general-purpose integer operations. Each of the IALUs:

- Provides memory addresses for data and update pointers
- Supports circular buffering and bit-reverse addressing
- Performs general-purpose integer operations, increasing programming flexibility
- Includes a 31-word register file for each IALU

As address generators, the IALUs perform immediate or indirect (pre- and post-modify) addressing. They perform modulus and bit-reverse operations with no constraints placed on memory addresses for the modulus data buffer placement. Each IALU can specify either a single, dual, or quad word access from memory.

LINK PORTS

The DSP's four link ports provide additional 8-bit bidirectional I/O capability. With the ability to operate at a double data rate—latching data on both the rising and falling edges of the clock—running at 125 MHz, each link port can support up to 250M bytes per second, for a combined maximum throughput of 1G bytes per second.

The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications. Applications can also use the link ports for booting.

Each link port has its own double-buffered input and output registers. The DSP's core can write directly to a link port's transmit register and read from a receive register, or the DMA controller can perform DMA transfers through eight (four transmit and four receive) dedicated link port DMA channels.

Each link port has three signals that control its operation. LxCLKOUT and LxCLKIN implement clock/acknowledge handshaking. LxDIR indicates the direction of transfer and is used only when buffering the LxDAT signals. An example application would be using differential low-swing buffers for long twisted-pair wires. LxDAT provides the 8-bit data bus input/output.

Applications can program separate error detection mechanisms for transmit and receive operations (applications can use the checksum mechanism to implement consecutive link port transfers), the size of data packets, and the speed at which bytes are transmitted.

Under certain conditions, the link port receiver can initiate a token switch to reverse the direction of transfer; the transmitter becomes the receiver and vice versa.

TIMER AND GENERAL-PURPOSE I/O

The ADSP-TS101S has a timer pin (TMR0E) that generates output when a programmed timer counter has expired. Also, the DSP has four programmable general-purpose I/O pins (FLAG3–0) that can function as either single-bit input or output. As outputs, these pins can signal peripheral devices; as inputs, they can provide the test for conditional branching.

RESET AND BOOTING

The ADSP-TS101S has two levels of reset (see reset specifications Page 24):

- Power-up reset—after power-up of the system, and strap options are stable, the $\overline{\text{RESET}}$ pin must be asserted (low).
- Normal reset—for any resets following the power-up reset sequence, the $\overline{\text{RESET}}$ pin must be asserted.

The DSP can be reset internally (core reset) by setting the SWRST bit in SQCTL. The core is reset, but not the external port or I/O.

After reset, the ADSP-TS101S has four boot options for beginning operation:

- Boot from EPROM. The DSP defaults to EPROM booting when the $\overline{\text{BMS}}$ pin strap option is set low. See Strap Pin Function Descriptions on Page 19.
- Boot by an external master (host or another ADSP-TS101S). Any master on the cluster bus can boot the ADSP-TS101S through writes to its internal memory or through autoDMA.
- Boot by link port. All four receive link DMA channels are initialized after reset to transfer a 256-word block to internal memory address 0 to 255, and to issue an interrupt at the end of the block (similar to EP DMA). The corresponding DMA interrupts are set to address zero (0).
- No boot—Start running from an external memory. Using the "no boot" option, the ADSP-TS101S must start running from an external memory, caused by asserting one of the $\overline{\text{IRQ3–0}}$ interrupt signals.

The ADSP-TS101S core always exits from reset in the idle state and waits for an interrupt. Some of the interrupts in the interrupt vector table are initialized and enabled after reset.

LOW POWER OPERATION

The ADSP-TS101S can enter a low power sleep mode in which its core does not execute instructions, reducing power consumption to a minimum. The ADSP-TS101S exits sleep mode when it senses a falling edge on any of its $\overline{\text{IRQ3–0}}$ interrupt inputs. The interrupt, if enabled, causes the ADSP-TS101S to execute the corresponding interrupt service routine. This feature is useful for systems that require a low power standby mode.

CLOCK DOMAINS

As shown in Figure 5, the ADSP-TS101S has two clock inputs, SCLK (system clock) and LCLK (local clock).

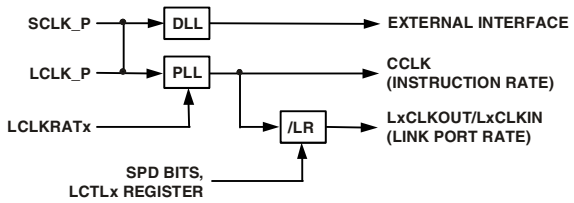

Figure 5. Clock Domains

These inputs drive its two major clock domains:

- SCLK (system clock). Provides clock input for the external bus interface and defines the ac specification reference for the external bus signals. The external bus interface runs at 1× the SCLK frequency. A DLL locks internal SCLK to SCLK input.
- LCLK (local clock). Provides clock input to the internal clock driver, CCLK, which is the internal clock for the core, internal buses, memory, and link ports. The instruction execution rate is equal to CCLK. A PLL from LCLK gener-

Table 5. Pin Definitions—External Port Bus Controls

Signal	Type	Term	Description
ADDR31–0[1]	I/O/T	nc	Address Bus. The DSP issues addresses for accessing memory and peripherals on these pins. In a multiprocessor system, the bus master drives addresses for accessing internal memory or I/O processor registers of other ADSP-TS101S processors. The DSP inputs addresses when a host or another DSP accesses its internal memory or I/O processor registers.
DATA63–0[1]	I/O/T	nc	External Data Bus. Data and instructions are received, and driven by the DSP, on these pins.
$\overline{RD}$[2]	I/O/T (pu[3])	nc	Memory Read. $\overline{RD}$ is asserted whenever the DSP reads from any slave in the system, excluding SDRAM. When the DSP is a slave, $\overline{RD}$ is an input and indicates read transactions that access its internal memory or universal registers. In a multiprocessor system, the bus master drives $\overline{RD}$. The $\overline{RD}$ pin changes concurrently with ADDR pins.
$\overline{WRL}$[2]	I/O/T (pu[3])	nc	Write Low. $\overline{WRL}$ is asserted in two cases: When the ADSP-TS101S writes to an even address word of external memory or to another external bus agent; and when the ADSP-TS101S writes to a 32-bit zone (host, memory, or DSP programmed to 32-bit bus). An external master (host or DSP) asserts $\overline{WRL}$ for writing to a DSP's low word of internal memory. In a multiprocessor system, the bus master drives $\overline{WRL}$. The $\overline{WRL}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRL}$ is an input and indicates write transactions that access its internal memory or universal registers.
$\overline{WRH}$[2]	I/O/T (pu[3])	nc	Write High. $\overline{WRH}$ is asserted when the ADSP-TS101S writes a long word (64 bits) or writes to an odd address word of external memory or to another external bus agent on a 64-bit data bus. An external master (host or another DSP) must assert $\overline{WRH}$ for writing to a DSP's high word of 64-bit data bus. In a multiprocessing system, the bus master drives $\overline{WRH}$. The $\overline{WRH}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRH}$ is an input and indicates write transactions that access its internal memory or universal registers.
ACK	I/O/T	epu	Acknowledge. External slave devices can deassert ACK to add wait states to external memory accesses. ACK is used by I/O devices, memory controllers, and other peripherals on the data phase. The DSP can deassert ACK to add wait states to read accesses of its internal memory. The ADSP-TS101S does not drive ACK during slave writes. Therefore, an external (approximately 10 kΩ) pull-up is required.
$\overline{BMS}$[2, 4]	O/T (pu/pd[3])	au	Boot Memory Select. $\overline{BMS}$ is the chip select for boot EPROM or flash memory. During reset, the DSP uses $\overline{BMS}$ as a strap pin (EBOOT) for EPROM boot mode. When the DSP is configured to boot from EPROM, $\overline{BMS}$ is active during the boot sequence. Pull-down enabled during $\overline{RESET}$ (asserted); pull-up enabled after $\overline{RESET}$ (deasserted). In a multiprocessor system, the DSP bus master drives $\overline{BMS}$. For details see Reset and Booting on Page 9 and the EBOOT signal description in Table 16 on Page 19.
$\overline{MS1–0}$[2]	O/T (pu[3])	nc	Memory Select. $\overline{MS0}$ or $\overline{MS1}$ is asserted whenever the DSP accesses memory banks 0 or 1, respectively. $\overline{MS1–0}$ are decoded memory address pins that change concurrently with ADDR pins. When ADDR31:26 = 0b000010, $\overline{MS0}$ is asserted. When ADDR31:26 = 0b000011, $\overline{MS1}$ is asserted. In multiprocessor systems, the master DSP drives $\overline{MS1–0}$.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

Table 8. Pin Definitions—External Port SDRAM Controller

Signal	Type	Term	Description
$\overline{\text{MSSD}}$[1]	I/O/T (pu[2])	nc	Memory Select SDRAM. $\overline{\text{MSSD}}$ is asserted whenever the DSP accesses SDRAM memory space. $\overline{\text{MSSD}}$ is a decoded memory address pin that is asserted whenever the DSP issues an SDRAM command cycle (access to ADDR31:26 = 0b000001). MSSD in a multiprocessor system is driven by the master DSP.
$\overline{\text{RAS}}$[1]	I/O/T (pu[2])	nc	Row Address Select. When sampled low, $\overline{\text{RAS}}$ indicates that a row address is valid in a read or write of SDRAM. In other SDRAM accesses, RAS defines the type of operation to execute according to SDRAM specification.
$\overline{\text{CAS}}$[1]	I/O/T (pu[2])	nc	Column Address Select. When sampled low, $\overline{\text{CAS}}$ indicates that a column address is valid in a read or write of SDRAM. In other SDRAM accesses, $\overline{\text{CAS}}$ defines the type of operation to execute according to the SDRAM specification.
LDQM[1]	O/T (pu[2])	nc	Low Word SDRAM Data Mask. When LDQM is sampled high, the DSP three-states the SDRAM DQ buffers. LDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted and is inactive on read transactions. On write transactions, LDQM is active when accessing an odd address word on a 64-bit memory bus to disable the write of the low word.
HDQM[1]	O/T (pu[2])	nc	High Word SDRAM Data Mask. When HDQM is sampled high, the DSP three-states the SDRAM DQ buffers. HDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted and is inactive on read transactions. On write transactions, HDQM is active when accessing an even address in word accesses or is active when memory is configured for a 32-bit bus to disable the write of the high word.
SDA10[1]	O/T (pu[2])	nc	SDRAM Address bit 10 pin. Separate A10 signals enable SDRAM refresh operation while the DSP executes non-SDRAM transactions.
SDCKE[1, 3]	I/O/T (pu/pd[2])	nc	SDRAM Clock Enable. Activates the SDRAM clock for SDRAM self-refresh or suspend modes. A slave DSP in a multiprocessor system does not have the pull-up or pull-down. A master DSP (or ID = 0 in a single processor system) has a 100 kΩ pull-up before granting the bus to the host, except when the SDRAM is put in self-refresh mode. In self-refresh mode, the master has a 100 kΩ pull-down before granting the bus to the host.
$\overline{\text{SDWE}}$[1]	I/O/T (pu[2])	nc	SDRAM Write Enable. When sampled low while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM write access. When sampled high while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM read access. In other SDRAM accesses, $\overline{\text{SDWE}}$ defines the type of operation to execute according to SDRAM specification.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.

Table 9. Pin Definitions—JTAG Port

Signal	Type	Term	Description
$\overline{\text{EMU}}$	O (o/d)	nc[1]	Emulation. Connected only to the DSP's JTAG emulator target board connector.
TCK	I	epd or epu[1]	Test Clock (JTAG). Provides an asynchronous clock for JTAG scan.
TDI[2]	I (pu[3])	nc[1]	Test Data Input (JTAG). A serial data input of the scan path.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

Table 9. Pin Definitions—JTAG Port (Continued)

Signal	Type	Term	Description
TDO	O/T	nc[1]	Test Data Output (JTAG). A serial data output of the scan path.
TMS[2]	I (pu[3])	nc[1]	Test Mode Select (JTAG). Used to control the test state machine.
$\overline{\text{TRST}}$[2]	I/A (pu[3])	au	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted or pulsed low after power-up for proper device operation.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] See the reference Page 11 to the JTAG emulation technical reference EE-68.
[2] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[3] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 10. Pin Definitions—Flags, Interrupts, and Timer

Signal	Type	Term	Description
FLAG3–0[1]	I/O/A (pd[2])	nc	FLAG pins. Bidirectional input/output pins can be used as program conditions. Each pin can be configured individually for input or for output. FLAG3–0 are inputs after power-up and reset.
$\overline{\text{IRQ3–0}}$[3]	I/A (pu[2])	nc	Interrupt Request. When asserted, the DSP generates an interrupt. Each of the $\overline{\text{IRQ3–0}}$ pins can be independently set for edge triggered or level sensitive operation. After reset, these pins are disabled unless the $\overline{\text{IRQ3–0}}$ strap option is initialized for booting.
TMR0E[1]	O (pd[2])	au	Timer 0 expires. This output pulses for four SCLK cycles whenever timer 0 expires. At reset this is a strap pin. For additional information, see Table 16 on Page 19.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 11. Pin Definitions—Link Ports

Signal	Type	Term	Description
L0DAT7–0[1]	I/O	nc	Link0 Data 7–0
L1DAT7–0[1]	I/O	nc	Link1 Data 7–0
L2DAT7–0[1]	I/O	nc	Link2 Data 7–0
L3DAT7–0[1]	I/O	nc	Link3 Data 7–0
L0CLKOUT	O	nc	Link0 Clock/Acknowledge Output
L1CLKOUT	O	nc	Link1 Clock/Acknowledge Output
L2CLKOUT	O	nc	Link2 Clock/Acknowledge Output
L3CLKOUT	O	nc	Link3 Clock/Acknowledge Output
L0CLKIN	I/A	epu	Link0 Clock/Acknowledge Input
L1CLKIN	I/A	epu	Link1 Clock/Acknowledge Input
L2CLKIN	I/A	epu	Link2 Clock/Acknowledge Input
L3CLKIN	I/A	epu	Link3 Clock/Acknowledge Input
L0DIR	O	nc	Link0 Direction. (0 = input, 1 = output)

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

For power-up sequencing, power-up reset, and normal reset (hot reset) timing requirements, refer to Table 26 and Figure 13, Table 27 and Figure 14, and Table 28, and Figure 15 respectively.

Table 19. AC Asynchronous Signal Specifications (All values in this table are in nanoseconds)

Name	Description	Pulse Width Low (min)	Pulse Width High (min)
$\overline{IRQ3–0}$[1]	Interrupt request input	t_{CCLK} + 3 ns	
$\overline{DMAR3–0}$[1]	DMA request input	t_{CCLK} + 4 ns	t_{CCLK} + 4 ns
TMR0E[2]	Timer 0 expired output		4 × t_{SCLK} ns
FLAG3–0[1, 3]	Flag pins input	3 × t_{CCLK} ns	3 × t_{CCLK} ns
$\overline{TRST}$	JTAG test reset input	1 ns	

[1] These input pins do not need to be synchronized to a clock reference.
[2] This pin is a strap option. During reset, an internal resistor pulls the pin low.
[3] For output specifications, see Table 29 and Table 30.

Table 20. Reference Clocks—Core Clock (CCLK) Cycle Time

Parameter	Description	Grade = 100 (300 MHz) Min	Grade = 100 (300 MHz) Max	Grade = 000 (250 MHz) Min	Grade = 000 (250 MHz) Max	Unit
t_{CCLK}[1]	Core Clock Cycle Time	3.3	12.5	4.0	12.5	ns

[1] CCLK is the internal processor clock or instruction cycle time. The period of this clock is equal to the system clock period (t_{SCLK}) divided by the system clock ratio (SCLKRAT2–0). For information on available part numbers for different internal processor clock rates, see the Ordering Guide on Page 45.

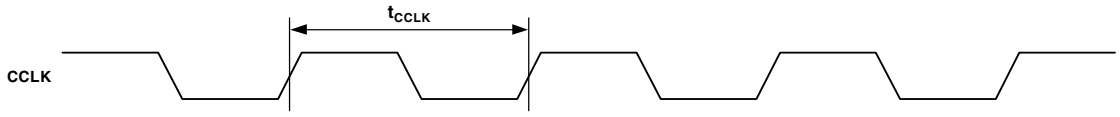

Figure 9. Reference Clocks—Core Clock (CCLK) Cycle Time

Table 21. Reference Clocks—Local Clock (LCLK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{LCLK}[1, 2, 3, 4]	Local Clock Cycle Time	10	25	ns
t_{LCLKH}	Local Clock Cycle High Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKL}	Local Clock Cycle Low Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKJ}[5, 6]	Local Clock Jitter Tolerance		500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] LCLK_P and SCLK_P must be connected to the same source.
[4] The value of (t_{LCLK} / LCLKRAT2-0) must not violate the specification for t_{CCLK}.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

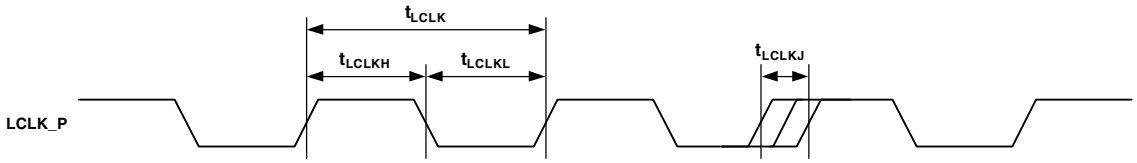

Figure 10. Reference Clocks—Local Clock (LCLK) Cycle Time

Table 25. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{START_LO}	$\overline{RESET}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, SCLK/LCLK, and Static/Strap Pins Are Stable and Within Specification	2		ms
t_{PULSE1_HI}	$\overline{RESET}$ Deasserted for First Pulse	$50 \times t_{SCLK}$	$100 \times t_{SCLK}$	ns
t_{PULSE2_LO}	$\overline{RESET}$ Asserted for Second Pulse	$100 \times t_{SCLK}$		ns
t_{TRST_PWR}[1]	$\overline{TRST}$ Asserted During Power-Up Reset	$2 \times t_{SCLK}$		ns

[1] Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, and SCLK/LCLK and static/strap pins are stable and within specification, and before $\overline{RESET}$ is deasserted.

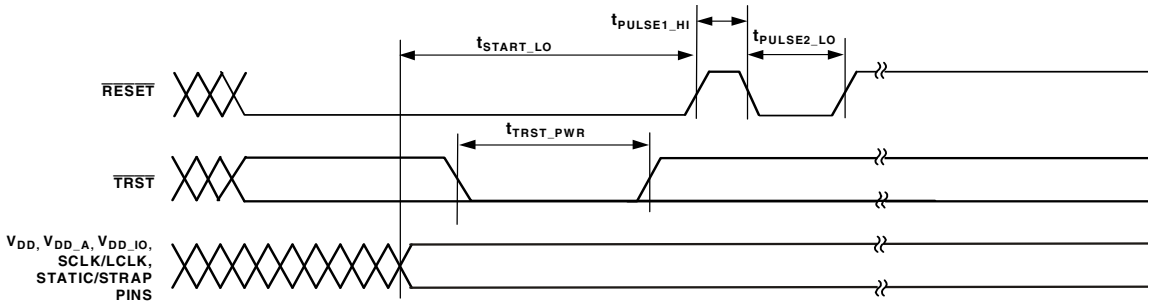

Figure 14. Power-Up Reset Timing

Table 26. Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RST_IN}	$\overline{RESET}$ Asserted	$100 \times t_{SCLK}$		ns
t_{STRAP}	$\overline{RESET}$ Deasserted After Strap Pins Stable	2		ms

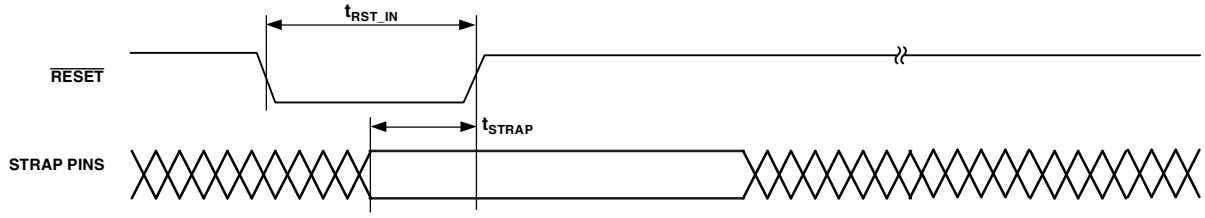

Figure 15. Normal Reset (Hot Reset) Timing

Table 27. AC Signal Specifications (for SCLK <16.7 ns) (All values in this table are in nanoseconds)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
ADDR31–0	External Address Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
DATA63–0	External Data Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSH}}$	Memory Select Host Line			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSSD}}$	Memory Select SDRAM Line	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RD}}$	Memory Read	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRL}}$	Write Low Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRH}}$	Write High Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
ACK	Acknowledge for Data	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
SDCKE	SDRAM Clock Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RAS}}$	Row Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CAS}}$	Column Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
LDQM	Low Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
HDQM	High Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
SDA10	SDRAM ADDR10			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{HBR}}$	Host Bus Request	2.6	0.5					SCLK
$\overline{\text{HBG}}$	Host Bus Grant	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BOFF}}$	Back Off Request	2.6	0.5					SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BRST}}$	Burst Access	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request	2.6	0.5	4.2	1.0			SCLK
$\overline{\text{FLYBY}}$	Flyby Mode Selection			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{IOEN}}$	Flyby I/O Enable			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CPA}}$ [3, 4]	Core Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{DPA}}$ [3, 4]	DMA Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{BMS}}$[5]	Boot Memory Select			4.2	1.0	0.9	2.5	SCLK
FLAG3–0[6]	FLAG Pins			4.2	1.0	1.0	4.0	SCLK
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	1.0			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

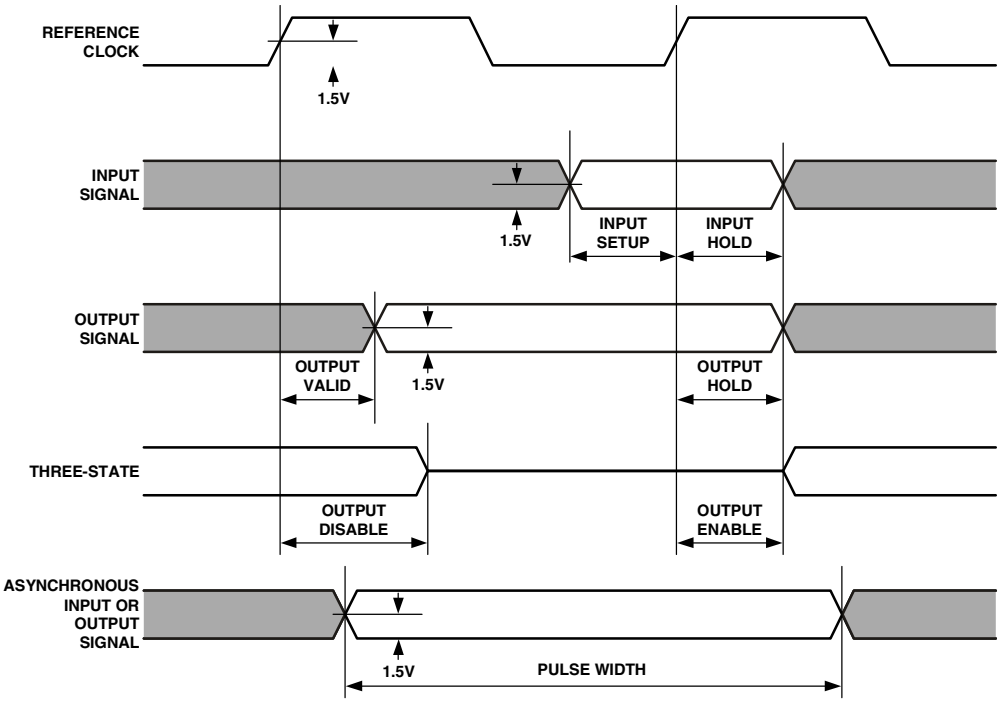

Figure 16. General AC Parameters Timing

Link Ports Data Transfer and Token Switch Timing

Table 31, Table 32, Table 33, and Table 34 with Figure 17, Figure 18, Figure 19, and Figure 20 provide the timing specifications for the link ports data transfer and token switch.

Table 29. Link Ports—Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{CONNS}[1]	Connectivity Pulse Setup	$2 \times t_{CCLK} + 3.5$		ns
t_{CONNS}[2]	Connectivity Pulse Setup	8		ns
t_{CONNIW}[3]	Connectivity Pulse Input Width	$t_{LxCLK\_Tx} + 1$		ns
t_{ACKS}	Acknowledge Setup	$0.5 \times t_{LxCLK\_Tx}$		ns
Switching Characteristics				
t_{LxCLK_Tx}[4]	Transmit Link Clock Period	$0.9 \times LR \times t_{CCLK}$	$1.1 \times LR \times t_{CCLK}$	ns
t_{LxCLKH_Tx}[1]	Transmit Link Clock Width High	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKH_Tx}[2]	Transmit Link Clock Width High	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[1]	Transmit Link Clock Width Low	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[2]	Transmit Link Clock Width Low	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{DIRS}	LxDIR Transmit Setup	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DIRH}	LxDIR Transmit Hold	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DOS}[1]	LxDAT7–0 Output Setup	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[1]	LxDAT7–0 Output Hold	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOS}[2]	LxDAT7–0 Output Setup	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[2]	LxDAT7–0 Output Hold	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{LDOE}	LxDAT7–0 Output Enable	1		ns
t_{LDOD}[5]	LxDAT7–0 Output Disable	1		ns

[1] The formula for this parameter applies when LR is 2.
[2] The formula for this parameter applies when LR is 3, 4, or 8.
[3] LxCLKIN shows the connectivity pulse with each of the three possible transitions to "Acknowledge." After a connectivity pulse low minimum, LxCLKIN may [1] return high and remain high for "Acknowledge," [2] return high and subsequently go low (meeting t_{ACKS}) for "Not Acknowledge," or [3] remain low for "Not Acknowledge."
[4] The Link clock Ratio (LR) is 2, 3, 4, or 8 as set by the SPD bits in the LCTLx register. The maximum LxCLK is 125 MHz. LR = 2 may not be used when CCLK ≥ 250 MHz.
[5] This specification applies to the last data byte or the "Dummy" byte that follows the verification byte if enabled. For more information, see the *ADSP-TS101* TigerSHARC *Processor Hardware Reference*.

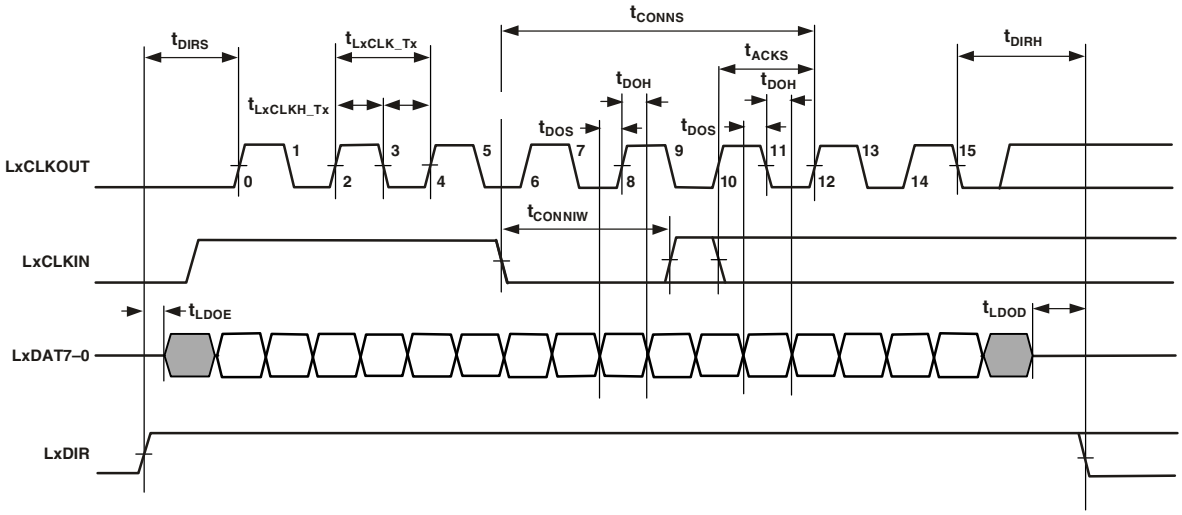

Figure 17. Link Ports—Transmit

OUTPUT DRIVE CURRENTS

Figure 21 through Figure 28 show typical I–V characteristics for the output drivers of the ADSP-TS101S. The curves in these diagrams represent the current drive capability of the output drivers as a function of output voltage over the range of drive strengths. For complete output driver characteristics, refer to IBIS models, available on the Analog Devices website, www.analog.com.

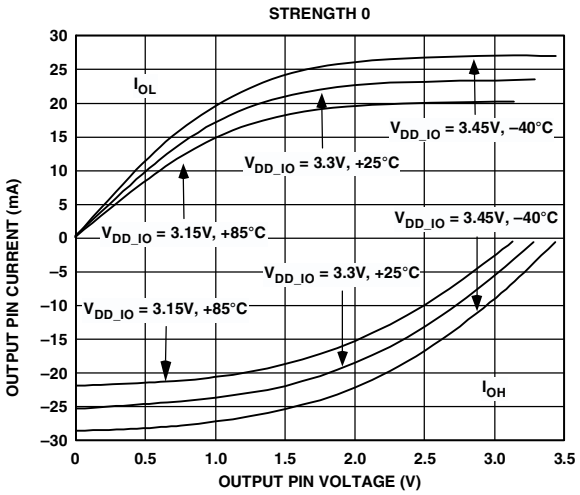

Figure 21. Typical Drive Currents at Strength 0

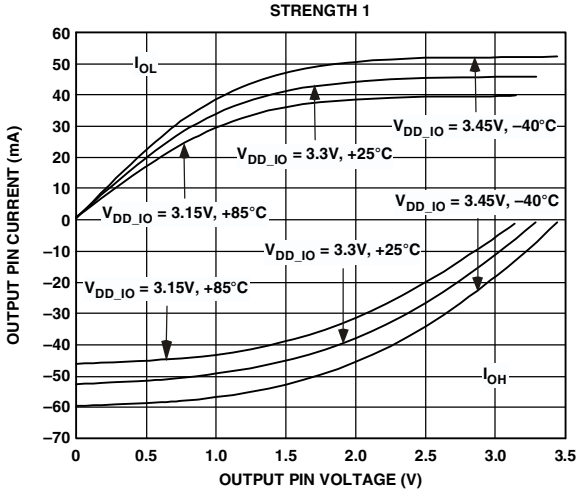

Figure 22. Typical Drive Currents at Strength 1

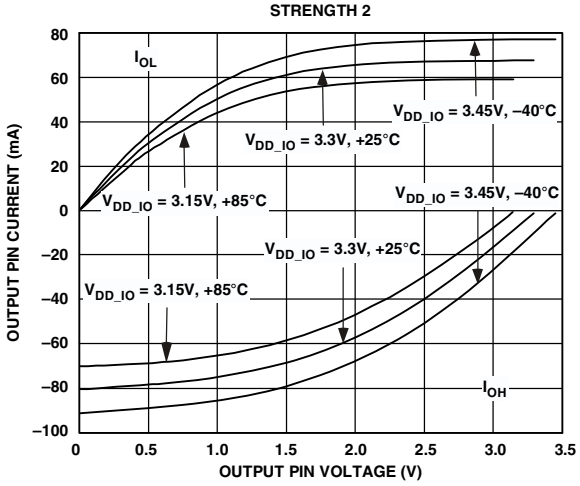

Figure 23. Typical Drive Currents at Strength 2

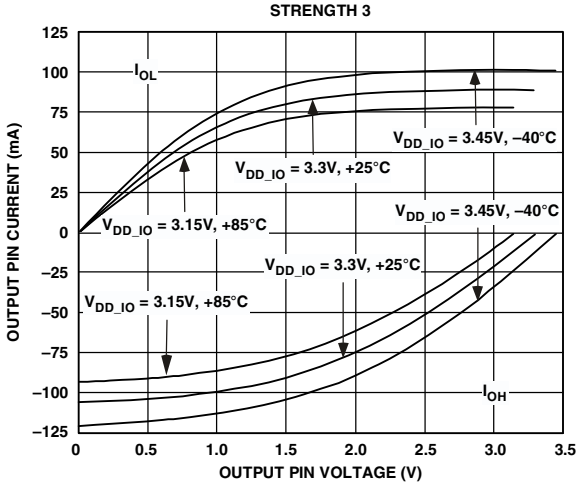

Figure 24. Typical Drive Currents at Strength 3

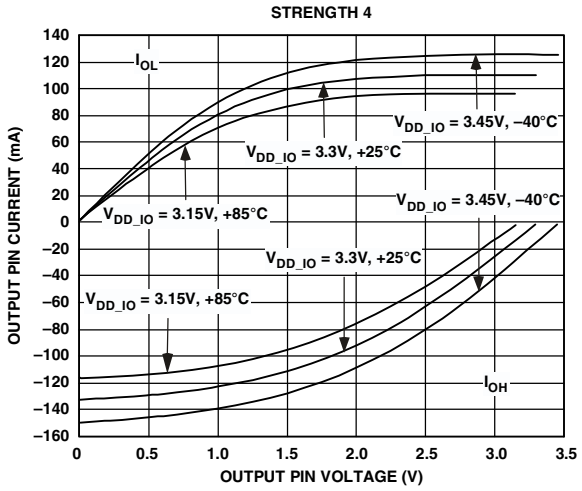

Figure 25. Typical Drive Currents at Strength 4

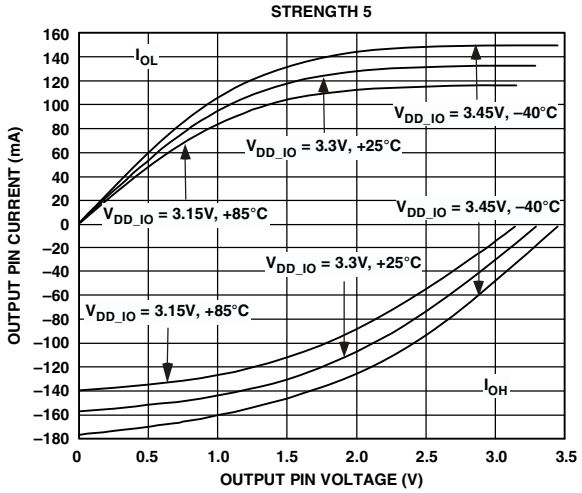

Figure 26. Typical Drive Currents at Strength 5

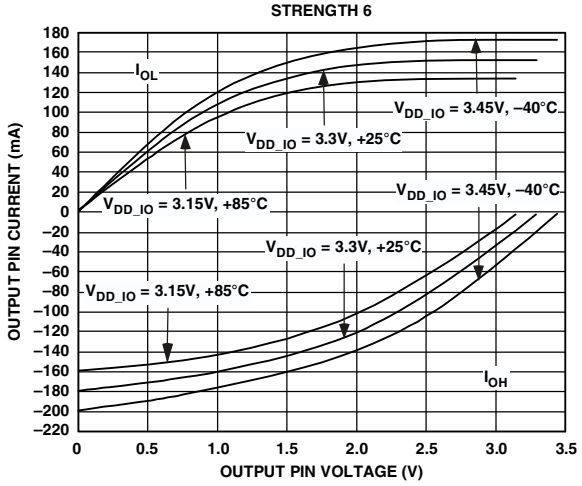

Figure 27. Typical Drive Currents at Strength 6

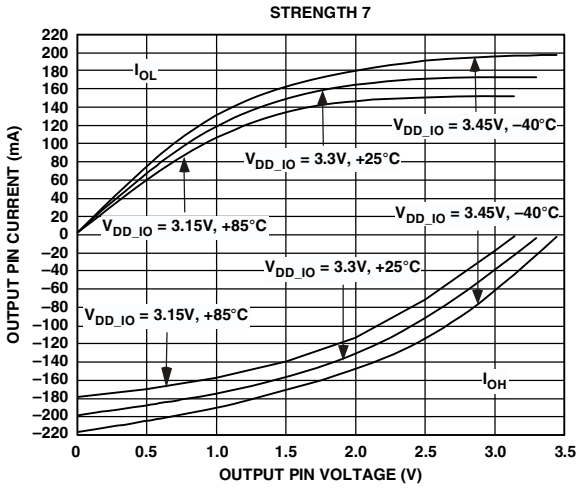

Figure 28. Typical Drive Currents at Strength 7

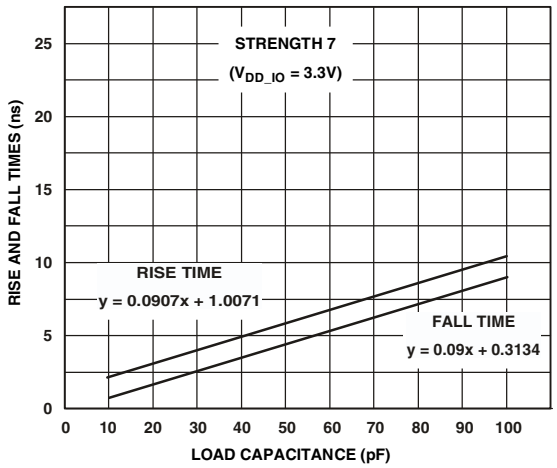

Figure 39. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 7

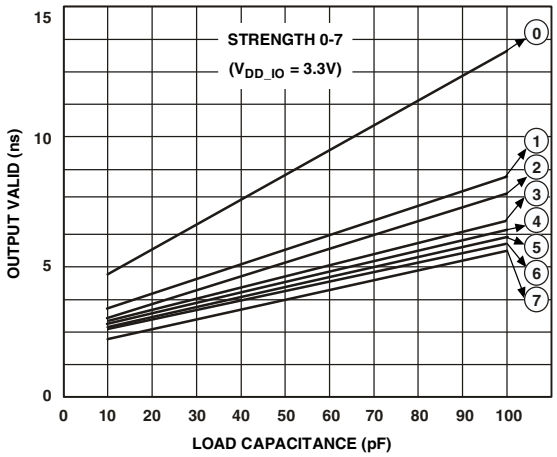

Figure 40. Typical Output Valid (V_{DD_IO} = 3.3 V) vs. Load Capacitance at Max Case Temperature and Strength 0–7[1]

[1] The line equations for the output valid vs. load capacitance are:
Strength 0: y = 0.0956x + 3.5662
Strength 1: y = 0.0523x + 3.2144
Strength 2: y = 0.0433x + 3.1319
Strength 3: y = 0.0391x + 2.9675
Strength 4: y = 0.0393x + 2.7653
Strength 5: y = 0.0373x + 2.6515
Strength 6: y = 0.0379x + 2.1206
Strength 7: y = 0.0399x + 1.9080

ENVIRONMENTAL CONDITIONS

The ADSP-TS101S is rated for performance over the extended commercial temperature range, T_{CASE} = –40°C to +85°C.

Thermal Characteristics

The ADSP-TS101S is packaged in a 19 mm × 19 mm and 27 mm × 27 mm Plastic Ball Grid Array (PBGA). The ADSP-TS101S is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heat sink and/or an air flow source may be used. See Table 33 and Table 34 for thermal data.

Table 33. Thermal Characteristics for 19 mm × 19 mm Package

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow[2] = 0 m/s	16.6	°C/W
	Airflow[3] = 1 m/s	14.0	°C/W
	Airflow[3] = 2 m/s	12.9	°C/W
θ_{JC}		6.7	°C/W
θ_{JB}		5.8	°C/W

[1] Determination of parameter is system dependent and is based on a number of factors, including device power dissipation, package thermal resistance, board thermal characteristics, ambient temperature, and air flow.
[2] Per JEDEC JESD51-2 procedure using a four layer board (compliant with JEDEC JESD51-9).
[3] Per SEMI Test Method G38-87 using a four layer board (compliant with JEDEC JESD51-9).

Table 34. Thermal Characteristics for 27 mm × 27 mm Package

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow[2] = 0 m/s	13.8	°C/W
	Airflow[3] = 1 m/s	11.7	°C/W
	Airflow[3] = 2 m/s	10.8	°C/W
θ_{JC}		3.1	°C/W
θ_{JB}		5.9	°C/W

[1] Determination of parameter is system dependent and is based on a number of factors, including device power dissipation, package thermal resistance, board thermal characteristics, ambient temperature, and air flow.
[2] Per JEDEC JESD51-2 procedure using a four layer board (compliant with JEDEC JESD51-9).
[3] Per SEMI Test Method G38-87 using a four layer board (compliant with JEDEC JESD51-9).

PBGA PIN CONFIGURATIONS

The 484-ball PBGA pin configurations appear in Table 35 and Figure 41. The 625-ball PBGA pin configurations appear in Table 36 and Figure 42.

Table 35. 484-Ball (19 mm × 19 mm) PBGA Pin Assignments

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
A1	V_{SS}	B1	DATA21	C1	DATA23	D1	DATA24	E1	DATA25
A2	DATA14	B2	DATA18	C2	DATA17	D2	DATA19	E2	DATA22
A3	DATA11	B3	DATA12	C3	DATA15	D3	DATA16	E3	DATA20
A4	DATA8	B4	DATA13	C4	DATA9	D4	V_{DD_IO}	E4	V_{DD_IO}
A5	DATA4	B5	DATA7	C5	DATA10	D5	V_{DD}	E5	V_{DD}
A6	DATA1	B6	DATA5	C6	DATA6	D6	V_{DD}	E6	V_{DD}
A7	L0DIR	B7	DATA2	C7	DATA3	D7	V_{DD_IO}	E7	V_{DD_IO}
A8	L0CLKIN	B8	NC	C8	DATA0	D8	V_{DD_IO}	E8	V_{DD}
A9	L0DAT6	B9	L0DAT7	C9	L0CLKOUT	D9	V_{DD_IO}	E9	V_{DD}
A10	L0DAT3	B10	L0DAT4	C10	L0DAT5	D10	V_{DD_IO}	E10	V_{DD}
A11	L0DAT1	B11	L0DAT0	C11	L0DAT2	D11	V_{DD_IO}	E11	V_{DD_IO}
A12	V_{SS}	B12	V_{SS}	C12	LCLK_P	D12	V_{DD_IO}	E12	V_{DD}
A13	LCLK_N	B13	V_{DD_A}	C13	V_{SS}	D13	V_{DD_IO}	E13	V_{DD_IO}
A14	V_{SS_A}	B14	V_{SS_A}	C14	V_{DD_A}	D14	V_{DD_IO}	E14	V_{DD}
A15	SCLK_N	B15	V_{SS}	C15	DS0	D15	V_{DD_IO}	E15	V_{DD_IO}
A16	SCLK_P	B16	DS1	C16	DS2	D16	V_{DD}	E16	V_{DD}
A17	CONTROLIMP2	B17	CONTROLIMP0	C17	V_{REF}	D17	V_{DD_IO}	E17	V_{DD_IO}
A18	CONTROLIMP1	B18	$\overline{\text{DMAR2}}$	C18	TRST	D18	V_{DD}	E18	V_{DD_IO}
A19	$\overline{\text{RESET}}$	B19	$\overline{\text{DMAR0}}$	C19	$\overline{\text{DMAR3}}$	D19	V_{DD_IO}	E19	V_{DD_IO}
A20	$\overline{\text{DMAR1}}$	B20	TMS	C20	TCK	D20	TDO	E20	$\overline{\text{BM}}$
A21	$\overline{\text{EMU}}$	B21	TDI	C21	$\overline{\text{IRQ3}}$	D21	$\overline{\text{IRQ2}}$	E21	$\overline{\text{BMS}}$
A22	V_{SS}	B22	$\overline{\text{IRQ1}}$	C22	$\overline{\text{IRQ0}}$	D22	LCLKRAT1	E22	LCLKRAT2
F1	DATA29	G1	L3DAT1	H1	L3DAT2	J1	L3DAT5	K1	L3CLKOUT
F2	DATA30	G2	DATA28	H2	L3DAT0	J2	L3DAT3	K2	L3DAT7
F3	DATA26	G3	DATA27	H3	DATA31	J3	L3DAT4	K3	L3DAT6
F4	V_{DD_IO}	G4	V_{DD}	H4	V_{DD}	J4	V_{DD_IO}	K4	V_{DD_IO}
F5	V_{DD_IO}	G5	V_{DD}	H5	V_{DD}	J5	V_{DD_IO}	K5	V_{DD_IO}
F6	V_{SS}	G6	V_{SS}	H6	V_{SS}	J6	V_{SS}	K6	V_{SS}
F7	V_{SS}	G7	V_{SS}	H7	V_{SS}	J7	V_{SS}	K7	V_{SS}
F8	V_{SS}	G8	V_{SS}	H8	V_{SS}	J8	V_{SS}	K8	V_{SS}
F9	V_{SS}	G9	V_{SS}	H9	V_{SS}	J9	V_{SS}	K9	V_{SS}
F10	V_{SS}	G10	V_{SS}	H10	V_{SS}	J10	V_{SS}	K10	V_{SS}
F11	V_{SS}	G11	V_{SS}	H11	V_{SS}	J11	V_{SS}	K11	V_{SS}
F12	V_{SS}	G12	V_{SS}	H12	V_{SS}	J12	V_{SS}	K12	V_{SS}
F13	V_{SS}	G13	V_{SS}	H13	V_{SS}	J13	V_{SS}	K13	V_{SS}
F14	V_{SS}	G14	V_{SS}	H14	V_{SS}	J14	V_{SS}	K14	V_{SS}
F15	V_{SS}	G15	V_{SS}	H15	V_{SS}	J15	V_{SS}	K15	V_{SS}
F16	V_{SS}	G16	V_{SS}	H16	V_{SS}	J16	V_{SS}	K16	V_{SS}
F17	V_{DD}	G17	V_{SS}	H17	V_{SS}	J17	V_{SS}	K17	V_{SS}
F18	V_{DD_IO}	G18	V_{DD}	H18	V_{DD_IO}	J18	V_{DD}	K18	V_{DD}
F19	V_{DD_IO}	G19	V_{DD_IO}	H19	V_{DD_IO}	J19	V_{DD_IO}	K19	V_{DD_IO}
F20	LCLKRAT0	G20	FLAG3	H20	FLAG1	J20	ID0	K20	$\overline{\text{IOEN}}$
F21	SCLKFREQ	G21	$\overline{\text{BUSLOCK}}$	H21	FLAG2	J21	ID2	K21	$\overline{\text{FLYBY}}$

Table 35. 484-Ball (19 mm × 19 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
AA1	DATA44	AA10	L2DAT3	AA19	SDA10	AB6	DATA62	AB15	$\overline{BR5}$
AA2	DATA50	AA11	L2DAT7	AA20	ADDR10	AB7	L2DAT1	AB16	$\overline{BOFF}$
AA3	DATA47	AA12	$\overline{BR2}$	AA21	ADDR13	AB8	L2DAT2	AB17	ADDR3
AA4	DATA49	AA13	$\overline{BR6}$	AA22	ADDR15	AB9	L2DAT6	AB18	ADDR4
AA5	DATA51	AA14	$\overline{HBR}$	AB1	V_{SS}	AB10	L2CLKIN	AB19	ADDR6
AA6	DATA54	AA15	$\overline{DPA}$	AB2	DATA53	AB11	L2DIR	AB20	ADDR7
AA7	DATA57	AA16	ADDR2	AB3	DATA55	AB12	$\overline{BR0}$	AB21	ADDR9
AA8	DATA61	AA17	ADDR5	AB4	DATA56	AB13	$\overline{BR1}$	AB22	V_{SS}
AA9	L2DAT0	AA18	ADDR8	AB5	DATA59	AB14	$\overline{BR3}$		

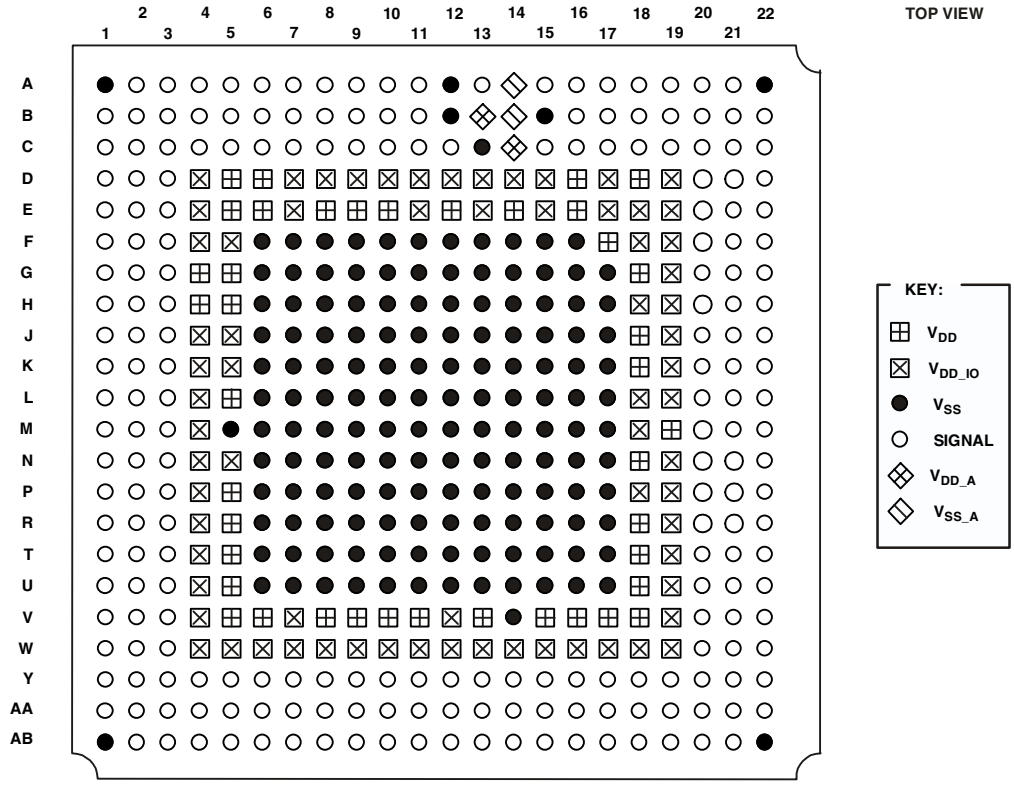

Figure 41. 484-Ball PBGA Pin Configurations (Top View, Summary)

OUTLINE DIMENSIONS

The ADSP-TS101S is available in a 19 mm × 19 mm, 484-ball PBGA package with 22 rows of balls (B-484); the DSP also is available in a 27 mm × 27 mm, 625-ball PBGA package with 25 rows of balls (B-625).

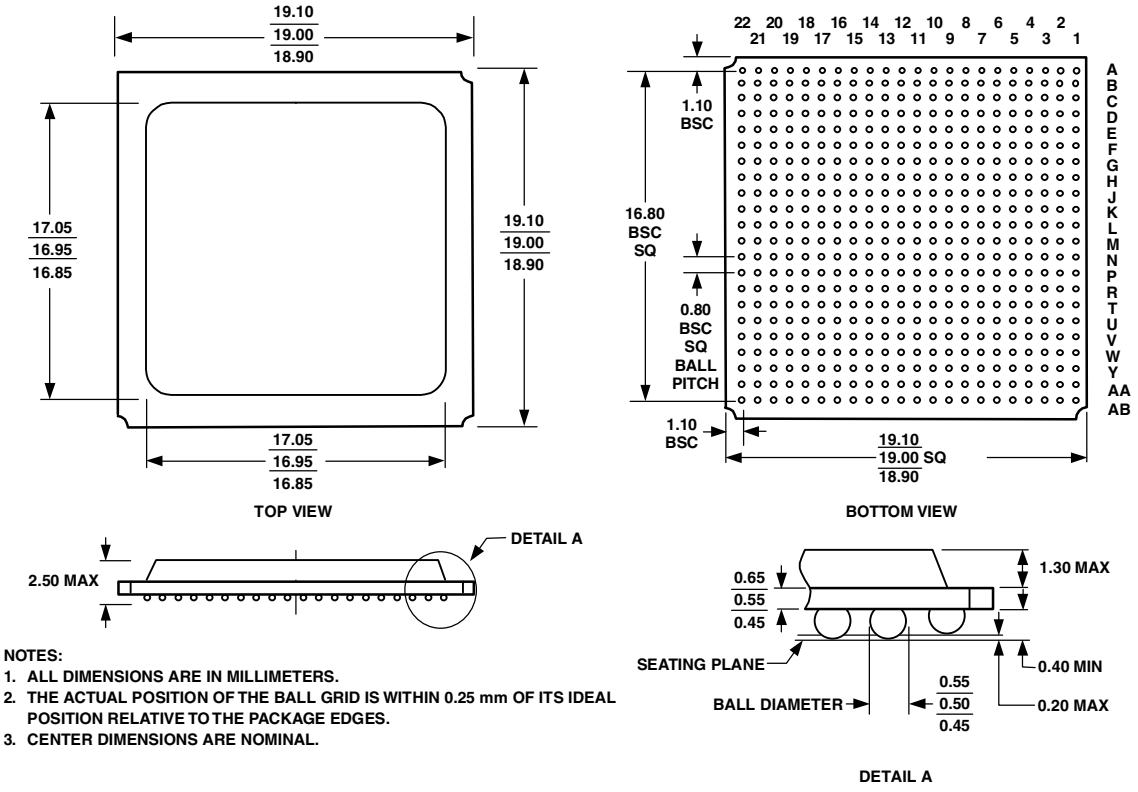

Figure 43. 484-Ball PBGA (B-484)

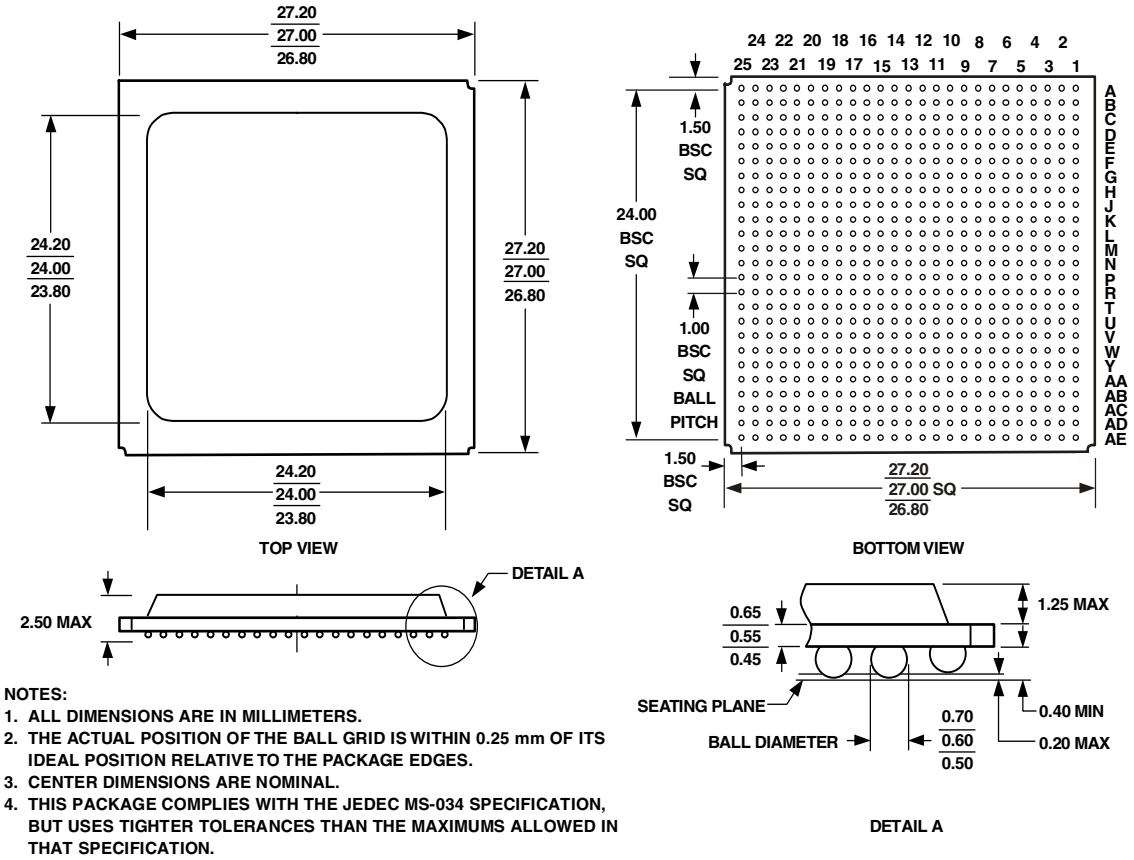

Figure 44. 625-Ball PBGA (B-625)

SURFACE-MOUNT DESIGN

The following table is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
625-ball (27 mm) PBGA	Solder Mask Defined (SMD)	0.45 mm diameter	0.60 mm diameter
484-ball (19 mm) PBGA	Solder Mask Defined (SMD)	0.40 mm diameter	0.53 mm diameter

ORDERING GUIDE

Part Number[1, 2, 3, 4]	Temperature Range (Case)	Core Clock (CCLK) Rate[5]	On-Chip SRAM	Package Description	Package Option
ADSP-TS101SAB1-000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1-100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB2-000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2-100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]

[1] S indicates 1.2 V and 3.3 V supplies.
[2] A indicates –40°C to +85°C temperature.
[3] 000 indicates 250 MHz speed grade; 100 indicates 300 MHz speed grade.
[4] Z indicates RoHS compliant part.
[5] The instruction rate runs at the internal DSP clock (CCLK) rate.
[6] The B-625 package measures 27 mm × 27 mm.
[7] The B-484 package measures 19 mm × 19 mm.