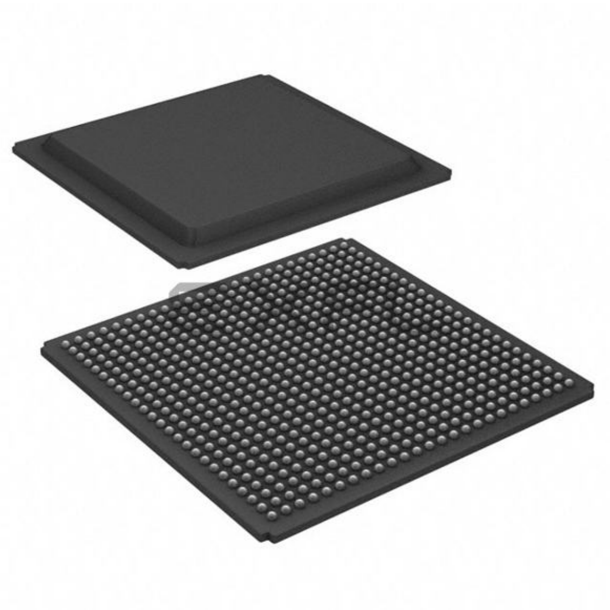

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	250MHz
Non-Volatile Memory	External
On-Chip RAM	768kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	625-BBGA
Supplier Device Package	625-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts101sab1z000

The ADSP-TS101S, in most cases, has a two-cycle arithmetic execution pipeline that is fully interlocked, so whenever a computation result is unavailable for another operation dependent on it, the DSP automatically inserts one or more stall cycles as needed. Efficient programming with dependency-free instructions can eliminate most computational and memory transfer data dependencies.

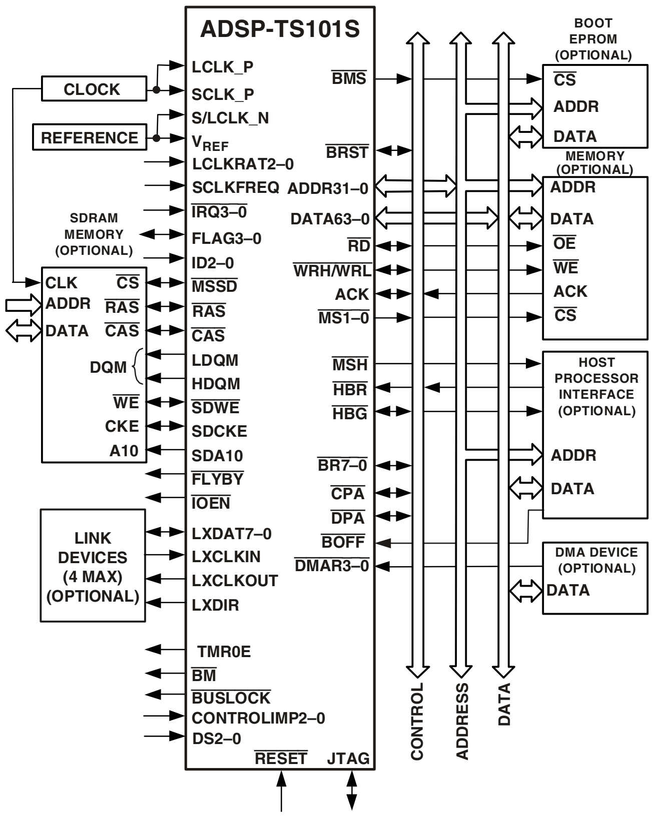

Figure 2. Single-Processor System with External SDRAM

In addition, the ADSP-TS101S supports SIMD operations two ways—SIMD compute blocks and SIMD computations. The programmer can direct both compute blocks to operate on the same data (broadcast distribution) or on different data (merged distribution). In addition, each compute block can execute four 16-bit or eight 8-bit SIMD computations in parallel.

DUAL COMPUTE BLOCKS

The ADSP-TS101S has compute blocks that can execute computations either independently or together as a SIMD engine. The DSP can issue up to two compute instructions per compute block each cycle, instructing the ALU, multiplier, or shifter to perform independent, simultaneous operations.

The compute blocks are referred to as X and Y in assembly syntax, and each block contains three computational units—an ALU, a multiplier, a 64-bit shifter, and a 32-word register file.

- Register file—each compute block has a multiported 32-word, fully orthogonal register file used for transferring data between the computation units and data buses and for storing intermediate results. Instructions can access the registers in the register file individually (word aligned), or in sets of two (dual aligned) or four (quad aligned).
- ALU—the ALU performs a standard set of arithmetic operations in both fixed- and floating-point formats. It also performs logic operations.
- Multiplier—the multiplier performs both fixed- and floating-point multiplication and fixed-point multiply and accumulate.
- Shifter—the 64-bit shifter performs logical and arithmetic shifts, bit and bit stream manipulation, and field deposit and extraction operations.
- Accelerator—128-bit unit for trellis decoding (for example, Viterbi and turbo decoders) and complex correlations for communication applications.

Using these features, the compute blocks can:

- Provide 8 MACs per cycle peak and 7.1 MACs per cycle sustained 16-bit performance and provide 2 MACs per cycle peak and 1.8 MACs per cycle sustained 32-bit performance (based on FIR)
- Execute six single-precision, floating-point or execute 24 fixed-point (16-bit) operations per cycle, providing 1,800 MFLOPS or 7.3 GOPS performance
- Perform two complex 16-bit MACs per cycle
- Execute eight trellis butterflies in one cycle

DATA ALIGNMENT BUFFER (DAB)

The DAB is a quad word FIFO that enables loading of quad word data from nonaligned addresses. Normally, load instructions must be aligned to their data size so that quad words are loaded from a quad-aligned address. Using the DAB significantly improves the efficiency of some applications, such as FIR filters.

DUAL INTEGER ALUS (IALUS)

The ADSP-TS101S has two IALUs that provide powerful address generation capabilities and perform many general-purpose integer operations. Each of the IALUs:

- Provides memory addresses for data and update pointers
- Supports circular buffering and bit-reverse addressing
- Performs general-purpose integer operations, increasing programming flexibility
- Includes a 31-word register file for each IALU

As address generators, the IALUs perform immediate or indirect (pre- and post-modify) addressing. They perform modulus and bit-reverse operations with no constraints placed on memory addresses for the modulus data buffer placement. Each IALU can specify either a single, dual, or quad word access from memory.

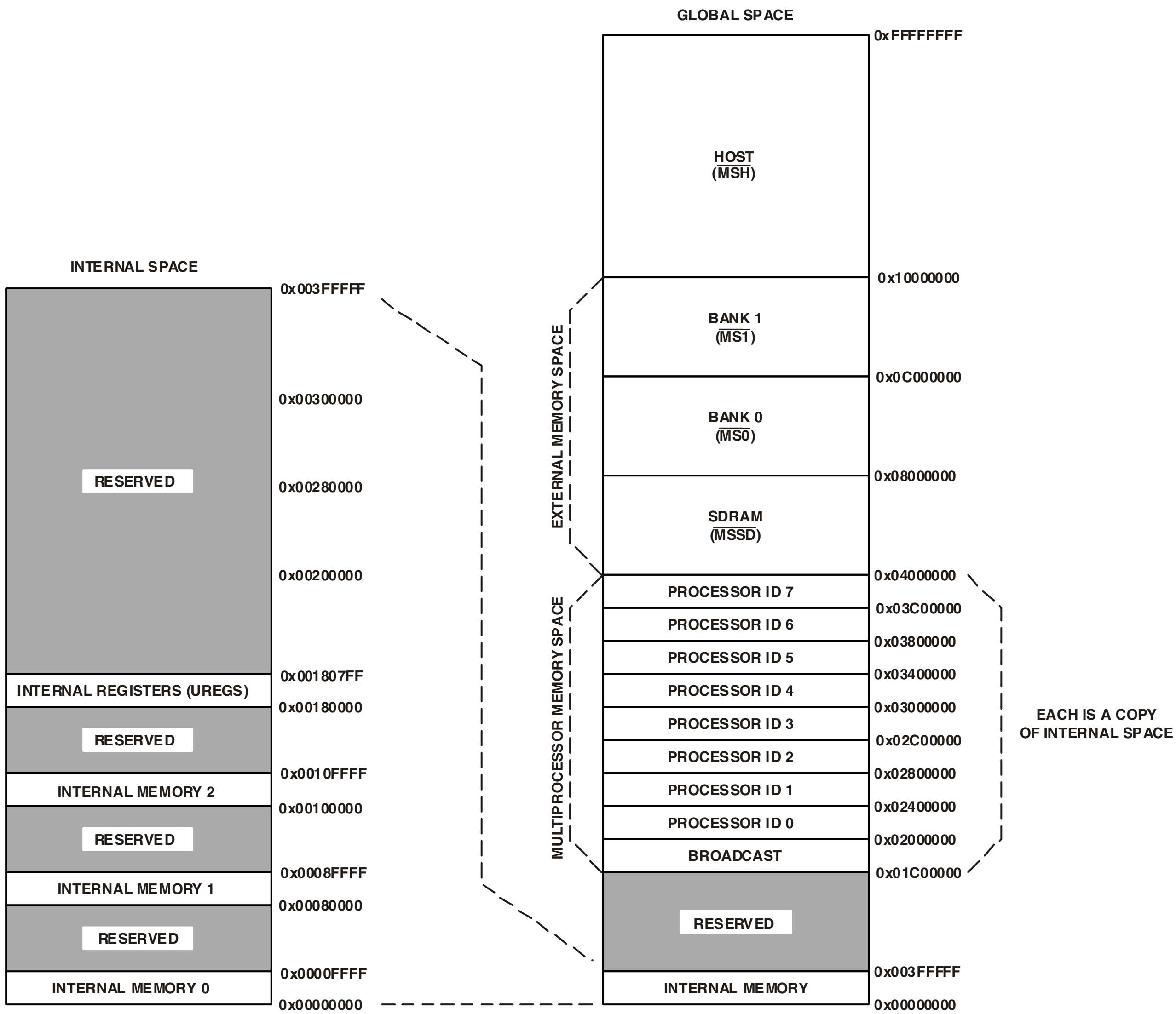

Figure 3. Memory Map

EXTERNAL PORT
(OFF-CHIP MEMORY/PERIPHERALS INTERFACE)

The ADSP-TS101S processor's external port provides the processor's interface to off-chip memory and peripherals. The 4G word address space is included in the DSP's unified address space. The separate on-chip buses—three 128-bit data buses and three 32-bit address buses—are multiplexed at the external port to create an external system bus with a single 64-bit data bus and a single 32-bit address bus. The external port supports data transfer rates of 800M bytes per second over external bus.

The external bus can be configured for 32- or 64-bit operation. When the system bus is configured for 64-bit operation, the lower 32 bits of the external data bus connect to even addresses, and the upper 32 bits connect to odd addresses.

The external port supports pipelined, slow, and SDRAM protocols. Addressing of external memory devices and memory-mapped peripherals is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals.

The ADSP-TS101S provides programmable memory, pipeline depth, and idle cycle for synchronous accesses, and external acknowledge controls to support interfacing to pipelined or slow devices, host processors, and other memory-mapped peripherals with variable access, hold, and disable time requirements.

Host Interface

The ADSP-TS101S provides an easy and configurable interface between its external bus and host processors through the external port. To accommodate a variety of host processors, the host interface supports pipelined or slow protocols for accesses of the host as slave. Each protocol has programmable transmission parameters, such as idle cycles, pipe depth, and internal wait cycles.

The host interface supports burst transactions initiated by a host processor. After the host issues the starting address of the burst and asserts the $\overline{\text{BRST}}$ signal, the DSP increments the address internally while the host continues to assert $\overline{\text{BRST}}$.

The host interface provides a deadlock recovery mechanism that enables a host to recover from deadlock situations involving the DSP. The $\overline{\text{BOFF}}$ signal provides the deadlock recovery mechanism. When the host asserts $\overline{\text{BOFF}}$, the DSP backs off the current transaction and asserts $\overline{\text{HBG}}$ and relinquishes the external bus.

The host can directly read or write the internal memory of the ADSP-TS101S, and it can access most of the DSP registers, including DMA control (TCB) registers. Vector interrupts support efficient execution of host commands.

Multiprocessor Interface

The ADSP-TS101S offers powerful features tailored to multiprocessing DSP systems through the external port and link ports. This multiprocessing capability provides highest bandwidth for interprocessor communication, including:

- Up to eight DSPs on a common bus
- On-chip arbitration for glueless multiprocessing
- Link ports for point-to-point communication

The external port and link ports provide integrated, glueless multiprocessing support.

The external port supports a unified address space (see Figure 3) that enables direct interprocessor accesses of each ADSP-TS101S processor's internal memory and registers. The DSP's on-chip distributed bus arbitration logic provides simple, glueless connection for systems containing up to eight ADSP-TS101S processors and a host processor. Bus arbitration has a rotating priority. Bus lock supports indivisible read-modify-write sequences for semaphores. A bus fairness feature prevents one DSP from holding the external bus too long.

The DSP's four link ports provide a second path for interprocessor communications with throughput of 1G bytes per second. The cluster bus provides 800M bytes per second throughput—with a total of 1.8G bytes per second interprocessor bandwidth.

SDRAM Controller

The SDRAM controller controls the ADSP-TS101S processor's transfers of data to and from synchronous DRAM (SDRAM). The throughput is 32 or 64 bits per SCLK cycle using the external port and SDRAM control pins.

The SDRAM interface provides a glueless interface with standard SDRAMs—16M bit, 64M bit, 128M bit, and 256M bit. The DSP directly supports a maximum of 64M words × 32 bits of SDRAM. The SDRAM interface is mapped in external memory in the DSP's unified memory map.

EPROM Interface

The ADSP-TS101S can be configured to boot from external 8-bit EPROM at reset through the external port. An automatic process (which follows reset) loads a program from the EPROM into internal memory. This process uses 16 wait cycles for each read access. During booting, the $\overline{\text{BMS}}$ pin functions as the EPROM chip select signal. The EPROM boot procedure uses DMA Channel 0, which packs the bytes into 32-bit instructions. Applications can also access the EPROM (write flash memories) during normal operation through DMA.

The EPROM or flash memory interface is not mapped in the DSP's unified memory map. It is a byte address space limited to a maximum of 16M bytes (24 address bits). The EPROM or flash memory interface can be used after boot via a DMA.

DMA CONTROLLER

The ADSP-TS101S processor's on-chip DMA controller, with 14 DMA channels, provides zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the DSP's core, enabling DMA operations to occur while the DSP's core continues to execute program instructions. The DMA controller performs DMA transfers between:

- Internal memory and external memory and memory-mapped peripherals
- Internal memory of other DSPs on a common bus, a host processor, or link port I/O
- External memory and external peripherals or link port I/O
- External bus master and internal memory or link port I/O

The DMA controller provides a number of additional features.

The DMA controller supports flyby transfers. Flyby operations only occur through the external port (DMA Channel 0) and do not involve the DSP's core. The DMA controller acts as a conduit to transfer data from one external device to another through external memory. During a transaction, the DSP:

- Relinquishes the external data bus
- Outputs addresses, memory selects ($\overline{\text{MS1–0}}$, $\overline{\text{MSSD}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{SDWE}}$) and the $\overline{\text{FLYBY}}$, $\overline{\text{IOEN}}$, and RD/$\overline{\text{WR}}$ strobes
- Responds to ACK

DMA chaining is also supported by the DMA controller. DMA chaining operations enable applications to automatically link one DMA transfer sequence to another for continuous transmission. The sequences can occur over different DMA channels and have different transmission attributes.

The DMA controller also supports two-dimensional transfers. The DMA controller can access and transfer two-dimensional memory arrays on any DMA transmit or receive channel. These transfers are implemented with index, count, and modify registers for both the X and Y dimensions.

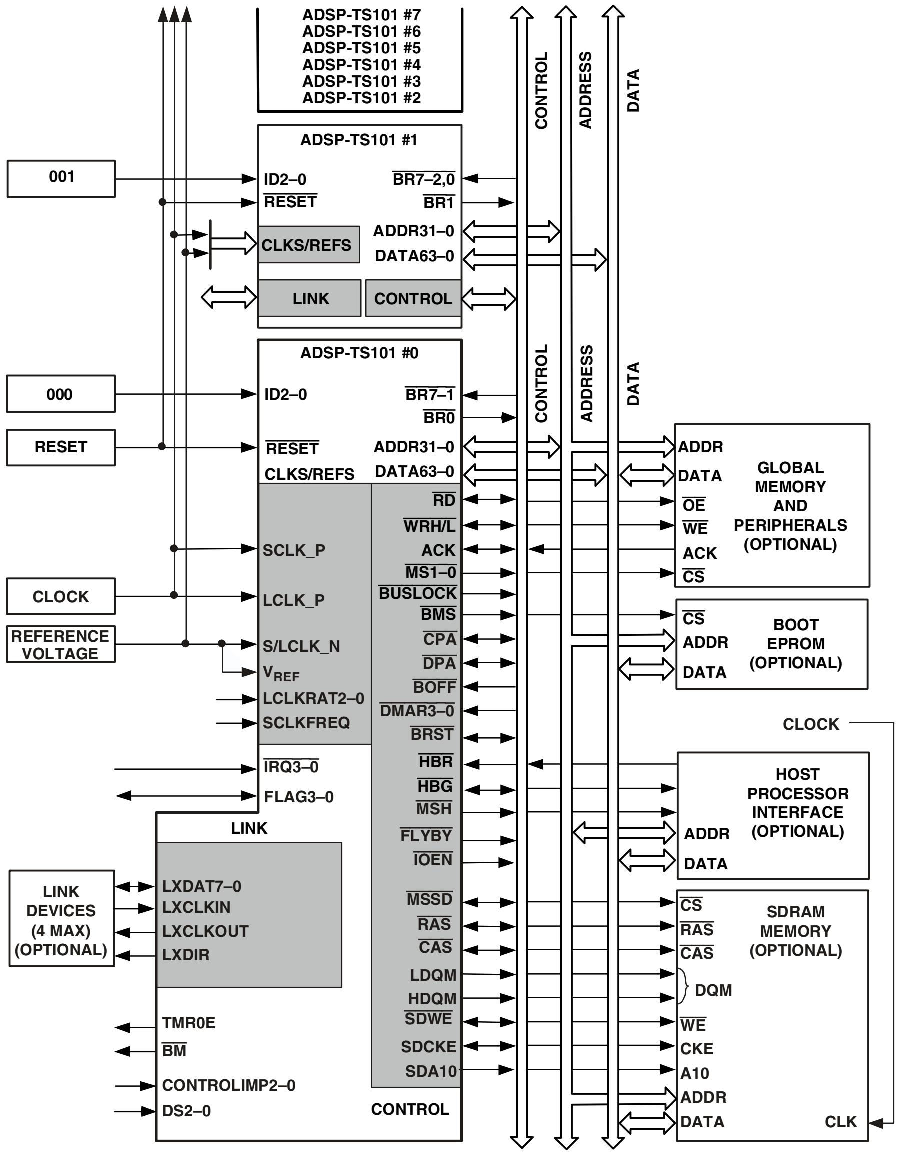

Figure 4. Shared Memory Multiprocessing System

The DMA controller performs the following DMA operations:

- External port block transfers. Four dedicated bidirectional DMA channels transfer blocks of data between the DSP's internal memory and any external memory or memory-mapped peripheral on the external bus. These transfers support master mode and handshake mode protocols.
- Link port transfers. Eight dedicated DMA channels (four transmit and four receive) transfer quad word data only between link ports and between a link port and internal or external memory. These transfers only use handshake mode protocol. DMA priority rotates between the four receive channels.
- AutoDMA transfers. Two dedicated unidirectional DMA channels transfer data received from an external bus master to internal memory or to link port I/O. These transfers only use slave mode protocol, and an external bus master must initiate the transfer.

LINK PORTS

The DSP's four link ports provide additional 8-bit bidirectional I/O capability. With the ability to operate at a double data rate—latching data on both the rising and falling edges of the clock—running at 125 MHz, each link port can support up to 250M bytes per second, for a combined maximum throughput of 1G bytes per second.

The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications. Applications can also use the link ports for booting.

Each link port has its own double-buffered input and output registers. The DSP's core can write directly to a link port's transmit register and read from a receive register, or the DMA controller can perform DMA transfers through eight (four transmit and four receive) dedicated link port DMA channels.

Each link port has three signals that control its operation. LxCLKOUT and LxCLKIN implement clock/acknowledge handshaking. LxDIR indicates the direction of transfer and is used only when buffering the LxDAT signals. An example application would be using differential low-swing buffers for long twisted-pair wires. LxDAT provides the 8-bit data bus input/output.

Applications can program separate error detection mechanisms for transmit and receive operations (applications can use the checksum mechanism to implement consecutive link port transfers), the size of data packets, and the speed at which bytes are transmitted.

Under certain conditions, the link port receiver can initiate a token switch to reverse the direction of transfer; the transmitter becomes the receiver and vice versa.

TIMER AND GENERAL-PURPOSE I/O

The ADSP-TS101S has a timer pin (TMR0E) that generates output when a programmed timer counter has expired. Also, the DSP has four programmable general-purpose I/O pins (FLAG3–0) that can function as either single-bit input or output. As outputs, these pins can signal peripheral devices; as inputs, they can provide the test for conditional branching.

RESET AND BOOTING

The ADSP-TS101S has two levels of reset (see reset specifications Page 24):

- Power-up reset—after power-up of the system, and strap options are stable, the $\overline{\text{RESET}}$ pin must be asserted (low).
- Normal reset—for any resets following the power-up reset sequence, the $\overline{\text{RESET}}$ pin must be asserted.

The DSP can be reset internally (core reset) by setting the SWRST bit in SQCTL. The core is reset, but not the external port or I/O.

After reset, the ADSP-TS101S has four boot options for beginning operation:

- Boot from EPROM. The DSP defaults to EPROM booting when the $\overline{\text{BMS}}$ pin strap option is set low. See Strap Pin Function Descriptions on Page 19.
- Boot by an external master (host or another ADSP-TS101S). Any master on the cluster bus can boot the ADSP-TS101S through writes to its internal memory or through autoDMA.
- Boot by link port. All four receive link DMA channels are initialized after reset to transfer a 256-word block to internal memory address 0 to 255, and to issue an interrupt at the end of the block (similar to EP DMA). The corresponding DMA interrupts are set to address zero (0).
- No boot—Start running from an external memory. Using the "no boot" option, the ADSP-TS101S must start running from an external memory, caused by asserting one of the $\overline{\text{IRQ3–0}}$ interrupt signals.

The ADSP-TS101S core always exits from reset in the idle state and waits for an interrupt. Some of the interrupts in the interrupt vector table are initialized and enabled after reset.

LOW POWER OPERATION

The ADSP-TS101S can enter a low power sleep mode in which its core does not execute instructions, reducing power consumption to a minimum. The ADSP-TS101S exits sleep mode when it senses a falling edge on any of its $\overline{\text{IRQ3–0}}$ interrupt inputs. The interrupt, if enabled, causes the ADSP-TS101S to execute the corresponding interrupt service routine. This feature is useful for systems that require a low power standby mode.

CLOCK DOMAINS

As shown in Figure 5, the ADSP-TS101S has two clock inputs, SCLK (system clock) and LCLK (local clock).

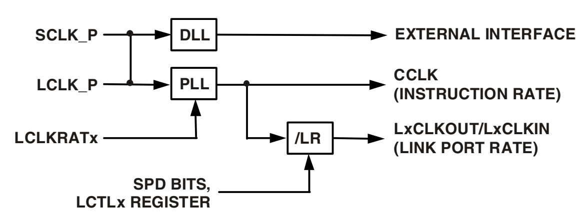

Figure 5. Clock Domains

These inputs drive its two major clock domains:

- SCLK (system clock). Provides clock input for the external bus interface and defines the ac specification reference for the external bus signals. The external bus interface runs at 1× the SCLK frequency. A DLL locks internal SCLK to SCLK input.
- LCLK (local clock). Provides clock input to the internal clock driver, CCLK, which is the internal clock for the core, internal buses, memory, and link ports. The instruction execution rate is equal to CCLK. A PLL from LCLK gener-

Table 5. Pin Definitions—External Port Bus Controls

Signal	Type	Term	Description
ADDR31–0[1]	I/O/T	nc	Address Bus. The DSP issues addresses for accessing memory and peripherals on these pins. In a multiprocessor system, the bus master drives addresses for accessing internal memory or I/O processor registers of other ADSP-TS101S processors. The DSP inputs addresses when a host or another DSP accesses its internal memory or I/O processor registers.
DATA63–0[1]	I/O/T	nc	External Data Bus. Data and instructions are received, and driven by the DSP, on these pins.
$\overline{\text{RD}}$[2]	I/O/T (pu[3])	nc	Memory Read. $\overline{\text{RD}}$ is asserted whenever the DSP reads from any slave in the system, excluding SDRAM. When the DSP is a slave, $\overline{\text{RD}}$ is an input and indicates read transactions that access its internal memory or universal registers. In a multiprocessor system, the bus master drives $\overline{\text{RD}}$. The $\overline{\text{RD}}$ pin changes concurrently with ADDR pins.
$\overline{\text{WRL}}$[2]	I/O/T (pu[3])	nc	Write Low. $\overline{\text{WRL}}$ is asserted in two cases: When the ADSP-TS101S writes to an even address word of external memory or to another external bus agent; and when the ADSP-TS101S writes to a 32-bit zone (host, memory, or DSP programmed to 32-bit bus). An external master (host or DSP) asserts $\overline{\text{WRL}}$ for writing to a DSP's low word of internal memory. In a multiprocessor system, the bus master drives $\overline{\text{WRL}}$. The $\overline{\text{WRL}}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{\text{WRL}}$ is an input and indicates write transactions that access its internal memory or universal registers.
$\overline{\text{WRH}}$[2]	I/O/T (pu[3])	nc	Write High. $\overline{\text{WRH}}$ is asserted when the ADSP-TS101S writes a long word (64 bits) or writes to an odd address word of external memory or to another external bus agent on a 64-bit data bus. An external master (host or another DSP) must assert $\overline{\text{WRH}}$ for writing to a DSP's high word of 64-bit data bus. In a multiprocessing system, the bus master drives $\overline{\text{WRH}}$. The $\overline{\text{WRH}}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{\text{WRH}}$ is an input and indicates write transactions that access its internal memory or universal registers.
ACK	I/O/T	epu	Acknowledge. External slave devices can deassert ACK to add wait states to external memory accesses. ACK is used by I/O devices, memory controllers, and other peripherals on the data phase. The DSP can deassert ACK to add wait states to read accesses of its internal memory. The ADSP-TS101S does not drive ACK during slave writes. Therefore, an external (approximately 10 kΩ) pull-up is required.
$\overline{\text{BMS}}$[2,4]	O/T (pu/pd[3])	au	Boot Memory Select. $\overline{\text{BMS}}$ is the chip select for boot EPROM or flash memory. During reset, the DSP uses $\overline{\text{BMS}}$ as a strap pin (EBOOT) for EPROM boot mode. When the DSP is configured to boot from EPROM, $\overline{\text{BMS}}$ is active during the boot sequence. Pull-down enabled during $\overline{\text{RESET}}$ (asserted); pull-up enabled after $\overline{\text{RESET}}$ (deasserted). In a multiprocessor system, the DSP bus master drives $\overline{\text{BMS}}$. For details see Reset and Booting on Page 9 and the EBOOT signal description in Table 16 on Page 19.
$\overline{\text{MS1–0}}$[2]	O/T (pu[3])	nc	Memory Select. $\overline{\text{MS0}}$ or $\overline{\text{MS1}}$ is asserted whenever the DSP accesses memory banks 0 or 1, respectively. $\overline{\text{MS1–0}}$ are decoded memory address pins that change concurrently with ADDR pins. When ADDR31:26 = 0b000010, $\overline{\text{MS0}}$ is asserted. When ADDR31:26 = 0b000011, $\overline{\text{MS1}}$ is asserted. In multiprocessor systems, the master DSP drives $\overline{\text{MS1–0}}$.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

Table 8. Pin Definitions—External Port SDRAM Controller

Signal	Type	Term	Description
$\overline{\text{MSSD}}$[1]	I/O/T (pu[2])	nc	Memory Select SDRAM. $\overline{\text{MSSD}}$ is asserted whenever the DSP accesses SDRAM memory space. $\overline{\text{MSSD}}$ is a decoded memory address pin that is asserted whenever the DSP issues an SDRAM command cycle (access to ADDR31:26 = 0b000001). MSSD in a multiprocessor system is driven by the master DSP.
$\overline{\text{RAS}}$[1]	I/O/T (pu[2])	nc	Row Address Select. When sampled low, $\overline{\text{RAS}}$ indicates that a row address is valid in a read or write of SDRAM. In other SDRAM accesses, RAS defines the type of operation to execute according to SDRAM specification.
$\overline{\text{CAS}}$[1]	I/O/T (pu[2])	nc	Column Address Select. When sampled low, $\overline{\text{CAS}}$ indicates that a column address is valid in a read or write of SDRAM. In other SDRAM accesses, $\overline{\text{CAS}}$ defines the type of operation to execute according to the SDRAM specification.
LDQM[1]	O/T (pu[2])	nc	Low Word SDRAM Data Mask. When LDQM is sampled high, the DSP three-states the SDRAM DQ buffers. LDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted and is inactive on read transactions. On write transactions, LDQM is active when accessing an odd address word on a 64-bit memory bus to disable the write of the low word.
HDQM[1]	O/T (pu[2])	nc	High Word SDRAM Data Mask. When HDQM is sampled high, the DSP three-states the SDRAM DQ buffers. HDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted and is inactive on read transactions. On write transactions, HDQM is active when accessing an even address in word accesses or is active when memory is configured for a 32-bit bus to disable the write of the high word.
SDA10[1]	O/T (pu[2])	nc	SDRAM Address bit 10 pin. Separate A10 signals enable SDRAM refresh operation while the DSP executes non-SDRAM transactions.
SDCKE[1, 3]	I/O/T (pu/pd[2])	nc	SDRAM Clock Enable. Activates the SDRAM clock for SDRAM self-refresh or suspend modes. A slave DSP in a multiprocessor system does not have the pull-up or pull-down. A master DSP (or ID = 0 in a single processor system) has a 100 kΩ pull-up before granting the bus to the host, except when the SDRAM is put in self-refresh mode. In self-refresh mode, the master has a 100 kΩ pull-down before granting the bus to the host.
$\overline{\text{SDWE}}$[1]	I/O/T (pu[2])	nc	SDRAM Write Enable. When sampled low while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM write access. When sampled high while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM read access. In other SDRAM accesses, $\overline{\text{SDWE}}$ defines the type of operation to execute according to SDRAM specification.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.

Table 9. Pin Definitions—JTAG Port

Signal	Type	Term	Description
$\overline{\text{EMU}}$	O (o/d)	nc[1]	Emulation. Connected only to the DSP's JTAG emulator target board connector.
TCK	I	epd or epu[1]	Test Clock (JTAG). Provides an asynchronous clock for JTAG scan.
TDI[2]	I (pu[3])	nc[1]	Test Data Input (JTAG). A serial data input of the scan path.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

Table 15. Pin Definitions—Power, Ground, and Reference

Signal	Type	Term	Description
V_{DD}	P	au	V_{DD} pins for internal logic.
V_{DD_A}	P	au	V_{DD} pins for analog circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	au	V_{DD} pins for I/O buffers.
V_{REF}	I	au	Reference voltage defines the trip point for all input buffers, except $\overline{\text{RESET}}$, $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, ID2–0, CONTROLIMP2–0, TCK, TDI, TMS, and $\overline{\text{TRST}}$. The value is 1.5 V ± 100 mV (which is the TTL trip point). V_{REF} can be connected to a power supply or set by a voltage divider circuit. The voltage divider should have an HF decoupling capacitor (1 nF HF SMD) connected to V_{SS}. Tie the decoupling capacitor between V_{REF} input and V_{SS}, as close to the DSP's pins as possible. For more information, see Filtering Reference Voltage and Clocks on Page 10.
V_{SS}	G	au	Ground pins.
V_{SS_A}	G	au	Ground pins for analog circuits.
NC			No connect. Do not connect these pins to anything (not to any supply, signal, or each other), because they are reserved and must be left unconnected.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set DSP operating modes. During reset, the DSP samples the strap option pins. Strap pins have an approximately 100 kΩ pull-down for the default value. If a strap pin is not connected to an external pull-up or logic load, the DSP samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up. In a multiprocessor system, up to eight DSPs may be connected on the cluster bus, resulting in parallel combination of strap pin pull-down resistors. Table 16 lists and describes each of the DSP's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	On Pin …	Description
EBOOT	$\overline{\text{BMS}}$	EPROM boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot DSP through the external port or a link port
IRQEN	$\overline{\text{BM}}$	Interrupt Enable. 0 = disable and set $\overline{\text{IRQ3–0}}$ interrupts to level sensitive after reset (default) 1 = enable and set $\overline{\text{IRQ3–0}}$ interrupts to edge sensitive immediately after reset
TM1	L2DIR	Test Mode 1. 0 = required setting during reset. 1 = reserved.
TM2	TMR0E	Test Mode 2. 0 = required setting during reset. 1 = reserved.

For power-up sequencing, power-up reset, and normal reset (hot reset) timing requirements, refer to Table 26 and Figure 13, Table 27 and Figure 14, and Table 28, and Figure 15 respectively.

Table 19. AC Asynchronous Signal Specifications (All values in this table are in nanoseconds)

Name	Description	Pulse Width Low (min)	Pulse Width High (min)
$\overline{\text{IRQ3–0}}$[1]	Interrupt request input	t_{CCLK} + 3 ns	
$\overline{\text{DMAR3–0}}$[1]	DMA request input	t_{CCLK} + 4 ns	t_{CCLK} + 4 ns
TMR0E[2]	Timer 0 expired output		4 × t_{SCLK} ns
FLAG3–0[1, 3]	Flag pins input	3 × t_{CCLK} ns	3 × t_{CCLK} ns
$\overline{\text{TRST}}$	JTAG test reset input	1 ns	

[1] These input pins do not need to be synchronized to a clock reference.
[2] This pin is a strap option. During reset, an internal resistor pulls the pin low.
[3] For output specifications, see Table 29 and Table 30.

Table 20. Reference Clocks—Core Clock (CCLK) Cycle Time

		Grade = 100 (300 MHz)		Grade = 000 (250 MHz)		
Parameter	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{CCLK}[1]	Core Clock Cycle Time	3.3	12.5	4.0	12.5	ns

[1] CCLK is the internal processor clock or instruction cycle time. The period of this clock is equal to the system clock period (t_{SCLK}) divided by the system clock ratio (SCLKRAT2–0). For information on available part numbers for different internal processor clock rates, see the Ordering Guide on Page 45.

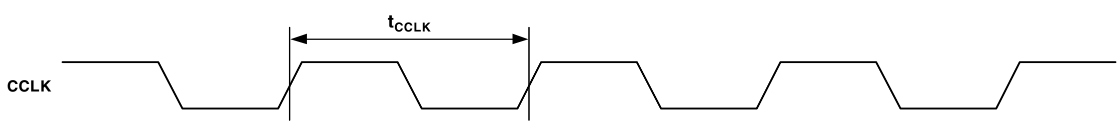

Figure 9. Reference Clocks—Core Clock (CCLK) Cycle Time

Table 21. Reference Clocks—Local Clock (LCLK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{LCLK}[1, 2, 3, 4]	Local Clock Cycle Time	10	25	ns
t_{LCLKH}	Local Clock Cycle High Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKL}	Local Clock Cycle Low Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKJ}[5, 6]	Local Clock Jitter Tolerance		500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] LCLK_P and SCLK_P must be connected to the same source.
[4] The value of (t_{LCLK} / LCLKRAT2-0) must not violate the specification for t_{CCLK}.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

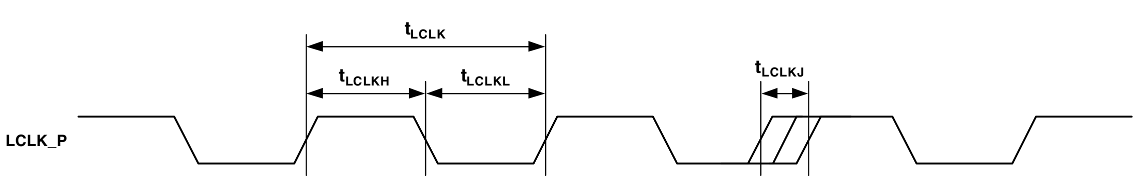

Figure 10. Reference Clocks—Local Clock (LCLK) Cycle Time

Table 27. AC Signal Specifications (for SCLK <16.7 ns) (All values in this table are in nanoseconds)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
ADDR31–0	External Address Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
DATA63–0	External Data Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSH}}$	Memory Select Host Line			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSSD}}$	Memory Select SDRAM Line	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RD}}$	Memory Read	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRL}}$	Write Low Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRH}}$	Write High Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
ACK	Acknowledge for Data	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
SDCKE	SDRAM Clock Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RAS}}$	Row Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CAS}}$	Column Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
LDQM	Low Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
HDQM	High Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
SDA10	SDRAM ADDR10			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{HBR}}$	Host Bus Request	2.6	0.5					SCLK
$\overline{\text{HBG}}$	Host Bus Grant	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BOFF}}$	Back Off Request	2.6	0.5					SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BRST}}$	Burst Access	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request	2.6	0.5	4.2	1.0			SCLK
$\overline{\text{FLYBY}}$	Flyby Mode Selection			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{IOEN}}$	Flyby I/O Enable			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CPA}}$ [3, 4]	Core Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{DPA}}$ [3, 4]	DMA Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{BMS}}$[5]	Boot Memory Select			4.2	1.0	0.9	2.5	SCLK
FLAG3–0[6]	FLAG Pins			4.2	1.0	1.0	4.0	SCLK
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	1.0			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

[1] The output valid (max) value in this column applies for the standard 30 pF capacitive load used in testing. To see how output valid varies with capacitive loading, see Figure 40 on Page 36.
[2] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.
[3] CPA and DPA pins are open drains and have 0.5 kΩ internal pull-ups.
[4] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference. These synchronous specifications only apply for recognition in the current clock reference cycle.
[5] This pin is a strap option. During reset, an internal resistor pulls the pin low.
[6] For input specifications, see Table 21.
[7] For additional requirement details, see Reset and Booting on Page 9.
[8] TCK_FE indicates TCK falling edge.
[9] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.
[10] Reference clock depends on function.
[11] System inputs are: IRQ3–0, BMS, LCLKRAT2–0, SCLKFREQ, BM, TMR0E, FLAG3–0, ID2–0, BRST, WRH, WRL, RD, MSSD, SDCKE, SDWE, CAS, RAS, ADDR31–0, DATA63–0, DPA, CPA, HBG, BOFF, HBR, ACK, BR7–0, L0CLKIN, L0DAT7–0, L1CLKIN, L1DAT7–0, L2CLKIN, L2DAT7–0, L2DIR, L3CLKIN, L3DAT7–0, DS2–0, CONTROLIMP2–0, RESET, DMAR3–0.
[12] System outputs are: BMS, BM, BUSLOCK, TMR0E, FLAG3–0, FLYBY, IOEN, MSH, BRST, WRH, WRL, RD, MS1–0, HDQM, LDQM, MSSD, SDCKE, SDWE, CAS, RAS, ADDR31–0, DATA63–0, DPA, CPA, HBG, ACK, BR7–0, L0CLKOUT, L0DAT7–0, L0DIR, L1CLKOUT, L1DAT7–0, L1DIR, L2CLKOUT, L2DAT7–0, L2DIR, L3CLKOUT, L3DAT7–0, L3DIR, EMU.

Table 28. AC Signal Specifications (for 16.7 ns <SCLK <25 ns) (All values in this table are in nanoseconds)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
ADDR31–0	External Address Bus	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
DATA63–0	External Data Bus	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
MSH	Memory Select Host Line			4.2	0.8	0.3	2.5	SCLK
MSSD	Memory Select SDRAM Line	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
MS1–0	Memory Select for Static Blocks			4.2	0.8	0.3	2.5	SCLK
RD	Memory Read	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
WRL	Write Low Word	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
WRH	Write High Word	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
ACK	Acknowledge for Data	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
SDCKE	SDRAM Clock Enable	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
RAS	Row Address Select	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
CAS	Column Address Select	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
SDWE	SDRAM Write Enable	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
LDQM	Low Word SDRAM Data Mask			4.2	0.8	0.3	2.5	SCLK
HDQM	High Word SDRAM Data Mask			4.2	0.8	0.3	2.5	SCLK
SDA10	SDRAM ADDR10			4.2	0.8	0.3	2.5	SCLK
HBR	Host Bus Request	2.8	0.5					SCLK
HBG	Host Bus Grant	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
BOFF	Back Off Request	2.8	0.5					SCLK
BUSLOCK	Bus Lock			4.2	0.8	0.3	2.5	SCLK
BRST	Burst Access	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
BR7–0	Multiprocessing Bus Request	2.8	0.5	4.2	0.8			SCLK
FLYBY	Flyby Mode Selection			4.2	0.8	0.3	2.5	SCLK
IOEN	Flyby Mode I/O Enable			4.2	0.8	0.3	2.5	SCLK
CPA[3,4]	Core Priority Access	2.8	0.5	5.8			2.5	SCLK
DPA[3,4]	DMA Priority Access	2.8	0.5	5.8			2.5	SCLK
BMS[5]	Boot Memory Select			4.2	0.8	0.3	2.5	SCLK
FLAG3–0[6]	FLAG Pins			4.2	1.0	1.0	4.0	SCLK

Table 28. AC Signal Specifications (for 16.7 ns <SCLK <25 ns) (All values in this table are in nanoseconds) (Continued)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
$\overline{\mathrm{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\mathrm{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\mathrm{BM}}$[5]	Bus Master Debug Aid Only			4.2	0.8			SCLK
$\overline{\mathrm{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

[1] The output valid (max) value in this column applies for the standard 30 pF capacitive load used in testing. To see how output valid varies with capacitive loading, see Figure 40 on Page 36.

[2] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.

[3] $\overline{\mathrm{CPA}}$ and $\overline{\mathrm{DPA}}$ pins are open drains and have 0.5 kΩ internal pull-ups.

[4] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference. These synchronous specifications only apply for recognition in the current clock reference cycle.

[5] This pin is a strap option. During reset, an internal resistor pulls the pin low.

[6] For input specifications, see Table 21.

[7] For additional requirement details, see Reset and Booting on Page 9.

[8] TCK_FE indicates TCK falling edge.

[9] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.

[10] Reference clock depends on function.

[11] System inputs are: $\overline{\mathrm{IRQ3{-}0}}$, $\overline{\mathrm{BMS}}$, LCLKRAT2–0, SCLKFREQ, $\overline{\mathrm{BM}}$, TMR0E, FLAG3–0, ID2–0, $\overline{\mathrm{BRST}}$, $\overline{\mathrm{WRH}}$, $\overline{\mathrm{WRL}}$, $\overline{\mathrm{RD}}$, $\overline{\mathrm{MSSD}}$, SDCKE, $\overline{\mathrm{SDWE}}$, $\overline{\mathrm{CAS}}$, $\overline{\mathrm{RAS}}$, ADDR31–0, DATA63–0, $\overline{\mathrm{DPA}}$, $\overline{\mathrm{CPA}}$, $\overline{\mathrm{HBG}}$, $\overline{\mathrm{BOFF}}$, $\overline{\mathrm{HBR}}$, ACK, $\overline{\mathrm{BR7{-}0}}$, L0CLKIN, L0DAT7–0, L1CLKIN, L1DAT7–0, L2CLKIN, L2DAT7–0, L2DIR, L3CLKIN, L3DAT7–0, DS2–0, CONTROLIMP2–0, $\overline{\mathrm{RESET}}$, $\overline{\mathrm{DMAR3{-}0}}$.

[12] System outputs are: $\overline{\mathrm{BMS}}$, $\overline{\mathrm{BM}}$, $\overline{\mathrm{BUSLOCK}}$, TMR0E, FLAG3–0, $\overline{\mathrm{FLYBY}}$, $\overline{\mathrm{IOEN}}$, $\overline{\mathrm{MSH}}$, $\overline{\mathrm{BRST}}$, $\overline{\mathrm{WRH}}$, $\overline{\mathrm{WRL}}$, $\overline{\mathrm{RD}}$, $\overline{\mathrm{MS1{-}0}}$, HDQM, LDQM, $\overline{\mathrm{MSSD}}$, SDCKE, $\overline{\mathrm{SDWE}}$, $\overline{\mathrm{CAS}}$, $\overline{\mathrm{RAS}}$, ADDR31–0, DATA63–0, $\overline{\mathrm{DPA}}$, $\overline{\mathrm{CPA}}$, $\overline{\mathrm{HBG}}$, ACK, $\overline{\mathrm{BR7{-}0}}$, L0CLKOUT, L0DAT7–0, L0DIR, L1CLKOUT, L1DAT7–0, L1DIR, L2CLKOUT, L2DAT7–0, L2DIR, L3CLKOUT, L3DAT7–0, L3DIR, $\overline{\mathrm{EMU}}$.

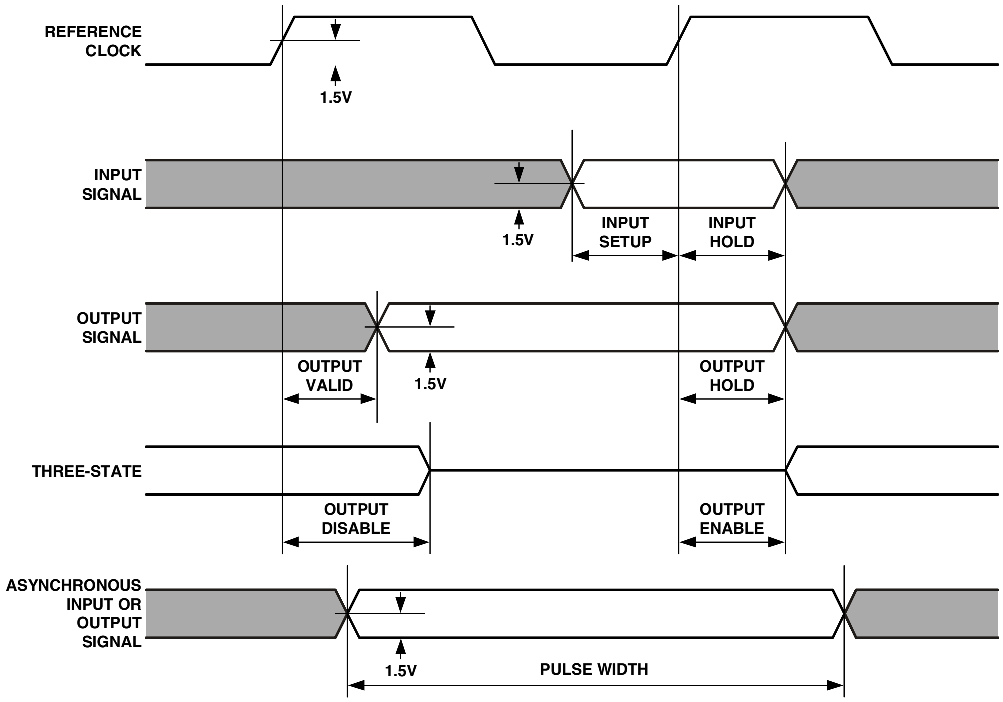

Figure 16. General AC Parameters Timing

Table 30. Link Ports—Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{LxCLK_Rx}[1, 2]	Receive Link Clock Period	$0.9 \times LR \times t_{CCLK}$	$1.1 \times LR \times t_{CCLK}$	ns
t_{LxCLKH_Rx}[3]	Receive Link Clock Width High	$0.33 \times t_{LxCLK\_Rx}$	$0.66 \times t_{LxCLK\_Rx}$	ns
t_{LxCLKH_Rx}[4]	Receive Link Clock Width High	$0.4 \times t_{LxCLK\_Rx}$	$0.6 \times t_{LxCLK\_Rx}$	ns
t_{LxCLKL_Rx}[3]	Receive Link Clock Width Low	$0.33 \times t_{LxCLK\_Rx}$	$0.66 \times t_{LxCLK\_Rx}$	ns
t_{LxCLKL_Rx}[4]	Receive Link Clock Width Low	$0.4 \times t_{LxCLK\_Rx}$	$0.6 \times t_{LxCLK\_Rx}$	ns
t_{DIS}	LxDAT7–0 Input Setup	0.6		ns
t_{DIH}	LxDAT7–0 Input Hold	0.6		ns
Switching Characteristics				
t_{CONNV}	Connectivity Pulse Valid	0	$2.5 \times t_{LxCLK\_Rx}$	ns
t_{CONNOW}	Connectivity Pulse Output Width	$1.5 \times t_{LxCLK\_Rx}$		ns

[1] The link clock ratio (LR) is 2, 3, 4, or 8 as set by the SPD bits in the LCTLx register.
[2] The maximum LxCLK is 125 MHz. LR = 2 may not be used when CCLK ≥ 250 MHz.
[3] The formula for this parameter applies when LR is 2.
[4] The formula for this parameter applies when LR is 3, 4, or 8.

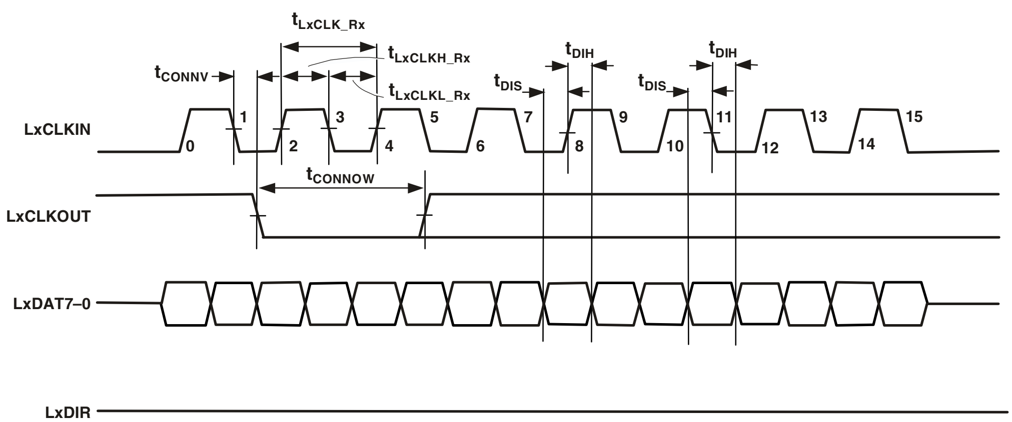

Figure 18. Link Ports—Receive

OUTPUT DRIVE CURRENTS

Figure 21 through Figure 28 show typical I–V characteristics for the output drivers of the ADSP-TS101S. The curves in these diagrams represent the current drive capability of the output drivers as a function of output voltage over the range of drive strengths. For complete output driver characteristics, refer to IBIS models, available on the Analog Devices website, www.analog.com.

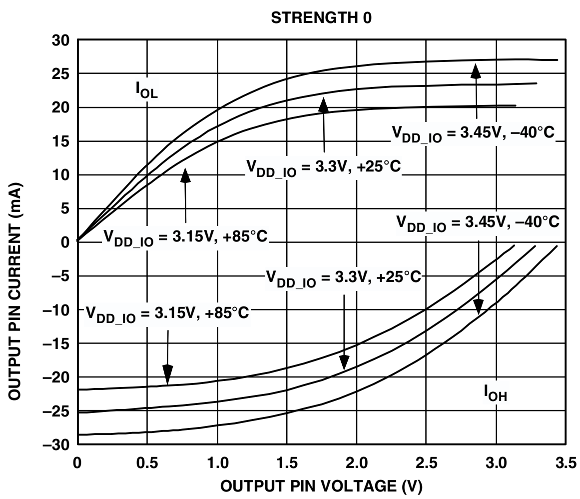

Figure 21. Typical Drive Currents at Strength 0

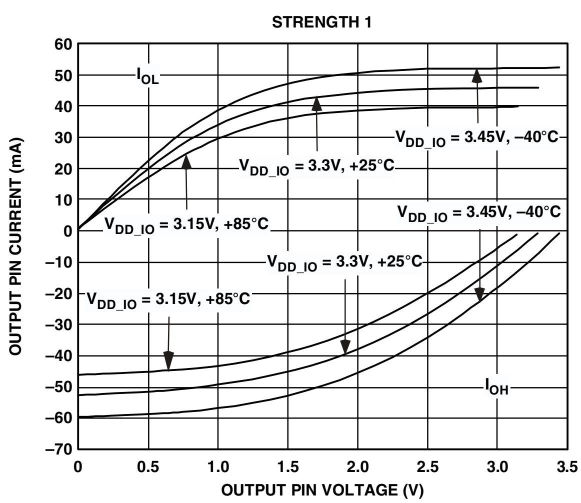

Figure 22. Typical Drive Currents at Strength 1

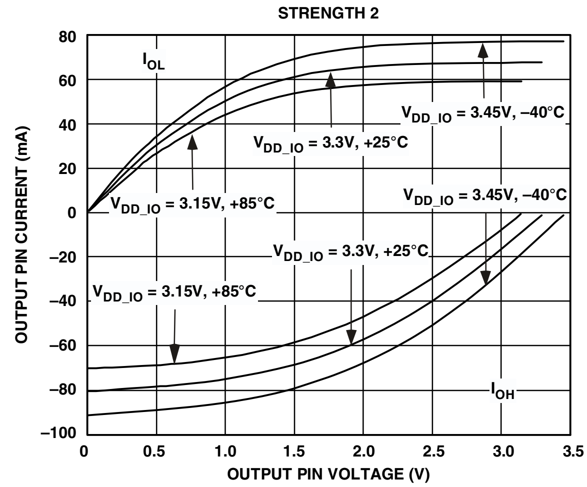

Figure 23. Typical Drive Currents at Strength 2

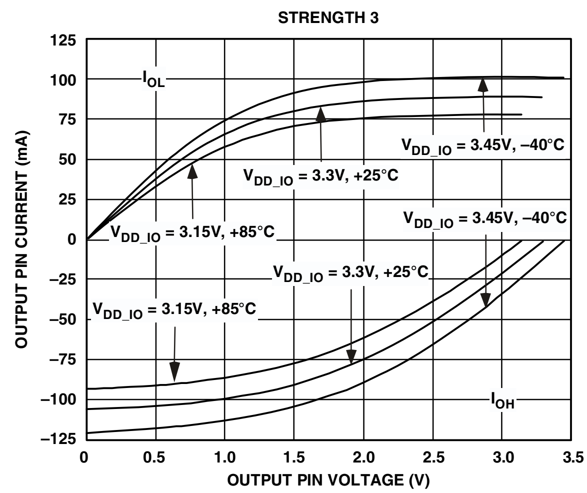

Figure 24. Typical Drive Currents at Strength 3

Table 35. 484-Ball (19 mm × 19 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
F22	TMR0E	G22	FLAG0	H22	ID1	J22	$\overline{MSH}$	K22	$\overline{WRL}$
L1	L3CLKIN	M1	L1DAT0	N1	L1DAT3	P1	L1DAT4	R1	L1DAT6
L2	NC	M2	L1DAT2	N2	L1DAT5	P2	L1CLKOUT	R2	DATA32
L3	L3DIR	M3	L1DAT1	N3	L1DAT7	P3	L1CLKIN	R3	DATA33
L4	V_{DD_IO}	M4	V_{DD_IO}	N4	V_{DD_IO}	P4	V_{DD_IO}	R4	V_{DD_IO}
L5	V_{DD}	M5	V_{SS}	N5	V_{DD_IO}	P5	V_{DD}	R5	V_{DD}
L6	V_{SS}	M6	V_{SS}	N6	V_{SS}	P6	V_{SS}	R6	V_{SS}
L7	V_{SS}	M7	V_{SS}	N7	V_{SS}	P7	V_{SS}	R7	V_{SS}
L8	V_{SS}	M8	V_{SS}	N8	V_{SS}	P8	V_{SS}	R8	V_{SS}
L9	V_{SS}	M9	V_{SS}	N9	V_{SS}	P9	V_{SS}	R9	V_{SS}
L10	V_{SS}	M10	V_{SS}	N10	V_{SS}	P10	V_{SS}	R10	V_{SS}
L11	V_{SS}	M11	V_{SS}	N11	V_{SS}	P11	V_{SS}	R11	V_{SS}
L12	V_{SS}	M12	V_{SS}	N12	V_{SS}	P12	V_{SS}	R12	V_{SS}
L13	V_{SS}	M13	V_{SS}	N13	V_{SS}	P13	V_{SS}	R13	V_{SS}
L14	V_{SS}	M14	V_{SS}	N14	V_{SS}	P14	V_{SS}	R14	V_{SS}
L15	V_{SS}	M15	V_{SS}	N15	V_{SS}	P15	V_{SS}	R15	V_{SS}
L16	V_{SS}	M16	V_{SS}	N16	V_{SS}	P16	V_{SS}	R16	V_{SS}
L17	V_{SS}	M17	V_{SS}	N17	V_{SS}	P17	V_{SS}	R17	V_{SS}
L18	V_{DD_IO}	M18	V_{DD_IO}	N18	V_{DD}	P18	V_{DD_IO}	R18	V_{DD}
L19	V_{DD_IO}	M19	V_{DD}	N19	V_{DD_IO}	P19	V_{DD_IO}	R19	V_{DD_IO}
L20	$\overline{BRST}$	M20	HDQM	N20	$\overline{SDWE}$	P20	ADDR31	R20	ADDR28
L21	$\overline{WRH}$	M21	$\overline{MS0}$	N21	$\overline{MSSD}$	P21	$\overline{RAS}$	R21	ADDR29
L22	$\overline{RD}$	M22	$\overline{MS1}$	N22	LDQM	P22	SDCKE	R22	$\overline{CAS}$
T1	L1DIR	U1	NC	V1	DATA34	W1	DATA40	Y1	DATA42
T2	DATA36	U2	DATA38	V2	DATA41	W2	DATA43	Y2	DATA45
T3	DATA37	U3	DATA39	V3	DATA35	W3	DATA46	Y3	L2DAT5
T4	V_{DD_IO}	U4	V_{DD_IO}	V4	V_{DD_IO}	W4	V_{DD_IO}	Y4	DATA48
T5	V_{DD}	U5	V_{DD}	V5	V_{DD}	W5	V_{DD_IO}	Y5	DATA52
T6	V_{SS}	U6	V_{SS}	V6	V_{DD}	W6	V_{DD_IO}	Y6	DATA58
T7	V_{SS}	U7	V_{SS}	V7	V_{DD_IO}	W7	V_{DD_IO}	Y7	DATA60
T8	V_{SS}	U8	V_{SS}	V8	V_{DD}	W8	V_{DD_IO}	Y8	DATA63
T9	V_{SS}	U9	V_{SS}	V9	V_{DD}	W9	V_{DD_IO}	Y9	L2DAT4
T10	V_{SS}	U10	V_{SS}	V10	V_{DD}	W10	V_{DD_IO}	Y10	L2CLKOUT
T11	V_{SS}	U11	V_{SS}	V11	V_{DD}	W11	V_{DD_IO}	Y11	NC
T12	V_{SS}	U12	V_{SS}	V12	V_{DD_IO}	W12	V_{DD_IO}	Y12	$\overline{BR4}$
T13	V_{SS}	U13	V_{SS}	V13	V_{DD}	W13	V_{DD_IO}	Y13	ACK
T14	V_{SS}	U14	V_{SS}	V14	V_{SS}	W14	V_{DD_IO}	Y14	$\overline{CPA}$
T15	V_{SS}	U15	V_{SS}	V15	V_{DD}	W15	V_{DD_IO}	Y15	ADDR0
T16	V_{SS}	U16	V_{SS}	V16	V_{DD}	W16	V_{DD_IO}	Y16	$\overline{BR7}$
T17	V_{SS}	U17	V_{SS}	V17	V_{DD}	W17	V_{DD_IO}	Y17	$\overline{HBG}$
T18	V_{DD}	U18	V_{DD}	V18	V_{DD}	W18	V_{DD_IO}	Y18	ADDR1
T19	V_{DD_IO}	U19	V_{DD_IO}	V19	V_{DD_IO}	W19	V_{DD_IO}	Y19	ADDR11
T20	ADDR23	U20	ADDR30	V20	ADDR14	W20	ADDR12	Y20	ADDR21
T21	ADDR25	U21	ADDR22	V21	ADDR19	W21	ADDR17	Y21	ADDR18
T22	ADDR27	U22	ADDR26	V22	ADDR24	W22	ADDR20	Y22	ADDR16

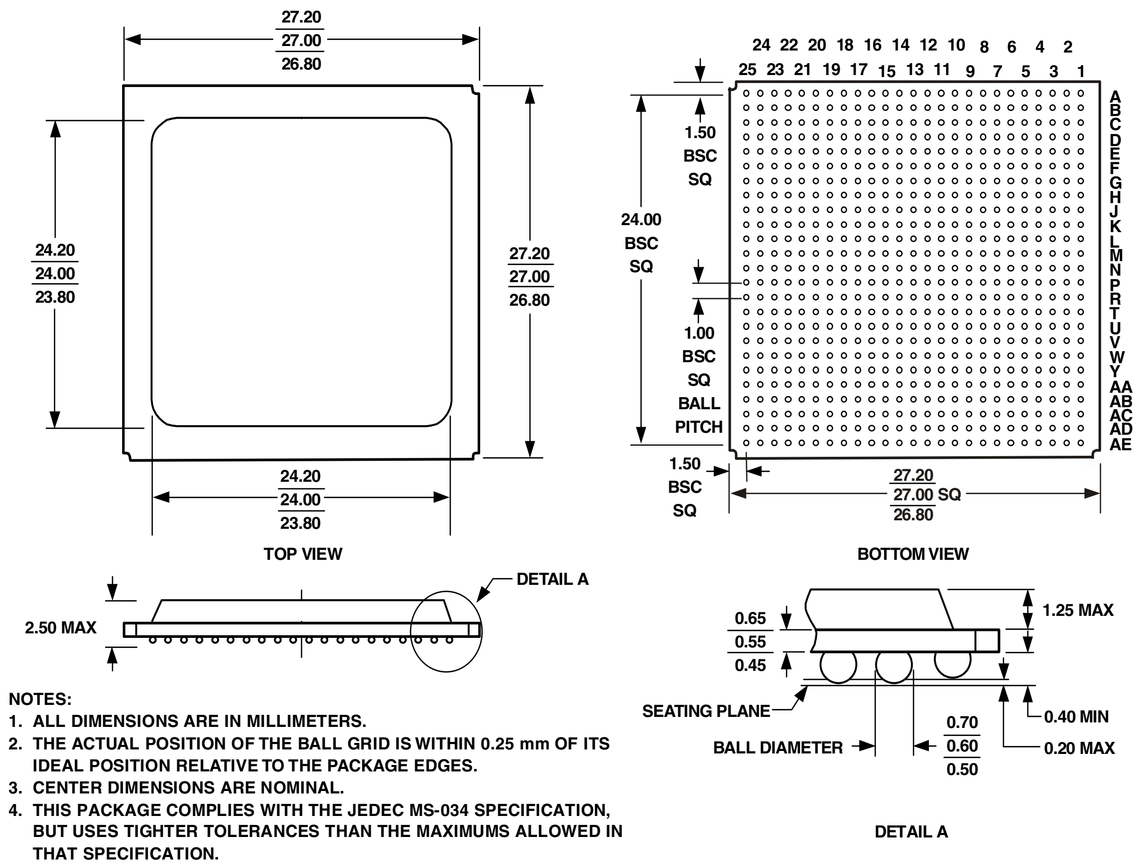

Figure 44. 625-Ball PBGA (B-625)

SURFACE-MOUNT DESIGN

The following table is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
625-ball (27 mm) PBGA	Solder Mask Defined (SMD)	0.45 mm diameter	0.60 mm diameter
484-ball (19 mm) PBGA	Solder Mask Defined (SMD)	0.40 mm diameter	0.53 mm diameter

ORDERING GUIDE

Part Number[1, 2, 3, 4]	Temperature Range (Case)	Core Clock (CCLK) Rate[5]	On-Chip SRAM	Package Description	Package Option
ADSP-TS101SAB1-000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1-100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB2-000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2-100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]

[1] S indicates 1.2 V and 3.3 V supplies.
[2] A indicates –40°C to +85°C temperature.
[3] 000 indicates 250 MHz speed grade; 100 indicates 300 MHz speed grade.
[4] Z indicates RoHS compliant part.
[5] The instruction rate runs at the internal DSP clock (CCLK) rate.
[6] The B-625 package measures 27 mm × 27 mm.
[7] The B-484 package measures 19 mm × 19 mm.