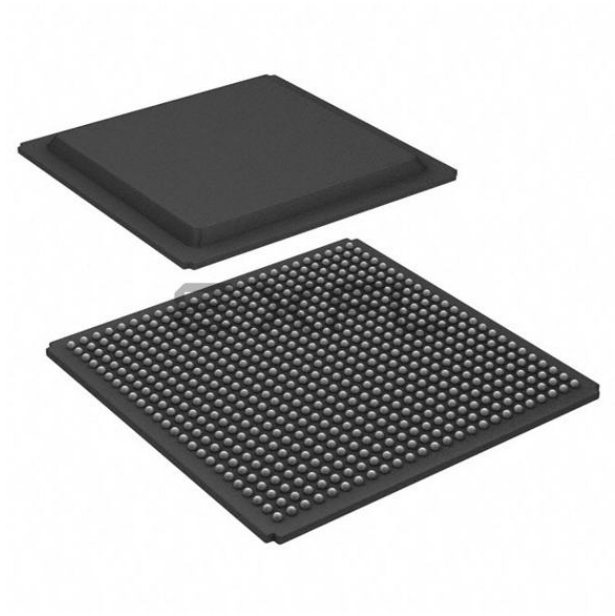

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	768kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	625-BBGA
Supplier Device Package	625-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts101sab1z100

ADSP-TS101S* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- EZ-KIT Lite Evaluation Kit for ADSP-TS201S Processor
- USB-Based Emulator and High Performance USB-Based Emulator

DOCUMENTATION

Application Notes

- AN-911: A Detailed Guide to Powering the TigerSHARC Processors
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-120: Interfacing Assembly Language Programs to C
- EE-126: The ABCs of SDRAMemories
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-143: Understanding DMA on the ADSP-TS101
- EE-147: Tuning C Source Code for the TigerSHARC® DSP Compiler
- EE-157: Explaining the Branch Target Buffer on the ADSP-TS101
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-167: Introduction to TigerSHARC® Multiprocessor Systems Using VisualDSP++™
- EE-169: Estimating Power For The ADSP-TS101S
- EE-174: ADSP-TS101S TigerSHARC® Processor Boot Loader Kernels Operation
- EE-175: Emulator and Evaluation Hardware Troubleshooting Guide for VisualDSP++ Users
- EE-176: Hardware Design Checklist For ADSP-TS101S TigerSHARC® Processors
- EE-178: The ADSP-TS101S TigerSHARC® On-chip SDRAM Controller
- EE-202: Using the Expert Linker for Multiprocessor LDFs
- EE-217: Updating the ADSP-TS101S TigerSHARC® EZ-KIT Lite™ Firmware
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-263: Parallel Implementation of Fixed-Point FFTs on TigerSHARC® Processors
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
- EE-68: Analog Devices JTAG Emulation Technical Reference

Data Sheet

- ADSP-TS101S: TigerSHARC Embedded Processor, 300 MHz, 6 Mbits, Data Sheet

Evaluation Kit Manuals

- ADSP-TS101S EZ-KIT Lite® Manual

Integrated Circuit Anomalies

- ADSP-TS101S TigerSHARC Anomaly List for Revision(s) 0.2, 0.4

Processor Manuals

- ADSP-TS101 TigerSHARC Processor Hardware Reference
- ADSP-TS101 TigerSHARC Processor Programming Reference
- TigerSHARC Processors: Manuals

Product Highlight

- General-Purpose TigerSHARC Processor Product Brief

Software Manuals

- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for TigerSHARC Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- TigerSHARC Evaluation Kits

TOOLS AND SIMULATIONS

- ADSP-TS101 TigerSHARC BSDL File 19x19mm PBGA Package for Revision 0.4, (11/2006)
- ADSP-TS101 TigerSHARC BSDL File 27x27mm PBGA Package for Revision 0.4, (11/2006)
- ADSP-TS101: 19x19mm PBGA Silicon Revision 0.0 and 0.1 [BSDL Original File], 02/08/2001
- ADSP-TS101: 19x19mm PBGA Package Silicon Revision 0.2, [BSDL Original File], 09/09/2003
- ADSP-TS101: 27x27 PBGA Package Siicon Revision 0.2, [BSDL Original File], 09/09/2003
- ADSP-TS101: 27x27 PBGA Package Silicon Revision 0.0 and 0.1 [BSDL Original File], 10/12/2001
- Designing with BGA
- TigerSHARC Processors: Software and Tools
- ADSP-TS101S IBIS Datafile BGA Package

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- A Software Solution for Chip Rate Processing in CDMA Wireless Infrastructure
- ADSP-TS101S MP System Simulation and Analysis
- Continuous Real-Time Signal Processing -- Comparing TigerSHARC and PowerPC Via Continuous cFFTs
- Rethinking Base Station, Baseband Processing for Wireless Communication
- SHARC Bites Back - The Memory Inside: TigerSHARC Swallows Its DRAM

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5/09—Rev. B to Rev. C

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Added surface-mount design info in Surface-Mount Design 44

Updated models in Ordering Guide 45

ates CCLK, which is phase-locked. The LCLKRAT pins define the clock multiplication of LCLK to CCLK (see Table 4). The link port clock is generated from CCLK via a software programmable divisor. $\overline{\text{RESET}}$ must be asserted until LCLK is stable and within specification for at least 2 ms. This applies to power-up as well as any dynamic modification of LCLK after power-up. Dynamic modification may include LCLK going out of specification as long as $\overline{\text{RESET}}$ is asserted.

Connecting SCLK and LCLK to the same clock source is a requirement for the device. Using an integer clock multiplication value provides predictable cycle-by-cycle operation, a requirement of fault-tolerant systems and some multiprocessing systems.

Noninteger values are completely functional and acceptable for applications that do not require predictable cycle-by-cycle operation.

OUTPUT PIN DRIVE STRENGTH CONTROL

Pins CONTROLIMP2–0 and DS2–0 work together to control the output drive strength of two groups of pins, the Address/Data/Control pin group and the Link pin group. CONTROLIMP2–0 independently configures the two pin groups to the maximum drive strength or to a digitally controlled drive strength that is selectable by the DS2–0 pins (see Table 13 on Page 18). If the digitally controlled drive strength is selected for a pin group, the DS2–0 pins determine one of eight strength levels for that group (see Table 14 on Page 18). The drive strength selected varies the slew rate of the driver. Drive strength 0 (DS2–0 = 000) is the weakest and slowest slew rate. Drive strength 7 (DS2–0 = 111) is the strongest and fastest slew rate.

The stronger drive strengths are useful for high frequency switching while the lower strengths may allow use of a relaxed design methodology. The strongest drive strengths have a larger di/dt and thus require more attention to signal integrity issues such a ringing, reflections and coupling. Also, a larger di/dt can increase external supply rail noise, which impacts power supply and power distribution design.

The drive strengths for the $\overline{\text{EMU}}$, $\overline{\text{CPA}}$, and $\overline{\text{DPA}}$ pins are not controllable and are fixed to the maximum level.

For drive strength calculation, see Output Drive Currents on Page 32.

POWER SUPPLIES

The ADSP-TS101S has separate power supply connections for internal logic (V_{DD}), analog circuits (V_{DD_A}), and I/O buffer (V_{DD_IO}) power supply. The internal (V_{DD}) and analog (V_{DD_A}) supplies must meet the 1.2 V requirement. The I/O buffer (V_{DD_IO}) supply must meet the 3.3 V requirement.

The analog supply (V_{DD_A}) powers the clock generator PLLs. To produce a stable clock, systems must provide a clean power supply to power input V_{DD_A}. Designs must pay critical attention to bypassing the V_{DD_A} supply.

The required power-on sequence for the DSP is to provide V_{DD} (and V_{DD_A}) before V_{DD_IO}.

FILTERING REFERENCE VOLTAGE AND CLOCKS

Figure 6 shows a possible circuit for filtering V_{REF}, SCLK_N, and LCLK_N. This circuit provides the reference voltage for the switching voltage, system clock, and local clock references.

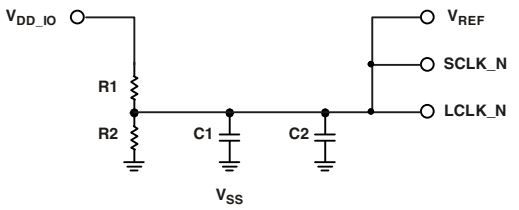

Figure 6. V_{REF}, SCLK_N, and LCLK_N Filter

DEVELOPMENT TOOLS

The ADSP-TS101S is supported with a complete set of CROSSCORE®† software and hardware development tools, including Analog Devices emulators and VisualDSP++®‡ development environment. The same emulator hardware that supports other TigerSHARC processors also fully emulates the ADSP-TS101S.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ run-time library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The DSP has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

† CROSSCORE is a registered trademark of Analog Devices, Inc.
‡ VisualDSP++ is a registered trademark of Analog Devices, Inc.

Table 5. Pin Definitions—External Port Bus Controls

Signal	Type	Term	Description
ADDR31–0[1]	I/O/T	nc	Address Bus. The DSP issues addresses for accessing memory and peripherals on these pins. In a multiprocessor system, the bus master drives addresses for accessing internal memory or I/O processor registers of other ADSP-TS101S processors. The DSP inputs addresses when a host or another DSP accesses its internal memory or I/O processor registers.
DATA63–0[1]	I/O/T	nc	External Data Bus. Data and instructions are received, and driven by the DSP, on these pins.
$\overline{RD}$[2]	I/O/T (pu[3])	nc	Memory Read. $\overline{RD}$ is asserted whenever the DSP reads from any slave in the system, excluding SDRAM. When the DSP is a slave, $\overline{RD}$ is an input and indicates read transactions that access its internal memory or universal registers. In a multiprocessor system, the bus master drives $\overline{RD}$. The $\overline{RD}$ pin changes concurrently with ADDR pins.
$\overline{WRL}$[2]	I/O/T (pu[3])	nc	Write Low. $\overline{WRL}$ is asserted in two cases: When the ADSP-TS101S writes to an even address word of external memory or to another external bus agent; and when the ADSP-TS101S writes to a 32-bit zone (host, memory, or DSP programmed to 32-bit bus). An external master (host or DSP) asserts $\overline{WRL}$ for writing to a DSP's low word of internal memory. In a multiprocessor system, the bus master drives $\overline{WRL}$. The $\overline{WRL}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRL}$ is an input and indicates write transactions that access its internal memory or universal registers.
$\overline{WRH}$[2]	I/O/T (pu[3])	nc	Write High. $\overline{WRH}$ is asserted when the ADSP-TS101S writes a long word (64 bits) or writes to an odd address word of external memory or to another external bus agent on a 64-bit data bus. An external master (host or another DSP) must assert $\overline{WRH}$ for writing to a DSP's high word of 64-bit data bus. In a multiprocessing system, the bus master drives $\overline{WRH}$. The $\overline{WRH}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRH}$ is an input and indicates write transactions that access its internal memory or universal registers.
ACK	I/O/T	epu	Acknowledge. External slave devices can deassert ACK to add wait states to external memory accesses. ACK is used by I/O devices, memory controllers, and other peripherals on the data phase. The DSP can deassert ACK to add wait states to read accesses of its internal memory. The ADSP-TS101S does not drive ACK during slave writes. Therefore, an external (approximately 10 kΩ) pull-up is required.
$\overline{BMS}$[2, 4]	O/T (pu/pd[3])	au	Boot Memory Select. $\overline{BMS}$ is the chip select for boot EPROM or flash memory. During reset, the DSP uses $\overline{BMS}$ as a strap pin (EBOOT) for EPROM boot mode. When the DSP is configured to boot from EPROM, $\overline{BMS}$ is active during the boot sequence. Pull-down enabled during $\overline{RESET}$ (asserted); pull-up enabled after $\overline{RESET}$ (deasserted). In a multiprocessor system, the DSP bus master drives $\overline{BMS}$. For details see Reset and Booting on Page 9 and the EBOOT signal description in Table 16 on Page 19.
$\overline{MS1–0}$[2]	O/T (pu[3])	nc	Memory Select. $\overline{MS0}$ or $\overline{MS1}$ is asserted whenever the DSP accesses memory banks 0 or 1, respectively. $\overline{MS1–0}$ are decoded memory address pins that change concurrently with ADDR pins. When ADDR31:26 = 0b000010, $\overline{MS0}$ is asserted. When ADDR31:26 = 0b000011, $\overline{MS1}$ is asserted. In multiprocessor systems, the master DSP drives $\overline{MS1–0}$.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

Table 6. Pin Definitions—External Port Arbitration (Continued)

Signal	Type	Term	Description
$\overline{HBG}$[3]	I/O/T (pu[2])	nc	Host Bus Grant. Acknowledges $\overline{HBR}$ and indicates that the host can take control of the external bus. When relinquishing the bus, the master DSP three-states the ADDR31–0, DATA63–0, $\overline{MSH}$, $\overline{MSSD}$, $\overline{MS1–0}$, $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{BMS}$, $\overline{BRST}$, $\overline{FLYBY}$, $\overline{IOEN}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, SDCKE, LDQM and HDQM pins, and the DSP puts the SDRAM in self-refresh mode. The DSP asserts $\overline{HBG}$ until the host deasserts $\overline{HBR}$. In multiprocessor systems, the current bus master DSP drives $\overline{HBG}$, and all slave DSPs monitor $\overline{HBG}$.
$\overline{CPA}$	I/O (o/d)	See next column	Core Priority Access. Asserted while the DSP's core accesses external memory. This pin enables a slave DSP to interrupt a master DSP's background DMA transfers and gain control of the external bus for core-initiated transactions. $\overline{CPA}$ is an open drain output, connected to all DSPs in the system. The $\overline{CPA}$ pin has an internal 500 Ω pull-up resistor, which is only enabled on the DSP with ID2–0 = 0. If ID0 is not used, terminate this pin as either epu or nc. If ID7–1 is not used, terminate this pin as epu.
$\overline{DPA}$	I/O (o/d)	See next column	DMA Priority Access. Asserted while a high-priority DSP DMA channel accesses external memory. This pin enables a high-priority DMA channel on a slave DSP to interrupt transfers of a normal-priority DMA channel on a master DSP and gain control of the external bus for DMA-initiated transactions. $\overline{DPA}$ is an open drain output, connected to all DSPs in the system. The $\overline{DPA}$ pin has an internal 500 Ω pull-up resistor, which is only enabled on the DSP with ID2–0 = 0. If ID0 is not used, terminate this pin as either epu or nc. If ID7–1 is not used, terminate this pin as epu.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 7. Pin Definitions—External Port DMA/Flyby

Signal	Type	Term	Description
$\overline{DMAR3–0}$	I/A	epu	DMA Request Pins. Enable external I/O devices to request DMA services from the DSP. In response to $\overline{DMARx}$, the DSP performs DMA transfers according to the DMA channel's initialization. The DSP ignores DMA requests from uninitialized channels.
$\overline{FLYBY}$[1]	O/T (pu[2])	nc	Flyby Mode. When a DSP DMA channel is initiated in $\overline{FLYBY}$ mode, it generates flyby transactions on the external bus. During flyby transactions, the DSP asserts $\overline{FLYBY}$, which signals the source or destination I/O device to latch the next data or strobe the current data, respectively, and to prepare for the next data on the next cycle.
$\overline{IOEN}$[1]	O/T (pu[2])	nc	I/O Device Output Enable. Enables the output buffers of an external I/O device for flyby transactions between the device and external memory. Active on flyby transactions.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 11. Pin Definitions—Link Ports (Continued)

Signal	Type	Term	Description
L1DIR	O	nc	Link1 Direction. (0 = input, 1 = output)
L2DIR[2]	O (pd[3])	au	Link2 Direction. (0 = input, 1 = output) At reset this is a strap pin. For more information, see Table 16 on Page 19.
L3DIR	O (pd[3])	nc	Link3 Direction. (0 = input, 1 = output)
Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state			
Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.			

[1] The link port data pins, if connected or floated for extended periods (for example, token slave with no token master), do not require pull-ups or pull-downs as there are no reliability issues and the worst-case power consumption for these floating inputs is negligible. Floating in this case means that these inputs are not driven by any source and that dc-biased terminations are not present.
[2] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[3] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 12. Pin Definitions—Impedance and Drive Strength Control

Signal	Type	Term	Description
CONTROLIMP2–1[1] CONTROLIMP0[2]	I (pu[3]) I (pd[3])	au au	Impedance Control. For ADC (Address/Data/Controls) and LINK (all link port outputs) signals, the CONTROLIMP2–0 pins control impedance as shown in Table 13. These pins enable or disable dig_ctrl mode. When dig_ctrl: 0 = Disabled (maximum drive strength) 1 = Enabled (use DS2–0 drive strength selection)
DS2–0[1]	I (pu[3])	au	Digital Drive Strength Selection. Selected as shown in Table 14. For drive strength calculation, see Output Drive Currents on Page 32. The drive strength for some pins is preset, not controlled by the DS2–0 pins. The pins that are always at drive strength 7 (100%) are: $\overline{CPA}$, $\overline{DPA}$, and $\overline{EMU}$.
Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state			
Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.			

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[3] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 13. Control Impedance Selection

CONTROLIMP2–0	ADC dig_ctrl	LINK dig_ctrl
000	0	0
001	0	0
010	0	1
011	reserved	reserved
100	1	0
101	reserved	reserved
110 (default)	1	1
111	reserved	reserved

Table 14. Drive Strength Selection

DS2–0	Drive Strength
000	Strength 0
001	Strength 1
010	Strength 2
011	Strength 3
100	Strength 4
101	Strength 5
110	Strength 6
111 (default)	Strength 7

For power-up sequencing, power-up reset, and normal reset (hot reset) timing requirements, refer to Table 26 and Figure 13, Table 27 and Figure 14, and Table 28, and Figure 15 respectively.

Table 19. AC Asynchronous Signal Specifications (All values in this table are in nanoseconds)

Name	Description	Pulse Width Low (min)	Pulse Width High (min)
$\overline{IRQ3–0}$[1]	Interrupt request input	t_{CCLK} + 3 ns	
$\overline{DMAR3–0}$[1]	DMA request input	t_{CCLK} + 4 ns	t_{CCLK} + 4 ns
TMR0E[2]	Timer 0 expired output		4 × t_{SCLK} ns
FLAG3–0[1, 3]	Flag pins input	3 × t_{CCLK} ns	3 × t_{CCLK} ns
$\overline{TRST}$	JTAG test reset input	1 ns	

[1] These input pins do not need to be synchronized to a clock reference.
[2] This pin is a strap option. During reset, an internal resistor pulls the pin low.
[3] For output specifications, see Table 29 and Table 30.

Table 20. Reference Clocks—Core Clock (CCLK) Cycle Time

Parameter	Description	Grade = 100 (300 MHz) Min	Grade = 100 (300 MHz) Max	Grade = 000 (250 MHz) Min	Grade = 000 (250 MHz) Max	Unit
t_{CCLK}[1]	Core Clock Cycle Time	3.3	12.5	4.0	12.5	ns

[1] CCLK is the internal processor clock or instruction cycle time. The period of this clock is equal to the system clock period (t_{SCLK}) divided by the system clock ratio (SCLKRAT2–0). For information on available part numbers for different internal processor clock rates, see the Ordering Guide on Page 45.

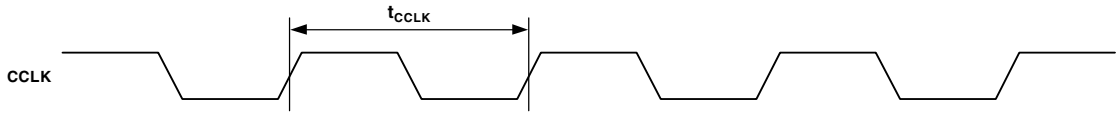

Figure 9. Reference Clocks—Core Clock (CCLK) Cycle Time

Table 21. Reference Clocks—Local Clock (LCLK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{LCLK}[1, 2, 3, 4]	Local Clock Cycle Time	10	25	ns
t_{LCLKH}	Local Clock Cycle High Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKL}	Local Clock Cycle Low Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKJ}[5, 6]	Local Clock Jitter Tolerance		500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] LCLK_P and SCLK_P must be connected to the same source.
[4] The value of (t_{LCLK} / LCLKRAT2-0) must not violate the specification for t_{CCLK}.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

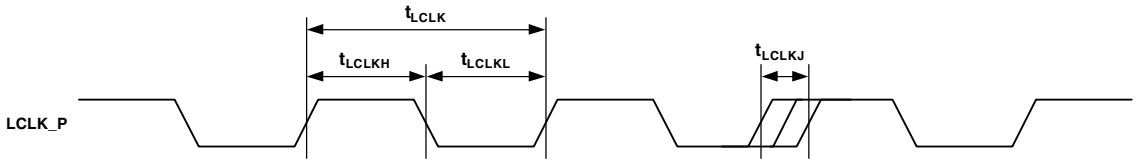

Figure 10. Reference Clocks—Local Clock (LCLK) Cycle Time

Table 25. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{START_LO}	$\overline{RESET}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, SCLK/LCLK, and Static/Strap Pins Are Stable and Within Specification	2		ms
t_{PULSE1_HI}	$\overline{RESET}$ Deasserted for First Pulse	$50 \times t_{SCLK}$	$100 \times t_{SCLK}$	ns
t_{PULSE2_LO}	$\overline{RESET}$ Asserted for Second Pulse	$100 \times t_{SCLK}$		ns
t_{TRST_PWR}[1]	$\overline{TRST}$ Asserted During Power-Up Reset	$2 \times t_{SCLK}$		ns

[1] Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, and SCLK/LCLK and static/strap pins are stable and within specification, and before $\overline{RESET}$ is deasserted.

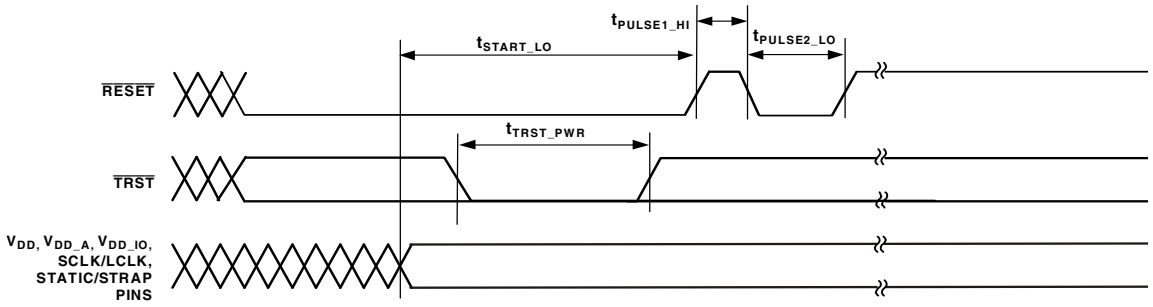

Figure 14. Power-Up Reset Timing

Table 26. Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RST_IN}	$\overline{RESET}$ Asserted	$100 \times t_{SCLK}$		ns
t_{STRAP}	$\overline{RESET}$ Deasserted After Strap Pins Stable	2		ms

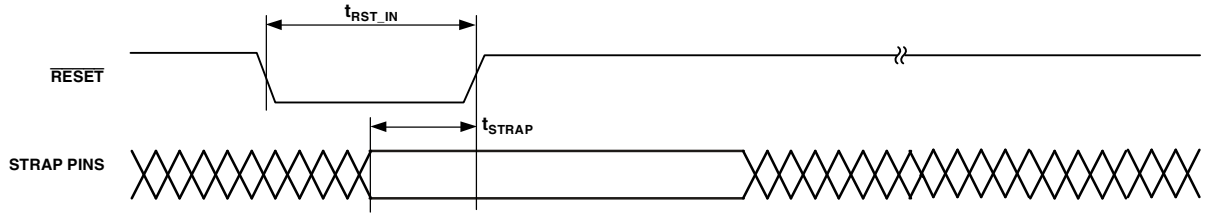

Figure 15. Normal Reset (Hot Reset) Timing

Table 27. AC Signal Specifications (for SCLK <16.7 ns) (All values in this table are in nanoseconds)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
ADDR31–0	External Address Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
DATA63–0	External Data Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSH}}$	Memory Select Host Line			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSSD}}$	Memory Select SDRAM Line	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RD}}$	Memory Read	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRL}}$	Write Low Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRH}}$	Write High Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
ACK	Acknowledge for Data	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
SDCKE	SDRAM Clock Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RAS}}$	Row Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CAS}}$	Column Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
LDQM	Low Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
HDQM	High Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
SDA10	SDRAM ADDR10			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{HBR}}$	Host Bus Request	2.6	0.5					SCLK
$\overline{\text{HBG}}$	Host Bus Grant	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BOFF}}$	Back Off Request	2.6	0.5					SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BRST}}$	Burst Access	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request	2.6	0.5	4.2	1.0			SCLK
$\overline{\text{FLYBY}}$	Flyby Mode Selection			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{IOEN}}$	Flyby I/O Enable			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CPA}}$ [3, 4]	Core Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{DPA}}$ [3, 4]	DMA Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{BMS}}$[5]	Boot Memory Select			4.2	1.0	0.9	2.5	SCLK
FLAG3–0[6]	FLAG Pins			4.2	1.0	1.0	4.0	SCLK
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	1.0			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

Table 28. AC Signal Specifications (for 16.7 ns <SCLK <25 ns) (All values in this table are in nanoseconds) (Continued)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	0.8			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

[1] The output valid (max) value in this column applies for the standard 30 pF capacitive load used in testing. To see how output valid varies with capacitive loading, see Figure 40 on Page 36.

[2] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.

[3] $\overline{\text{CPA}}$ and $\overline{\text{DPA}}$ pins are open drains and have 0.5 kΩ internal pull-ups.

[4] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference. These synchronous specifications only apply for recognition in the current clock reference cycle.

[5] This pin is a strap option. During reset, an internal resistor pulls the pin low.

[6] For input specifications, see Table 21.

[7] For additional requirement details, see Reset and Booting on Page 9.

[8] TCK_FE indicates TCK falling edge.

[9] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.

[10] Reference clock depends on function.

[11] System inputs are: $\overline{\text{IRQ3–0}}$, $\overline{\text{BMS}}$, LCLKRAT2–0, SCLKFREQ, $\overline{\text{BM}}$, TMR0E, FLAG3–0, ID2–0, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, $\overline{\text{BOFF}}$, $\overline{\text{HBR}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKIN, L0DAT7–0, L1CLKIN, L1DAT7–0, L2CLKIN, L2DAT7–0, L2DIR, L3CLKIN, L3DAT7–0, DS2–0, CONTROLIMP2–0, $\overline{\text{RESET}}$, $\overline{\text{DMAR3–0}}$.

[12] System outputs are: $\overline{\text{BMS}}$, $\overline{\text{BM}}$, $\overline{\text{BUSLOCK}}$, TMR0E, FLAG3–0, $\overline{\text{FLYBY}}$, $\overline{\text{IOEN}}$, $\overline{\text{MSH}}$, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MS1–0}}$, HDQM, LDQM, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKOUT, L0DAT7–0, L0DIR, L1CLKOUT, L1DAT7–0, L1DIR, L2CLKOUT, L2DAT7–0, L2DIR, L3CLKOUT, L3DAT7–0, L3DIR, $\overline{\text{EMU}}$.

Table 31. Link Ports—Token Switch, Token Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{REQI}	Token Request Input Width	$5.0 \times t_{LxCLK\_Rx}$		ns
t_{TKRQ}	Token Request from Token Enable[1]		$3.0 \times t_{LxCLK\_Tx}$	ns
Switching Characteristics				
t_{TKENO}	Token Switch Enable Output	$8.0 \times t_{LxCLK\_Tx}$		ns
t_{REQO}	Token Request Output Width[2]	$6.0 \times t_{LxCLK\_Tx}$		ns

[1] For guaranteeing token switch during token enable.
[2] LxCLKOUT shows both possible responses to the token request: [1] a "Token Grant" (LxCLKOUT remains high), and [2] a "Token Regret" (LxCLKOUT goes low).

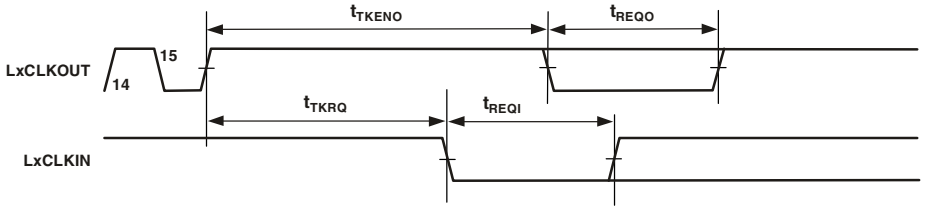

Figure 19. Link Ports—Token Switch, Token Master

Table 32. Link Ports—Token Switch, Token Requester

Parameter		Min	Max	Unit
Timing Requirements				
t_{TKENI}[1]	Token Switch Enable Input	$8.0 \times t_{LxCLK\_Rx}$		ns
Switching Characteristics				
t_{REQO}	Token Request Output Width[2]	$6.0 \times t_{LxCLK\_Rx}$		ns

[1] Required whenever there is a break in transmission.
[2] LxCLKOUT shows both possible responses to the token request: [1] a "Token Grant" (LxCLKOUT remains high), and [2] a "Token Regret" (LxCLKOUT goes low).

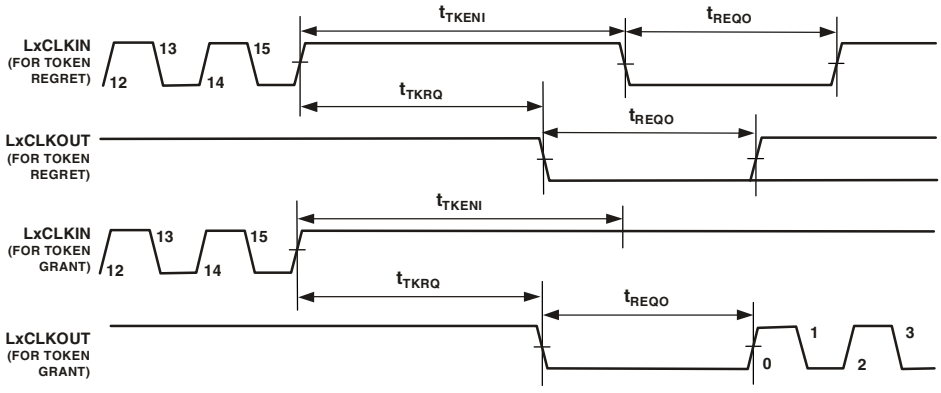

Figure 20. Link Ports—Token Switch, Token Requester

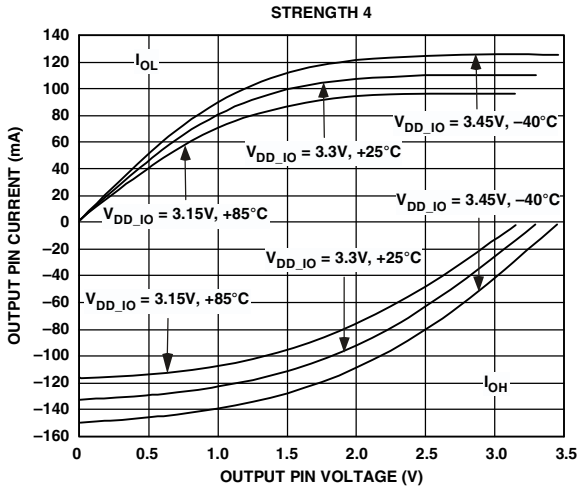

Figure 25. Typical Drive Currents at Strength 4

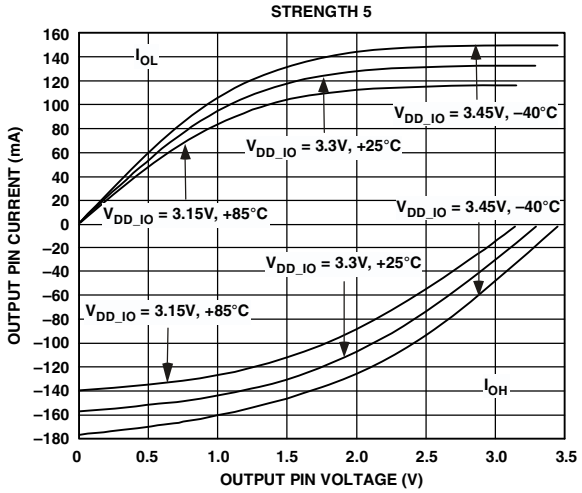

Figure 26. Typical Drive Currents at Strength 5

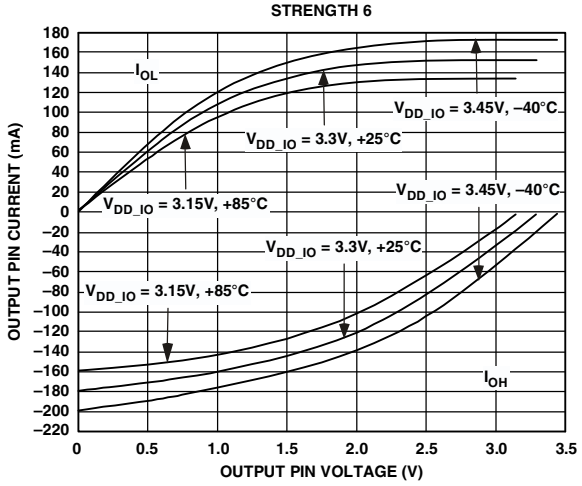

Figure 27. Typical Drive Currents at Strength 6

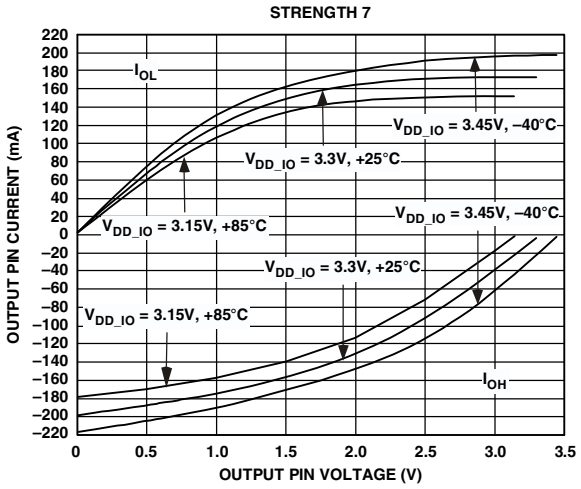

Figure 28. Typical Drive Currents at Strength 7

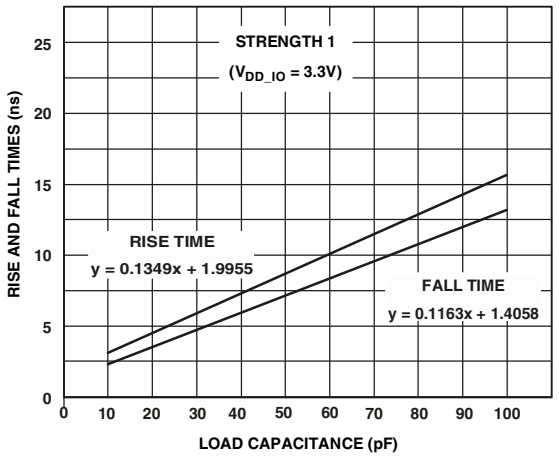

Figure 33. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 1

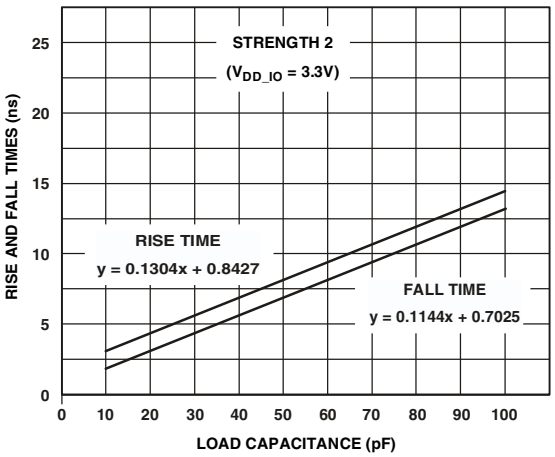

Figure 34. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 2

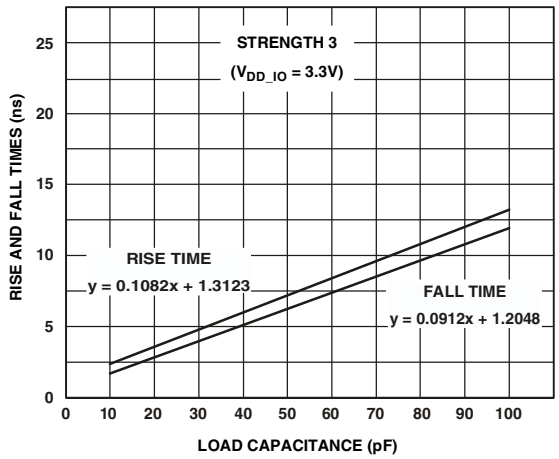

Figure 35. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 3

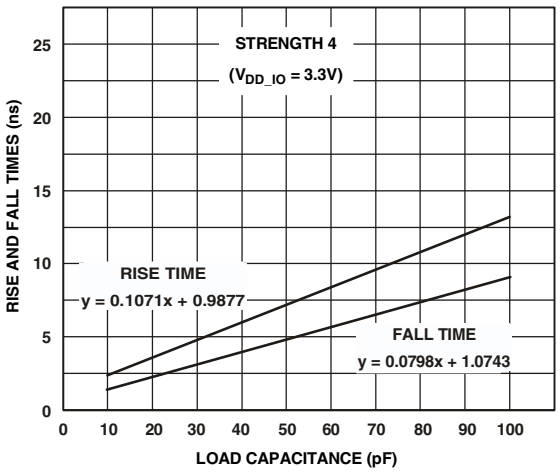

Figure 36. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 4

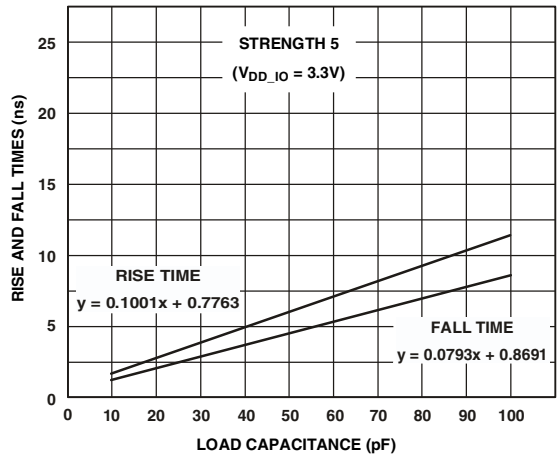

Figure 37. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 5

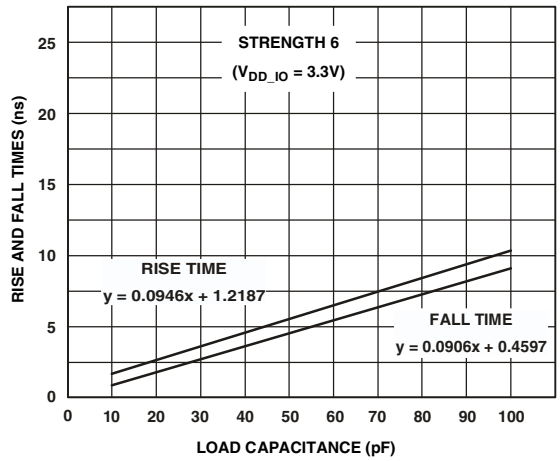

Figure 38. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 6

Table 35. 484-Ball (19 mm × 19 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
AA1	DATA44	AA10	L2DAT3	AA19	SDA10	AB6	DATA62	AB15	$\overline{BR5}$
AA2	DATA50	AA11	L2DAT7	AA20	ADDR10	AB7	L2DAT1	AB16	$\overline{BOFF}$
AA3	DATA47	AA12	$\overline{BR2}$	AA21	ADDR13	AB8	L2DAT2	AB17	ADDR3
AA4	DATA49	AA13	$\overline{BR6}$	AA22	ADDR15	AB9	L2DAT6	AB18	ADDR4
AA5	DATA51	AA14	$\overline{HBR}$	AB1	V_{SS}	AB10	L2CLKIN	AB19	ADDR6
AA6	DATA54	AA15	$\overline{DPA}$	AB2	DATA53	AB11	L2DIR	AB20	ADDR7
AA7	DATA57	AA16	ADDR2	AB3	DATA55	AB12	$\overline{BR0}$	AB21	ADDR9
AA8	DATA61	AA17	ADDR5	AB4	DATA56	AB13	$\overline{BR1}$	AB22	V_{SS}
AA9	L2DAT0	AA18	ADDR8	AB5	DATA59	AB14	$\overline{BR3}$		

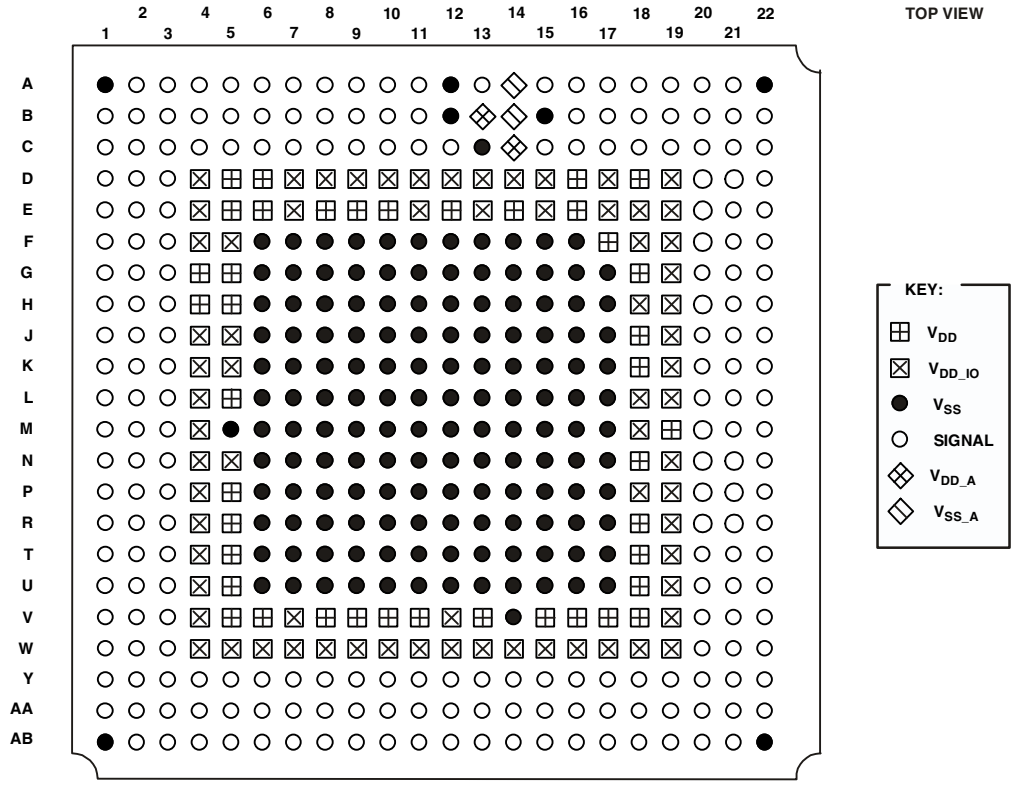

Figure 41. 484-Ball PBGA Pin Configurations (Top View, Summary)

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
A1	V_{SS}	B1	V_{SS}	C1	V_{SS}	D1	V_{SS}	E1	DATA23
A2	DATA17	B2	V_{SS}	C2	DATA20	D2	V_{SS}	E2	DATA22
A3	DATA14	B3	DATA16	C3	DATA21	D3	DATA19	E3	V_{SS}
A4	DATA11	B4	DATA13	C4	DATA18	D4	V_{DD_IO}	E4	V_{DD_IO}
A5	DATA9	B5	DATA12	C5	DATA15	D5	V_{DD_IO}	E5	V_{DD_IO}
A6	DATA7	B6	DATA10	C6	DATA8	D6	V_{DD_IO}	E6	V_{DD}
A7	DATA4	B7	DATA5	C7	DATA6	D7	V_{DD_IO}	E7	V_{DD}
A8	DATA1	B8	DATA2	C8	DATA3	D8	V_{DD_IO}	E8	V_{DD_IO}
A9	L0DIR	B9	NC	C9	DATA0	D9	V_{DD_IO}	E9	V_{DD_IO}
A10	L0DAT7	B10	L0CLKOUT	C10	L0CLKIN	D10	V_{DD_IO}	E10	V_{DD}
A11	L0DAT4	B11	L0DAT5	C11	L0DAT6	D11	V_{DD_IO}	E11	V_{DD}
A12	L0DAT1	B12	L0DAT2	C12	L0DAT3	D12	V_{DD_IO}	E12	V_{DD_IO}
A13	LCLK_N	B13	V_{SS}	C13	L0DAT0	D13	V_{DD_IO}	E13	V_{DD_IO}
A14	LCLK_P	B14	V_{SS}	C14	V_{SS_A}	D14	V_{DD_IO}	E14	V_{DD}
A15	V_{DD_A}	B15	V_{SS_A}	C15	V_{DD_A}	D15	V_{DD_IO}	E15	V_{DD}
A16	SCLK_N	B16	SCLK_P	C16	V_{SS}	D16	V_{DD_IO}	E16	V_{DD_IO}
A17	V_{REF}	B17	V_{SS}	C17	DS0	D17	V_{DD_IO}	E17	V_{DD_IO}
A18	DS1	B18	DS2	C18	CONTROLIMP0	D18	V_{DD_IO}	E18	V_{DD}
A19	CONTROLIMP2	B19	CONTROLIMP1	C19	$\overline{\text{DMAR1}}$	D19	V_{DD_IO}	E19	V_{DD}
A20	$\overline{\text{RESET}}$	B20	$\overline{\text{DMAR3}}$	C20	TDI	D20	V_{DD_IO}	E20	V_{DD_IO}
A21	$\overline{\text{DMAR2}}$	B21	$\overline{\text{DMAR0}}$	C21	$\overline{\text{IRQ2}}$	D21	V_{DD_IO}	E21	V_{DD_IO}
A22	$\overline{\text{EMU}}$	B22	$\overline{\text{IRQ3}}$	C22	LCLKRAT0	D22	V_{DD_IO}	E22	V_{DD_IO}
A23	$\overline{\text{TRST}}$	B23	TCK	C23	LCLKRAT1	D23	$\overline{\text{BMS}}$	E23	V_{SS}
A24	TMS	B24	$\overline{\text{IRQ1}}$	C24	$\overline{\text{IRQ0}}$	D24	V_{SS}	E24	SCLKFREQ
A25	V_{SS}	B25	TDO	C25	V_{SS}	D25	V_{SS}	E25	LCLKRAT2
F1	DATA26	G1	DATA29	H1	L3DAT0	J1	L3DAT3	K1	L3DAT6
F2	DATA25	G2	DATA28	H2	DATA31	J2	L3DAT2	K2	L3DAT5
F3	DATA24	G3	DATA27	H3	DATA30	J3	L3DAT1	K3	L3DAT4
F4	V_{DD_IO}	G4	V_{DD_IO}	H4	V_{DD_IO}	J4	V_{DD_IO}	K4	V_{DD_IO}
F5	V_{DD_IO}	G5	V_{DD}	H5	V_{DD}	J5	V_{DD_IO}	K5	V_{DD_IO}
F6	V_{DD}	G6	V_{DD}	H6	V_{DD}	J6	V_{DD}	K6	V_{DD}
F7	V_{DD}	G7	V_{SS}	H7	V_{SS}	J7	V_{SS}	K7	V_{SS}
F8	V_{DD}	G8	V_{SS}	H8	V_{SS}	J8	V_{SS}	K8	V_{SS}
F9	V_{DD}	G9	V_{SS}	H9	V_{SS}	J9	V_{SS}	K9	V_{SS}
F10	V_{DD}	G10	V_{SS}	H10	V_{SS}	J10	V_{SS}	K10	V_{SS}
F11	V_{DD}	G11	V_{SS}	H11	V_{SS}	J11	V_{SS}	K11	V_{SS}
F12	V_{DD}	G12	V_{SS}	H12	V_{SS}	J12	V_{SS}	K12	V_{SS}
F13	V_{DD}	G13	V_{SS}	H13	V_{SS}	J13	V_{SS}	K13	V_{SS}
F14	V_{DD}	G14	V_{SS}	H14	V_{SS}	J14	V_{SS}	K14	V_{SS}
F15	V_{DD}	G15	V_{SS}	H15	V_{SS}	J15	V_{SS}	K15	V_{SS}
F16	V_{DD}	G16	V_{SS}	H16	V_{SS}	J16	V_{SS}	K16	V_{SS}
F17	V_{DD}	G17	V_{SS}	H17	V_{SS}	J17	V_{SS}	K17	V_{SS}
F18	V_{DD}	G18	V_{SS}	H18	V_{SS}	J18	V_{SS}	K18	V_{SS}
F19	V_{DD}	G19	V_{SS}	H19	V_{SS}	J19	V_{SS}	K19	V_{SS}
F20	V_{DD}	G20	V_{DD}	H20	V_{DD}	J20	V_{DD}	K20	V_{DD}
F21	V_{DD}	G21	V_{DD}	H21	V_{DD_IO}	J21	V_{DD_IO}	K21	V_{DD}
F22	V_{DD_IO}	G22	V_{DD_IO}	H22	V_{DD_IO}	J22	V_{DD_IO}	K22	V_{DD_IO}
F23	$\overline{\text{BM}}$	G23	FLAG3	H23	FLAG0	J23	ID0	K23	NC
F24	$\overline{\text{BUSLOCK}}$	G24	FLAG2	H24	ID2	J24	NC	K24	NC
F25	TMR0E	G25	FLAG1	H25	ID1	J25	NC	K25	NC

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
L1	L3CLKIN	M1	L1DAT0	N1	L1DAT2	P1	L1DAT5	R1	L1CLKOUT
L2	L3CLKOUT	M2	NC	N2	NC	P2	L1DAT4	R2	L1DAT7
L3	L3DAT7	M3	L3DIR	N3	L1DAT1	P3	L1DAT3	R3	L1DAT6
L4	V_{DD_IO}	M4	V_{DD_IO}	N4	V_{DD_IO}	P4	V_{DD_IO}	R4	V_{DD_IO}
L5	V_{DD}	M5	V_{DD}	N5	V_{DD_IO}	P5	V_{DD_IO}	R5	V_{DD}
L6	V_{DD}	M6	V_{DD}	N6	V_{DD}	P6	V_{DD}	R6	V_{DD}
L7	V_{SS}	M7	V_{SS}	N7	V_{SS}	P7	V_{SS}	R7	V_{SS}
L8	V_{SS}	M8	V_{SS}	N8	V_{SS}	P8	V_{SS}	R8	V_{SS}
L9	V_{SS}	M9	V_{SS}	N9	V_{SS}	P9	V_{SS}	R9	V_{SS}
L10	V_{SS}	M10	V_{SS}	N10	V_{SS}	P10	V_{SS}	R10	V_{SS}
L11	V_{SS}	M11	V_{SS}	N11	V_{SS}	P11	V_{SS}	R11	V_{SS}
L12	V_{SS}	M12	V_{SS}	N12	V_{SS}	P12	V_{SS}	R12	V_{SS}
L13	V_{SS}	M13	V_{SS}	N13	V_{SS}	P13	V_{SS}	R13	V_{SS}
L14	V_{SS}	M14	V_{SS}	N14	V_{SS}	P14	V_{SS}	R14	V_{SS}
L15	V_{SS}	M15	V_{SS}	N15	V_{SS}	P15	V_{SS}	R15	V_{SS}
L16	V_{SS}	M16	V_{SS}	N16	V_{SS}	P16	V_{SS}	R16	V_{SS}
L17	V_{SS}	M17	V_{SS}	N17	V_{SS}	P17	V_{SS}	R17	V_{SS}
L18	V_{SS}	M18	V_{SS}	N18	V_{SS}	P18	V_{SS}	R18	V_{SS}
L19	V_{SS}	M19	V_{SS}	N19	V_{SS}	P19	V_{SS}	R19	V_{SS}
L20	V_{DD}	M20	V_{DD}	N20	V_{DD}	P20	V_{DD}	R20	V_{DD}
L21	V_{DD}	M21	V_{DD_IO}	N21	V_{DD_IO}	P21	V_{DD}	R21	V_{DD}
L22	V_{DD_IO}	M22	V_{DD_IO}	N22	V_{DD_IO}	P22	V_{DD_IO}	R22	V_{DD_IO}
L23	NC	M23	$\overline{\text{IOEN}}$	N23	$\overline{\text{WRH}}$	P23	$\overline{\text{MS1}}$	R23	LDQM
L24	NC	M24	$\overline{\text{MSH}}$	N24	$\overline{\text{WRL}}$	P24	$\overline{\text{MS0}}$	R24	NC
L25	$\overline{\text{FLYBY}}$	M25	$\overline{\text{BRST}}$	N25	$\overline{\text{RD}}$	P25	HDQM	R25	$\overline{\text{MSSD}}$
T1	NC	U1	DATA34	V1	DATA37	W1	DATA40	Y1	DATA43
T2	L1DIR	U2	DATA33	V2	DATA36	W2	DATA39	Y2	DATA42
T3	L1CLKIN	U3	DATA32	V3	DATA35	W3	DATA38	Y3	DATA41
T4	V_{DD_IO}	U4	V_{DD_IO}	V4	V_{DD_IO}	W4	V_{DD_IO}	Y4	V_{DD_IO}
T5	V_{DD}	U5	V_{DD_IO}	V5	V_{DD_IO}	W5	V_{DD}	Y5	V_{DD}
T6	V_{DD}	U6	V_{DD}	V6	V_{DD}	W6	V_{DD}	Y6	V_{DD}
T7	V_{SS}	U7	V_{SS}	V7	V_{SS}	W7	V_{SS}	Y7	V_{DD}
T8	V_{SS}	U8	V_{SS}	V8	V_{SS}	W8	V_{SS}	Y8	V_{DD}
T9	V_{SS}	U9	V_{SS}	V9	V_{SS}	W9	V_{SS}	Y9	V_{DD}
T10	V_{SS}	U10	V_{SS}	V10	V_{SS}	W10	V_{SS}	Y10	V_{DD}
T11	V_{SS}	U11	V_{SS}	V11	V_{SS}	W11	V_{SS}	Y11	V_{DD}
T12	V_{SS}	U12	V_{SS}	V12	V_{SS}	W12	V_{SS}	Y12	V_{DD}
T13	V_{SS}	U13	V_{SS}	V13	V_{SS}	W13	V_{SS}	Y13	V_{DD}
T14	V_{SS}	U14	V_{SS}	V14	V_{SS}	W14	V_{SS}	Y14	V_{DD}
T15	V_{SS}	U15	V_{SS}	V15	V_{SS}	W15	V_{SS}	Y15	V_{DD}
T16	V_{SS}	U16	V_{SS}	V16	V_{SS}	W16	V_{SS}	Y16	V_{DD}
T17	V_{SS}	U17	V_{SS}	V17	V_{SS}	W17	V_{SS}	Y17	V_{DD}
T18	V_{SS}	U18	V_{SS}	V18	V_{SS}	W18	V_{SS}	Y18	V_{DD}
T19	V_{SS}	U19	V_{SS}	V19	V_{SS}	W19	V_{SS}	Y19	V_{DD}
T20	V_{DD}	U20	V_{DD}	V20	V_{DD}	W20	V_{DD}	Y20	V_{DD}
T21	V_{DD_IO}	U21	V_{DD_IO}	V21	V_{DD}	W21	V_{DD}	Y21	V_{DD_IO}
T22	V_{DD_IO}	U22	V_{DD_IO}	V22	V_{DD_IO}	W22	V_{DD_IO}	Y22	V_{DD_IO}
T23	SDCKE	U23	$\overline{\text{CAS}}$	V23	ADDR31	W23	ADDR28	Y23	ADDR26
T24	NC	U24	NC	V24	ADDR30	W24	NC	Y24	ADDR25
T25	$\overline{\text{SDWE}}$	U25	$\overline{\text{RAS}}$	V25	ADDR29	W25	ADDR27	Y25	ADDR24

ORDERING GUIDE

Part Number[1, 2, 3, 4]	Temperature Range (Case)	Core Clock (CCLK) Rate[5]	On-Chip SRAM	Package Description	Package Option
ADSP-TS101SAB1-000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1-100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB2-000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2-100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]

[1] S indicates 1.2 V and 3.3 V supplies.
[2] A indicates –40°C to +85°C temperature.
[3] 000 indicates 250 MHz speed grade; 100 indicates 300 MHz speed grade.
[4] Z indicates RoHS compliant part.
[5] The instruction rate runs at the internal DSP clock (CCLK) rate.
[6] The B-625 package measures 27 mm × 27 mm.
[7] The B-484 package measures 19 mm × 19 mm.