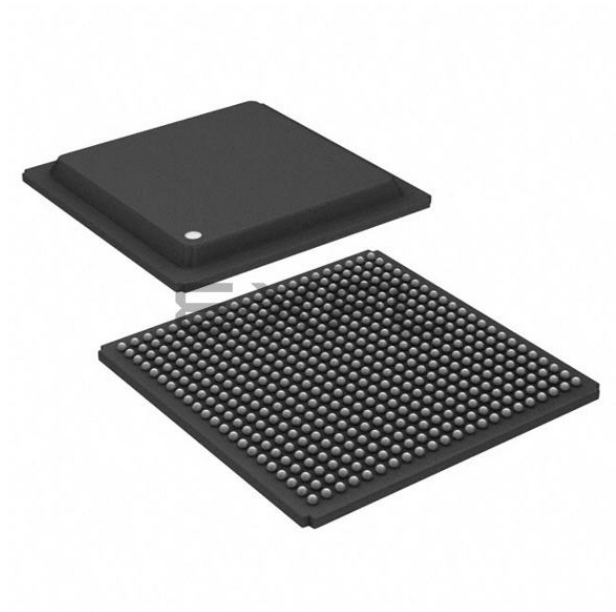

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	250MHz
Non-Volatile Memory	External
On-Chip RAM	768kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	484-BFBGA
Supplier Device Package	484-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts101sab2-000

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ integrated development and debugging environment (IDDE) lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the TigerSHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command-line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command-line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the DSP or external memory with a drag of the mouse, examine run-time stack and heap usage. The Expert Linker is fully compatible with existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices DSP emulators use the IEEE 1149.1 JTAG Test Access Port of the ADSP-TS101S processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the TigerSHARC processor family. Hardware tools include TigerSHARC processor PC plug-in cards. Third-party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

DESIGNING AN EMULATOR-COMPATIBLE DSP BOARD (TARGET)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG DSP. The emulator uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-TS101S processor's architecture and functionality. For detailed information on the ADSP-TS101S processor's core architecture and instruction set, see the *ADSP-TS101 TigerSHARC Processor Programming Reference* and the *ADSP-TS101 TigerSHARC Processor Hardware Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

PIN FUNCTION DESCRIPTIONS

While most of the ADSP-TS101S processor's input pins are normally synchronous—tied to a specific clock—a few are asynchronous. For these asynchronous signals, an on-chip synchronization circuit prevents metastability problems. The synchronous ac specification for asynchronous signals is used only when predictable cycle-by-cycle behavior is required.

All inputs are sampled by a clock reference, therefore input specifications (asynchronous minimum pulse widths or synchronous input setup and hold) must be met to guarantee recognition.

PIN STATES AT RESET

The output pins can be three-stated during normal operation. The DSP three-states all outputs during reset, allowing these pins to get to their internal pull-up or pull-down state. Some output pins (control signals) have a pull-up or pull-down that maintains a known value during transitions between different drivers.

PIN DEFINITIONS

The Type column in the following pin definitions tables describes the pin type, when the pin is used in the system. The Term (for termination) column describes the pin termination type if the pin is not used by the system. Note that some pins are always used (indicated with au symbol).

Table 3. Pin Definitions—Clocks and Reset

Signal	Type	Term	Description
LCLK_N	I	au	Local Clock Reference. Connect this pin to V_{REF} as shown in Figure 6.
LCLK_P	I	au	Local Clock Input. DSP clock input. The instruction cycle rate = n × LCLK, where n is user-programmable to 2, 2.5, 3, 3.5, 4, 5, or 6. For more information, see Clock Domains on Page 9.
LCLKRAT2–0[1]	I (pd[2])	au	LCLK Ratio. The DSP's core clock (instruction cycle rate) = n × LCLK, where n is user-programmable to 2, 2.5, 3, 3.5, 4, 5, or 6 as shown in Table 4. These pins must have a constant value while the DSP is powered.
SCLK_N	I	au	System Clock Reference. Connect this pin to V_{REF} as shown in Figure 6.
SCLK_P	I	au	System Clock Input. The DSP's system input clock for cluster bus. This pin must be connected to the same clock source as LCLK_P. For more information, see Clock Domains on Page 9.
SCLKFREQ[3]	I (pu[2])	au	SCLK Frequency. SCLKFREQ = 1 is required. The SCLKFREQ pin must have a constant value while the DSP is powered.
$\overline{\text{RESET}}$	I/A	au	Reset. Sets the DSP to a known state and causes program to be in idle state. $\overline{\text{RESET}}$ must be asserted at specified time according to the type of reset operation. For details, see Reset and Booting on Page 9.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 4. LCLK Ratio

LCLKRAT2–0	Ratio
000 (default)	2
001	2.5
010	3
011	3.5
100	4
101	5
110	6
111	Reserved

Table 5. Pin Definitions—External Port Bus Controls (Continued)

Signal	Type	Term	Description
$\overline{MSH}$[2]	O/T (pu[3])	nc	Memory Select Host. $\overline{MSH}$ is asserted whenever the DSP accesses the host address space (ADDR31:28 ≠ 0b0000). $\overline{MSH}$ is a decoded memory address pin that changes concurrently with ADDR pins. In a multiprocessor system, the bus master DSP drives $\overline{MSH}$.
$\overline{BRST}$[2]	I/O/T (pu[3])	nc	Burst. The current bus master (DSP or host) asserts this pin to indicate that it is reading or writing data associated with consecutive addresses. A slave device can ignore addresses after the first one and increment an internal address counter after each transfer. For host-to-DSP burst accesses, the DSP increments the address automatically while $\overline{BRST}$ is asserted.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The address and data buses may float for several cycles during bus mastership transitions between a TigerSHARC processor and a host. Floating in this case means that these inputs are not driven by any source and that dc-biased terminations are not present. It is not necessary to add pull-ups as there are no reliability issues and the worst-case power consumption for these floating inputs is negligible. Unconnected address pins may require pull-ups or pull-downs to avoid erroneous slave accesses, depending on the system. Unconnected data pins may be left floating.

[2] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

[3] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

[4] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.

Table 6. Pin Definitions—External Port Arbitration

Signal	Type	Term	Description
$\overline{BR7–0}$	I/O	epu	Multiprocessing Bus Request Pins. Used by the DSPs in a multiprocessor system to arbitrate for bus mastership. Each DSP drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In systems with fewer than eight DSPs, set the unused $\overline{BRx}$ pins high.
ID2–0[1]	I (pd[2])	au	Multiprocessor ID. Indicates the DSP's ID. From the ID, the DSP determines its order in a multiprocessor system. These pins also indicate to the DSP which bus request ($\overline{BR0}$–$\overline{BR7}$) to assert when requesting the bus: 000 = $\overline{BR0}$, 001 = $\overline{BR1}$, 010 = $\overline{BR2}$, 011 = $\overline{BR3}$, 100 = $\overline{BR4}$, 101 = $\overline{BR5}$, 110 = $\overline{BR6}$, or 111 = $\overline{BR7}$. ID2–0 must have a constant value during system operation and can change during reset only.
$\overline{BM}$[1]	O (pd[2])	au	Bus Master. The current bus master DSP asserts $\overline{BM}$. For debugging only. At reset this is a strap pin. For more information, see Table 16 on Page 19.
$\overline{BOFF}$	I	epu	Back Off. A deadlock situation can occur when the host and a DSP try to read from each other's bus at the same time. When deadlock occurs, the host can assert $\overline{BOFF}$ to force the DSP to relinquish the bus before completing its outstanding transaction, but only if the outstanding transaction is to host memory space ($\overline{MSH}$).
$\overline{BUSLOCK}$[3]	O/T (pu[2])	nc	Bus Lock Indication. Provides an indication that the current bus master has locked the bus.
$\overline{HBR}$	I	epu	Host Bus Request. A host must assert $\overline{HBR}$ to request control of the DSP's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the bus master relinquishes the bus and asserts $\overline{HBG}$ once the outstanding transaction is finished.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

Table 6. Pin Definitions—External Port Arbitration (Continued)

Signal	Type	Term	Description
$\overline{HBG}$[3]	I/O/T (pu[2])	nc	Host Bus Grant. Acknowledges $\overline{HBR}$ and indicates that the host can take control of the external bus. When relinquishing the bus, the master DSP three-states the ADDR31–0, DATA63–0, $\overline{MSH}$, $\overline{MSSD}$, $\overline{MS1–0}$, $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{BMS}$, $\overline{BRST}$, $\overline{FLYBY}$, $\overline{IOEN}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, SDCKE, LDQM and HDQM pins, and the DSP puts the SDRAM in self-refresh mode. The DSP asserts $\overline{HBG}$ until the host deasserts $\overline{HBR}$. In multiprocessor systems, the current bus master DSP drives $\overline{HBG}$, and all slave DSPs monitor $\overline{HBG}$.
$\overline{CPA}$	I/O (o/d)	See next column	Core Priority Access. Asserted while the DSP's core accesses external memory. This pin enables a slave DSP to interrupt a master DSP's background DMA transfers and gain control of the external bus for core-initiated transactions. $\overline{CPA}$ is an open drain output, connected to all DSPs in the system. The $\overline{CPA}$ pin has an internal 500 Ω pull-up resistor, which is only enabled on the DSP with ID2–0 = 0. If ID0 is not used, terminate this pin as either epu or nc. If ID7–1 is not used, terminate this pin as epu.
$\overline{DPA}$	I/O (o/d)	See next column	DMA Priority Access. Asserted while a high-priority DSP DMA channel accesses external memory. This pin enables a high-priority DMA channel on a slave DSP to interrupt transfers of a normal-priority DMA channel on a master DSP and gain control of the external bus for DMA-initiated transactions. $\overline{DPA}$ is an open drain output, connected to all DSPs in the system. The $\overline{DPA}$ pin has an internal 500 Ω pull-up resistor, which is only enabled on the DSP with ID2–0 = 0. If ID0 is not used, terminate this pin as either epu or nc. If ID7–1 is not used, terminate this pin as epu.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 7. Pin Definitions—External Port DMA/Flyby

Signal	Type	Term	Description
$\overline{DMAR3–0}$	I/A	epu	DMA Request Pins. Enable external I/O devices to request DMA services from the DSP. In response to $\overline{DMARx}$, the DSP performs DMA transfers according to the DMA channel's initialization. The DSP ignores DMA requests from uninitialized channels.
$\overline{FLYBY}$[1]	O/T (pu[2])	nc	Flyby Mode. When a DSP DMA channel is initiated in $\overline{FLYBY}$ mode, it generates flyby transactions on the external bus. During flyby transactions, the DSP asserts $\overline{FLYBY}$, which signals the source or destination I/O device to latch the next data or strobe the current data, respectively, and to prepare for the next data on the next cycle.
$\overline{IOEN}$[1]	O/T (pu[2])	nc	I/O Device Output Enable. Enables the output buffers of an external I/O device for flyby transactions between the device and external memory. Active on flyby transactions.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 9. Pin Definitions—JTAG Port (Continued)

Signal	Type	Term	Description
TDO	O/T	nc[1]	Test Data Output (JTAG). A serial data output of the scan path.
TMS[2]	I (pu[3])	nc[1]	Test Mode Select (JTAG). Used to control the test state machine.
$\overline{\text{TRST}}$[2]	I/A (pu[3])	au	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted or pulsed low after power-up for proper device operation.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] See the reference Page 11 to the JTAG emulation technical reference EE-68.
[2] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[3] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 10. Pin Definitions—Flags, Interrupts, and Timer

Signal	Type	Term	Description
FLAG3–0[1]	I/O/A (pd[2])	nc	FLAG pins. Bidirectional input/output pins can be used as program conditions. Each pin can be configured individually for input or for output. FLAG3–0 are inputs after power-up and reset.
$\overline{\text{IRQ3–0}}$[3]	I/A (pu[2])	nc	Interrupt Request. When asserted, the DSP generates an interrupt. Each of the $\overline{\text{IRQ3–0}}$ pins can be independently set for edge triggered or level sensitive operation. After reset, these pins are disabled unless the $\overline{\text{IRQ3–0}}$ strap option is initialized for booting.
TMR0E[1]	O (pd[2])	au	Timer 0 expires. This output pulses for four SCLK cycles whenever timer 0 expires. At reset this is a strap pin. For additional information, see Table 16 on Page 19.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 11. Pin Definitions—Link Ports

Signal	Type	Term	Description
L0DAT7–0[1]	I/O	nc	Link0 Data 7–0
L1DAT7–0[1]	I/O	nc	Link1 Data 7–0
L2DAT7–0[1]	I/O	nc	Link2 Data 7–0
L3DAT7–0[1]	I/O	nc	Link3 Data 7–0
L0CLKOUT	O	nc	Link0 Clock/Acknowledge Output
L1CLKOUT	O	nc	Link1 Clock/Acknowledge Output
L2CLKOUT	O	nc	Link2 Clock/Acknowledge Output
L3CLKOUT	O	nc	Link3 Clock/Acknowledge Output
L0CLKIN	I/A	epu	Link0 Clock/Acknowledge Input
L1CLKIN	I/A	epu	Link1 Clock/Acknowledge Input
L2CLKIN	I/A	epu	Link2 Clock/Acknowledge Input
L3CLKIN	I/A	epu	Link3 Clock/Acknowledge Input
L0DIR	O	nc	Link0 Direction. (0 = input, 1 = output)

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

Table 11. Pin Definitions—Link Ports (Continued)

Signal	Type	Term	Description
L1DIR	O	nc	Link1 Direction. (0 = input, 1 = output)
L2DIR[2]	O (pd[3])	au	Link2 Direction. (0 = input, 1 = output) At reset this is a strap pin. For more information, see Table 16 on Page 19.
L3DIR	O (pd[3])	nc	Link3 Direction. (0 = input, 1 = output)
Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state			
Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.			

[1] The link port data pins, if connected or floated for extended periods (for example, token slave with no token master), do not require pull-ups or pull-downs as there are no reliability issues and the worst-case power consumption for these floating inputs is negligible. Floating in this case means that these inputs are not driven by any source and that dc-biased terminations are not present.
[2] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[3] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 12. Pin Definitions—Impedance and Drive Strength Control

Signal	Type	Term	Description
CONTROLIMP2–1[1] CONTROLIMP0[2]	I (pu[3]) I (pd[3])	au au	Impedance Control. For ADC (Address/Data/Controls) and LINK (all link port outputs) signals, the CONTROLIMP2–0 pins control impedance as shown in Table 13. These pins enable or disable dig_ctrl mode. When dig_ctrl: 0 = Disabled (maximum drive strength) 1 = Enabled (use DS2–0 drive strength selection)
DS2–0[1]	I (pu[3])	au	Digital Drive Strength Selection. Selected as shown in Table 14. For drive strength calculation, see Output Drive Currents on Page 32. The drive strength for some pins is preset, not controlled by the DS2–0 pins. The pins that are always at drive strength 7 (100%) are: $\overline{CPA}$, $\overline{DPA}$, and $\overline{EMU}$.
Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state			
Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.			

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[3] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 13. Control Impedance Selection

CONTROLIMP2–0	ADC dig_ctrl	LINK dig_ctrl
000	0	0
001	0	0
010	0	1
011	reserved	reserved
100	1	0
101	reserved	reserved
110 (default)	1	1
111	reserved	reserved

Table 14. Drive Strength Selection

DS2–0	Drive Strength
000	Strength 0
001	Strength 1
010	Strength 2
011	Strength 3
100	Strength 4
101	Strength 5
110	Strength 6
111 (default)	Strength 7

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{DD}	Internal Supply Voltage		1.14		1.26	V
V_{DD_A}	Analog Supply Voltage		1.14		1.26	V
V_{DD_IO}	I/O Supply Voltage		3.15		3.45	V
T_{CASE}	Case Operating Temperature		–40		+85	°C
V_{IH}	High Level Input Voltage[1]	@ V_{DD}, V_{DD_IO} = max	2		V_{DD_IO} + 0.5	V
V_{IL}	Low Level Input Voltage[1]	@ V_{DD}, V_{DD_IO} = min	–0.5		+0.8	V
I_{DD}	V_{DD} Supply Current for Typical Activity[2]	@ CCLK = 250 MHz, V_{DD} = 1.25 V, T_{CASE} = 25°C		1.2		A
I_{DD}	V_{DD} Supply Current for Typical Activity[2]	@ CCLK = 300 MHz, V_{DD} = 1.25 V, T_{CASE} = 25°C		1.5		A
$I_{DDIDLELP}$	V_{DD} Supply Current for IDLELP Instruction Execution	@ CCLK = 300 MHz, V_{DD} = 1.20 V, T_{CASE} = 25°C		173		mA
I_{DD_IO}	V_{DD_IO} Supply Current for Typical Activity[2]	@ SCLK = 100 MHz, V_{DD_IO} = 3.3 V, T_{CASE} = 25°C		137		mA
I_{DD_A}	V_{DD_A} Supply Current	@ V_{DD} = 1.25 V, T_{CASE} = 25°C		25	31.25	mA
V_{REF}	Voltage Reference		1.4		1.6	V

[1] Applies to input and bidirectional pins.
[2] For details on internal and external power estimation, including: power vector definitions, current usage descriptions, and formulas, see *EE-169, Estimating Power for the ADSP-TS101S* on the Analog Devices website—use site search on "EE-169" (www.analog.com). This document is updated regularly to keep pace with silicon revisions.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@V_{DD_IO} = min, I_{OH} = –2 mA	2.4		V
V_{OL}	Low Level Output Voltage[1]	@V_{DD_IO} = min, I_{OL} = 4 mA		0.4	V
I_{IH}	High Level Input Current[2]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max		10	µA
I_{IHP}	High Level Input Current (pd)[2]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max	17.2	44.5	µA
I_{IL}	Low Level Input Current[3]	@V_{DD_IO} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current (pu)[4]	@V_{DD_IO} = max, V_{IN} = 0 V	–69	–23	µA
I_{OZH}	Three-State Leakage Current High[5, 6]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max		10	µA
I_{OZHP}	Three-State Leakage Current High (pd)[7]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max	17.2	44.5	µA
I_{OZL}	Three-State Leakage Current Low[8]	@V_{DD_IO} = max, V_{IN} = 0 V		10	µA
I_{OZLP}	Three-State Leakage Current Low (pu)[9]	@V_{DD_IO} = max, V_{IN} = 0 V	–69	–23	µA
I_{OZLO}	Three-State Leakage Current Low (od)[7]	@V_{DD_IO} = max, V_{IN} = 0 V	–9.8	–4.6	mA
C_{IN}	Input Capacitance[10, 11]	@f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		5	pF

[1] Applies to output and bidirectional pins.
[2] Applies to input pins with internal pull-downs (pd).
[3] Applies to input pins without internal pull-ups (pu).
[4] Applies to input pins with internal pull-ups (pu).
[5] Applies to three-stateable pins without internal pull-downs (pd).
[6] Applies to open drain (od) pins with 500 Ω pull-ups (pu).
[7] Applies to three-stateable pins with internal pull-downs (pd).
[8] Applies to three-stateable pins without internal pull-ups (pu).
[9] Applies to three-stateable pins with internal pull-ups (pu).
[10] Applies to all signals.
[11] Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 19 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 17. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.40 V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.40 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD_IO} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DD_IO} + 0.5 V
Storage Temperature Range	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 7 provide details about the package branding for the ADSP-TS101S processors. For a complete listing of product availability, see Ordering Guide on Page 45.

Figure 7. Typical Package Brand

Table 18. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option (optional)
ccc	See Ordering Guide
LLLLLLLLL-L	Silicon Lot Number
R.R	Silicon Revision
yyww	Date Code
vvvvvv	Assembly Lot Code

TIMING SPECIFICATIONS

With the exception of link port, $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, TMR0E, FLAG3–0 (input), and $\overline{\text{TRST}}$ pins, all ac timing for the ADSP-TS101S is relative to a reference clock edge. Because input setup/hold, output valid/hold, and output enable/disable times are relative to a clock edge, the timing data for the ADSP-TS101S has few calculated (formula-based) values. For information on ac timing, see General AC Timing. For information on link port transfer timing, see Link Ports Data Transfer and Token Switch Timing on Page 29.

General AC Timing

Timing is measured on signals when they cross the 1.5 V level as described in Figure 16 on Page 28. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

The ac asynchronous timing data for the $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, TMR0E, FLAG3–0 (input), and $\overline{\text{TRST}}$ pins appears in Table 21.

The general ac timing data appears in Table 21, Table 29, and Table 30. All ac specifications are measured with the load specified in Figure 8, and with the output drive strength set to strength 4. Output valid and hold are based on standard capacitive loads: 30 pF on all pins. The delay and hold specifications given should be derated by a drive strength related factor for loads other than the nominal value of 30 pF.

In order to calculate the output valid and hold times for different load conditions and/or output drive strengths, refer to Figure 32 on Page 34 through Figure 39 on Page 36 (Rise and Fall Time vs. Load Capacitance) and Figure 40 on Page 36 (Output Valid vs. Load Capacitance and Drive Strength).

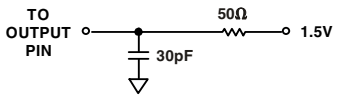

Figure 8. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

For power-up sequencing, power-up reset, and normal reset (hot reset) timing requirements, refer to Table 26 and Figure 13, Table 27 and Figure 14, and Table 28, and Figure 15 respectively.

Table 19. AC Asynchronous Signal Specifications (All values in this table are in nanoseconds)

Name	Description	Pulse Width Low (min)	Pulse Width High (min)
$\overline{IRQ3–0}$[1]	Interrupt request input	t_{CCLK} + 3 ns	
$\overline{DMAR3–0}$[1]	DMA request input	t_{CCLK} + 4 ns	t_{CCLK} + 4 ns
TMR0E[2]	Timer 0 expired output		4 × t_{SCLK} ns
FLAG3–0[1, 3]	Flag pins input	3 × t_{CCLK} ns	3 × t_{CCLK} ns
$\overline{TRST}$	JTAG test reset input	1 ns	

[1] These input pins do not need to be synchronized to a clock reference.
[2] This pin is a strap option. During reset, an internal resistor pulls the pin low.
[3] For output specifications, see Table 29 and Table 30.

Table 20. Reference Clocks—Core Clock (CCLK) Cycle Time

Parameter	Description	Grade = 100 (300 MHz) Min	Grade = 100 (300 MHz) Max	Grade = 000 (250 MHz) Min	Grade = 000 (250 MHz) Max	Unit
t_{CCLK}[1]	Core Clock Cycle Time	3.3	12.5	4.0	12.5	ns

[1] CCLK is the internal processor clock or instruction cycle time. The period of this clock is equal to the system clock period (t_{SCLK}) divided by the system clock ratio (SCLKRAT2–0). For information on available part numbers for different internal processor clock rates, see the Ordering Guide on Page 45.

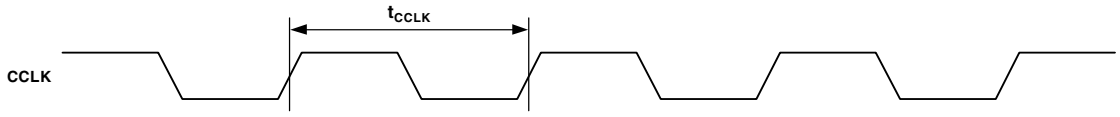

Figure 9. Reference Clocks—Core Clock (CCLK) Cycle Time

Table 21. Reference Clocks—Local Clock (LCLK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{LCLK}[1, 2, 3, 4]	Local Clock Cycle Time	10	25	ns
t_{LCLKH}	Local Clock Cycle High Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKL}	Local Clock Cycle Low Time	0.4 × t_{LCLK}	0.6 × t_{LCLK}	ns
t_{LCLKJ}[5, 6]	Local Clock Jitter Tolerance		500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] LCLK_P and SCLK_P must be connected to the same source.
[4] The value of (t_{LCLK} / LCLKRAT2-0) must not violate the specification for t_{CCLK}.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

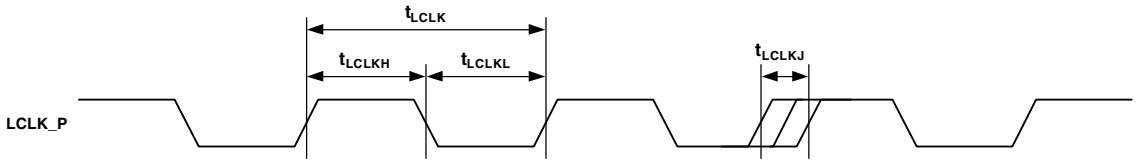

Figure 10. Reference Clocks—Local Clock (LCLK) Cycle Time

Table 22. Reference Clocks—System Clock (SCLK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{SCLK}[1, 2, 3, 4]	System Clock Cycle Time	10	25	ns
t_{SCLKH}	System Clock Cycle High Time	$0.4 \times t_{SCLK}$	$0.6 \times t_{SCLK}$	ns
t_{SCLKL}	System Clock Cycle Low Time	$0.4 \times t_{SCLK}$	$0.6 \times t_{SCLK}$	ns
t_{SCLKJ}[5, 6]	System Clock Jitter Tolerance		500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] LCLK_P and SCLK_P must be connected to the same source.
[4] The value of (t_{SCLK} / LCLKRAT2-0) must not violate the specification for t_{CCLK}.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

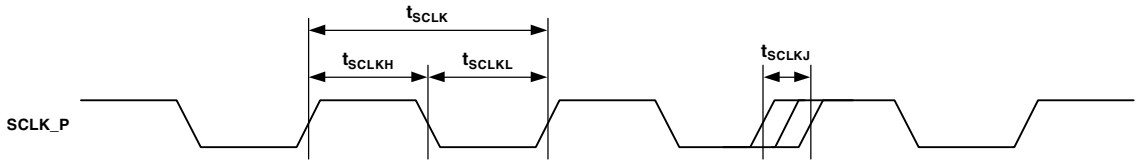

Figure 11. Reference Clocks—System Clock (SCLK) Cycle Time

Table 23. Reference Clocks—Test Clock (TCK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{TCK}	Test Clock (JTAG) Cycle Time	Greater of 30 or $t_{CCLK} \times 4$		ns
t_{TCKH}	Test Clock (JTAG) Cycle High Time	12.5		ns
t_{TCKL}	Test Clock (JTAG) Cycle Low Time	12.5		ns

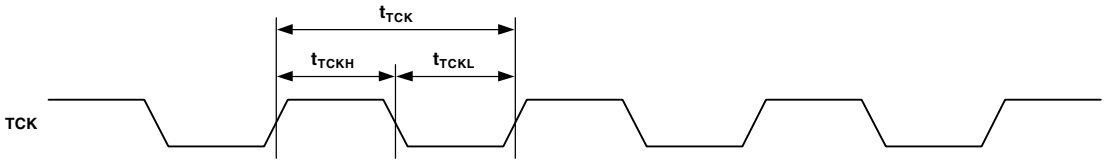

Figure 12. Reference Clocks—Test Clock (TCK) Cycle Time

Table 24. Power-Up Timing[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{VDD_IO}	V_{DD_IO} Stable and Within Specification After V_{DD} and V_{DD_A} Are Stable and Within Specification	>0		ms

[1] For information about power supply sequencing and monitoring solutions, please visit http://www.analog.com/sequencing.

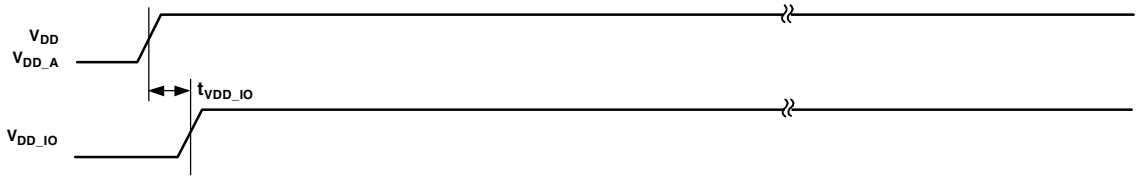

Figure 13. Power-Up Sequencing Timing

[1] The output valid (max) value in this column applies for the standard 30 pF capacitive load used in testing. To see how output valid varies with capacitive loading, see Figure 40 on Page 36.
[2] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.
[3] $\overline{CPA}$ and $\overline{DPA}$ pins are open drains and have 0.5 kΩ internal pull-ups.
[4] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference. These synchronous specifications only apply for recognition in the current clock reference cycle.
[5] This pin is a strap option. During reset, an internal resistor pulls the pin low.
[6] For input specifications, see Table 21.
[7] For additional requirement details, see Reset and Booting on Page 9.
[8] TCK_FE indicates TCK falling edge.
[9] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.
[10] Reference clock depends on function.
[11] System inputs are: $\overline{IRQ3–0}$, $\overline{BMS}$, LCLKRAT2–0, SCLKFREQ, $\overline{BM}$, TMR0E, FLAG3–0, ID2–0, $\overline{BRST}$, $\overline{WRH}$, $\overline{WRL}$, $\overline{RD}$, $\overline{MSSD}$, SDCKE, $\overline{SDWE}$, $\overline{CAS}$, $\overline{RAS}$, ADDR31–0, DATA63–0, $\overline{DPA}$, $\overline{CPA}$, $\overline{HBG}$, $\overline{BOFF}$, $\overline{HBR}$, ACK, $\overline{BR7–0}$, L0CLKIN, L0DAT7–0, L1CLKIN, L1DAT7–0, L2CLKIN, L2DAT7–0, L2DIR, L3CLKIN, L3DAT7–0, DS2–0, CONTROLIMP2–0, $\overline{RESET}$, $\overline{DMAR3–0}$.
[12] System outputs are: $\overline{BMS}$, $\overline{BM}$, $\overline{BUSLOCK}$, TMR0E, FLAG3–0, $\overline{FLYBY}$, $\overline{IOEN}$, $\overline{MSH}$, $\overline{BRST}$, $\overline{WRH}$, $\overline{WRL}$, $\overline{RD}$, $\overline{MS1–0}$, HDQM, LDQM, $\overline{MSSD}$, SDCKE, $\overline{SDWE}$, $\overline{CAS}$, $\overline{RAS}$, ADDR31–0, DATA63–0, $\overline{DPA}$, $\overline{CPA}$, $\overline{HBG}$, ACK, $\overline{BR7–0}$, L0CLKOUT, L0DAT7–0, L0DIR, L1CLKOUT, L1DAT7–0, L1DIR, L2CLKOUT, L2DAT7–0, L2DIR, L3CLKOUT, L3DAT7–0, L3DIR, $\overline{EMU}$.

Table 28. AC Signal Specifications (for 16.7 ns <SCLK <25 ns) (All values in this table are in nanoseconds)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
ADDR31–0	External Address Bus	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
DATA63–0	External Data Bus	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{MSH}$	Memory Select Host Line			4.2	0.8	0.3	2.5	SCLK
$\overline{MSSD}$	Memory Select SDRAM Line	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{MS1–0}$	Memory Select for Static Blocks			4.2	0.8	0.3	2.5	SCLK
$\overline{RD}$	Memory Read	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{WRL}$	Write Low Word	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{WRH}$	Write High Word	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
ACK	Acknowledge for Data	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
SDCKE	SDRAM Clock Enable	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{RAS}$	Row Address Select	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{CAS}$	Column Address Select	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{SDWE}$	SDRAM Write Enable	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
LDQM	Low Word SDRAM Data Mask			4.2	0.8	0.3	2.5	SCLK
HDQM	High Word SDRAM Data Mask			4.2	0.8	0.3	2.5	SCLK
SDA10	SDRAM ADDR10			4.2	0.8	0.3	2.5	SCLK
$\overline{HBR}$	Host Bus Request	2.8	0.5					SCLK
$\overline{HBG}$	Host Bus Grant	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{BOFF}$	Back Off Request	2.8	0.5					SCLK
$\overline{BUSLOCK}$	Bus Lock			4.2	0.8	0.3	2.5	SCLK
$\overline{BRST}$	Burst Access	2.8	0.5	4.2	0.8	0.3	2.5	SCLK
$\overline{BR7–0}$	Multiprocessing Bus Request	2.8	0.5	4.2	0.8			SCLK
$\overline{FLYBY}$	Flyby Mode Selection			4.2	0.8	0.3	2.5	SCLK
$\overline{IOEN}$	Flyby Mode I/O Enable			4.2	0.8	0.3	2.5	SCLK
$\overline{CPA}$ [3, 4]	Core Priority Access	2.8	0.5	5.8			2.5	SCLK
$\overline{DPA}$ [3, 4]	DMA Priority Access	2.8	0.5	5.8			2.5	SCLK
$\overline{BMS}$[5]	Boot Memory Select			4.2	0.8	0.3	2.5	SCLK
FLAG3–0[6]	FLAG Pins			4.2	1.0	1.0	4.0	SCLK

Table 28. AC Signal Specifications (for 16.7 ns <SCLK <25 ns) (All values in this table are in nanoseconds) (Continued)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	0.8			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

[1] The output valid (max) value in this column applies for the standard 30 pF capacitive load used in testing. To see how output valid varies with capacitive loading, see Figure 40 on Page 36.

[2] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.

[3] $\overline{\text{CPA}}$ and $\overline{\text{DPA}}$ pins are open drains and have 0.5 kΩ internal pull-ups.

[4] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference. These synchronous specifications only apply for recognition in the current clock reference cycle.

[5] This pin is a strap option. During reset, an internal resistor pulls the pin low.

[6] For input specifications, see Table 21.

[7] For additional requirement details, see Reset and Booting on Page 9.

[8] TCK_FE indicates TCK falling edge.

[9] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.

[10] Reference clock depends on function.

[11] System inputs are: $\overline{\text{IRQ3–0}}$, $\overline{\text{BMS}}$, LCLKRAT2–0, SCLKFREQ, $\overline{\text{BM}}$, TMR0E, FLAG3–0, ID2–0, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, $\overline{\text{BOFF}}$, $\overline{\text{HBR}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKIN, L0DAT7–0, L1CLKIN, L1DAT7–0, L2CLKIN, L2DAT7–0, L2DIR, L3CLKIN, L3DAT7–0, DS2–0, CONTROLIMP2–0, $\overline{\text{RESET}}$, $\overline{\text{DMAR3–0}}$.

[12] System outputs are: $\overline{\text{BMS}}$, $\overline{\text{BM}}$, $\overline{\text{BUSLOCK}}$, TMR0E, FLAG3–0, $\overline{\text{FLYBY}}$, $\overline{\text{IOEN}}$, $\overline{\text{MSH}}$, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MS1–0}}$, HDQM, LDQM, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKOUT, L0DAT7–0, L0DIR, L1CLKOUT, L1DAT7–0, L1DIR, L2CLKOUT, L2DAT7–0, L2DIR, L3CLKOUT, L3DAT7–0, L3DIR, $\overline{\text{EMU}}$.

Link Ports Data Transfer and Token Switch Timing

Table 31, Table 32, Table 33, and Table 34 with Figure 17, Figure 18, Figure 19, and Figure 20 provide the timing specifications for the link ports data transfer and token switch.

Table 29. Link Ports—Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{CONNS}[1]	Connectivity Pulse Setup	$2 \times t_{CCLK} + 3.5$		ns
t_{CONNS}[2]	Connectivity Pulse Setup	8		ns
t_{CONNIW}[3]	Connectivity Pulse Input Width	$t_{LxCLK\_Tx} + 1$		ns
t_{ACKS}	Acknowledge Setup	$0.5 \times t_{LxCLK\_Tx}$		ns
Switching Characteristics				
t_{LxCLK_Tx}[4]	Transmit Link Clock Period	$0.9 \times LR \times t_{CCLK}$	$1.1 \times LR \times t_{CCLK}$	ns
t_{LxCLKH_Tx}[1]	Transmit Link Clock Width High	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKH_Tx}[2]	Transmit Link Clock Width High	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[1]	Transmit Link Clock Width Low	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[2]	Transmit Link Clock Width Low	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{DIRS}	LxDIR Transmit Setup	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DIRH}	LxDIR Transmit Hold	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DOS}[1]	LxDAT7–0 Output Setup	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[1]	LxDAT7–0 Output Hold	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOS}[2]	LxDAT7–0 Output Setup	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[2]	LxDAT7–0 Output Hold	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{LDOE}	LxDAT7–0 Output Enable	1		ns
t_{LDOD}[5]	LxDAT7–0 Output Disable	1		ns

[1] The formula for this parameter applies when LR is 2.
[2] The formula for this parameter applies when LR is 3, 4, or 8.
[3] LxCLKIN shows the connectivity pulse with each of the three possible transitions to "Acknowledge." After a connectivity pulse low minimum, LxCLKIN may [1] return high and remain high for "Acknowledge," [2] return high and subsequently go low (meeting t_{ACKS}) for "Not Acknowledge," or [3] remain low for "Not Acknowledge."
[4] The Link clock Ratio (LR) is 2, 3, 4, or 8 as set by the SPD bits in the LCTLx register. The maximum LxCLK is 125 MHz. LR = 2 may not be used when CCLK ≥ 250 MHz.
[5] This specification applies to the last data byte or the "Dummy" byte that follows the verification byte if enabled. For more information, see the *ADSP-TS101* TigerSHARC *Processor Hardware Reference*.

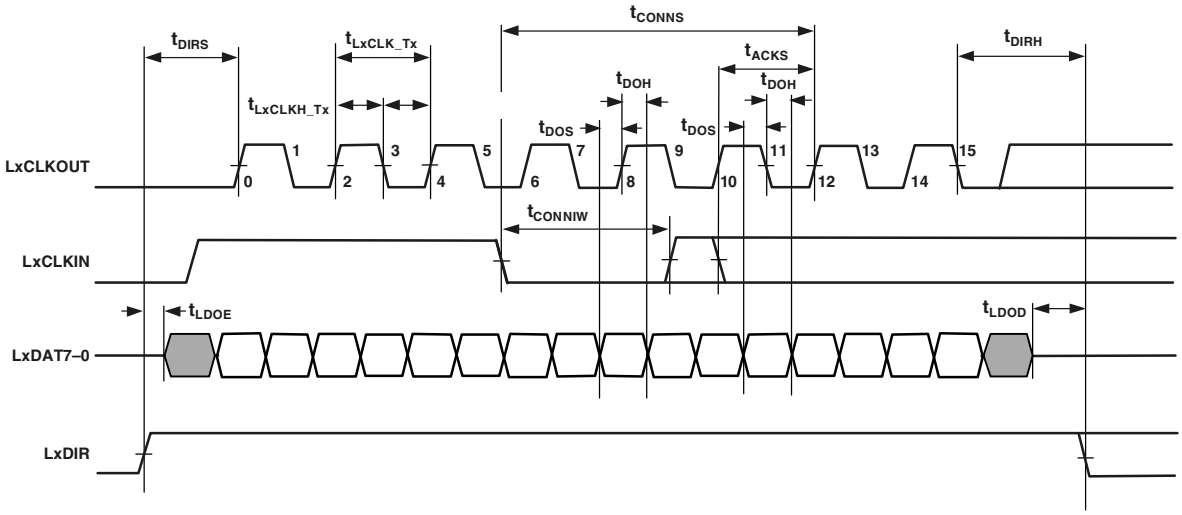

Figure 17. Link Ports—Transmit

Table 31. Link Ports—Token Switch, Token Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{REQI}	Token Request Input Width	$5.0 \times t_{LxCLK\_Rx}$		ns
t_{TKRQ}	Token Request from Token Enable[1]		$3.0 \times t_{LxCLK\_Tx}$	ns
Switching Characteristics				
t_{TKENO}	Token Switch Enable Output	$8.0 \times t_{LxCLK\_Tx}$		ns
t_{REQO}	Token Request Output Width[2]	$6.0 \times t_{LxCLK\_Tx}$		ns

[1] For guaranteeing token switch during token enable.
[2] LxCLKOUT shows both possible responses to the token request: [1] a "Token Grant" (LxCLKOUT remains high), and [2] a "Token Regret" (LxCLKOUT goes low).

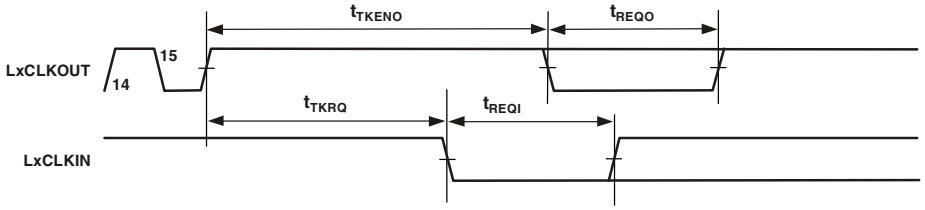

Figure 19. Link Ports—Token Switch, Token Master

Table 32. Link Ports—Token Switch, Token Requester

Parameter		Min	Max	Unit
Timing Requirements				
t_{TKENI}[1]	Token Switch Enable Input	$8.0 \times t_{LxCLK\_Rx}$		ns
Switching Characteristics				
t_{REQO}	Token Request Output Width[2]	$6.0 \times t_{LxCLK\_Rx}$		ns

[1] Required whenever there is a break in transmission.
[2] LxCLKOUT shows both possible responses to the token request: [1] a "Token Grant" (LxCLKOUT remains high), and [2] a "Token Regret" (LxCLKOUT goes low).

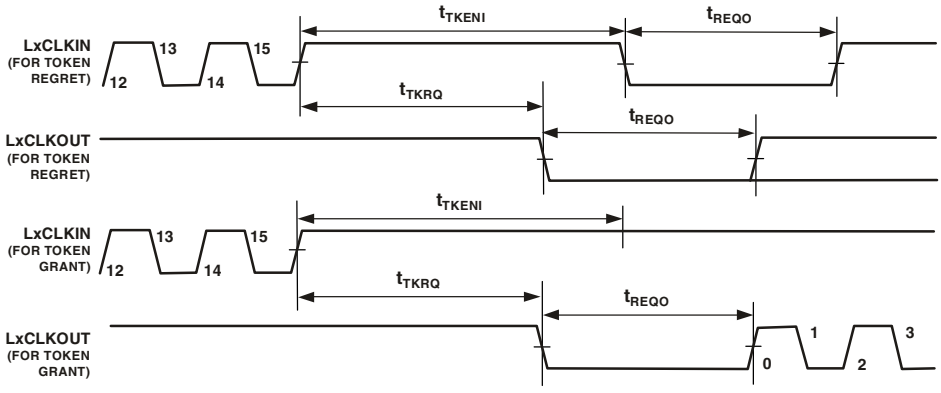

Figure 20. Link Ports—Token Switch, Token Requester

OUTPUT DRIVE CURRENTS

Figure 21 through Figure 28 show typical I–V characteristics for the output drivers of the ADSP-TS101S. The curves in these diagrams represent the current drive capability of the output drivers as a function of output voltage over the range of drive strengths. For complete output driver characteristics, refer to IBIS models, available on the Analog Devices website, www.analog.com.

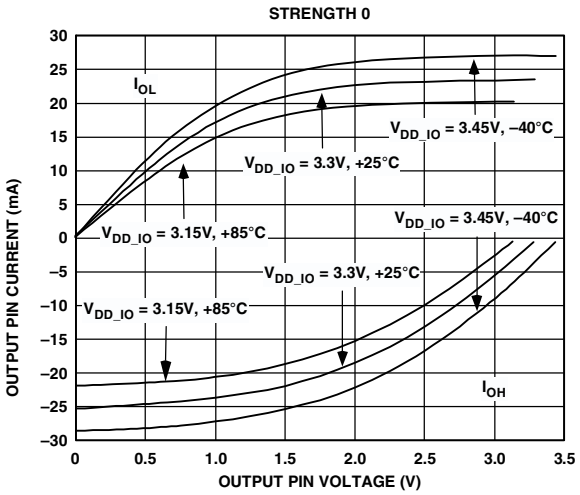

Figure 21. Typical Drive Currents at Strength 0

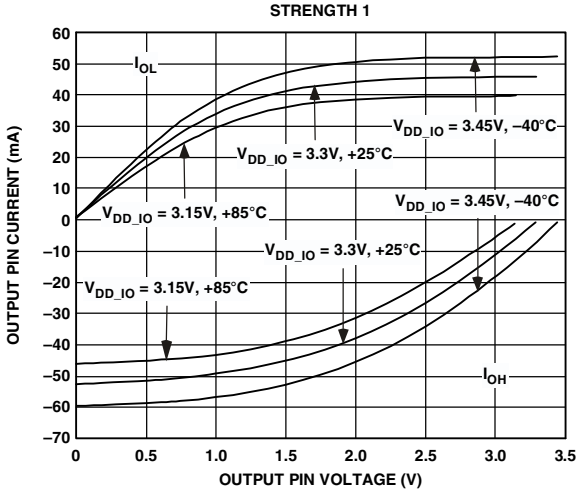

Figure 22. Typical Drive Currents at Strength 1

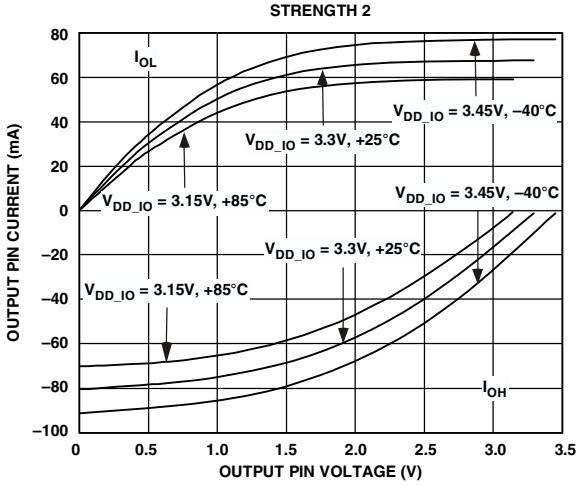

Figure 23. Typical Drive Currents at Strength 2

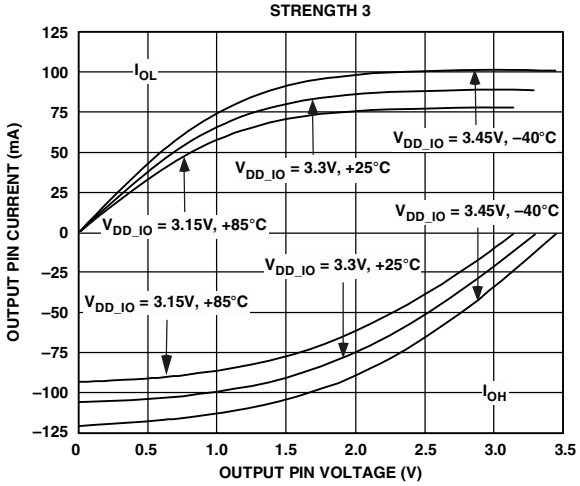

Figure 24. Typical Drive Currents at Strength 3

TEST CONDITIONS

The test conditions for timing parameters appearing in Table 29 on Page 29 and Table 30 on Page 30 include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 29.

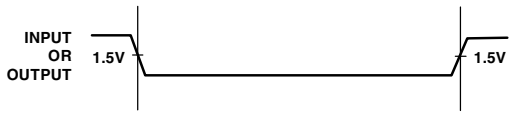

Figure 29. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

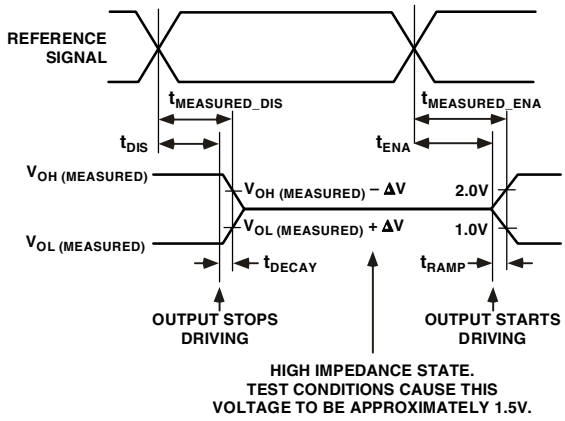

Figure 30. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED\_DIS}$ and t_{DECAY} as shown in Figure 30. The time $t_{MEASURED\_DIS}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. The t_{DECAY} value is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The time for the voltage on the bus to ramp by ΔV is dependent on the capacitive load, C_L, and the drive current, I_D. This ramp time can be approximated by the following equation:

$$t_{RAMP} = \frac{C_L \Delta V}{I_D}$$

The output enable time t_{ENA} is the difference between $t_{MEASURED\_ENA}$ and t_{RAMP} as shown in Figure 30. The time $t_{MEASURED\_ENA}$ is the interval from when the reference signal switches to when the output voltage ramps ΔV from the measured three-stated output level. The t_{RAMP} value is calculated with test load C_L, drive current I_D, and with ΔV equal to 0.5 V.

Capacitive Loading

Figure 31 shows the circuit with variable capacitance that is used for measuring typical output rise and fall times. Figure 32 through Figure 39 show how output rise time varies with capacitance. Figure 40 graphically shows how output valid varies with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 34.) The graphs of Figure 32 through Figure 40 may not be linear outside the ranges shown.

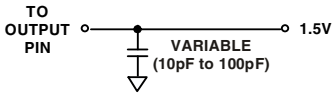

Figure 31. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

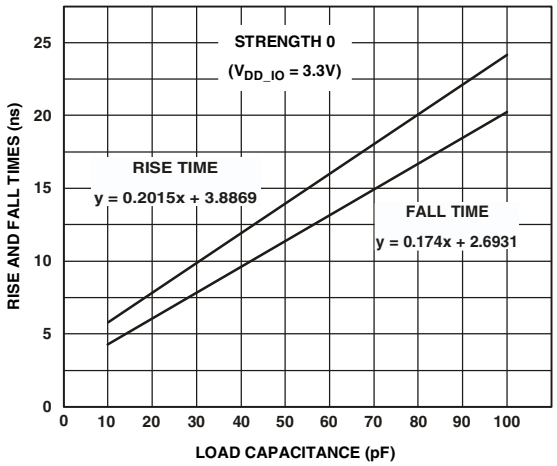

Figure 32. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 0

Table 35. 484-Ball (19 mm × 19 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
F22	TMR0E	G22	FLAG0	H22	ID1	J22	$\overline{\text{MSH}}$	K22	$\overline{\text{WRL}}$
L1	L3CLKIN	M1	L1DAT0	N1	L1DAT3	P1	L1DAT4	R1	L1DAT6
L2	NC	M2	L1DAT2	N2	L1DAT5	P2	L1CLKOUT	R2	DATA32
L3	L3DIR	M3	L1DAT1	N3	L1DAT7	P3	L1CLKIN	R3	DATA33
L4	V_{DD_IO}	M4	V_{DD_IO}	N4	V_{DD_IO}	P4	V_{DD_IO}	R4	V_{DD_IO}
L5	V_{DD}	M5	V_{SS}	N5	V_{DD_IO}	P5	V_{DD}	R5	V_{DD}
L6	V_{SS}	M6	V_{SS}	N6	V_{SS}	P6	V_{SS}	R6	V_{SS}
L7	V_{SS}	M7	V_{SS}	N7	V_{SS}	P7	V_{SS}	R7	V_{SS}
L8	V_{SS}	M8	V_{SS}	N8	V_{SS}	P8	V_{SS}	R8	V_{SS}
L9	V_{SS}	M9	V_{SS}	N9	V_{SS}	P9	V_{SS}	R9	V_{SS}
L10	V_{SS}	M10	V_{SS}	N10	V_{SS}	P10	V_{SS}	R10	V_{SS}
L11	V_{SS}	M11	V_{SS}	N11	V_{SS}	P11	V_{SS}	R11	V_{SS}
L12	V_{SS}	M12	V_{SS}	N12	V_{SS}	P12	V_{SS}	R12	V_{SS}
L13	V_{SS}	M13	V_{SS}	N13	V_{SS}	P13	V_{SS}	R13	V_{SS}
L14	V_{SS}	M14	V_{SS}	N14	V_{SS}	P14	V_{SS}	R14	V_{SS}
L15	V_{SS}	M15	V_{SS}	N15	V_{SS}	P15	V_{SS}	R15	V_{SS}
L16	V_{SS}	M16	V_{SS}	N16	V_{SS}	P16	V_{SS}	R16	V_{SS}
L17	V_{SS}	M17	V_{SS}	N17	V_{SS}	P17	V_{SS}	R17	V_{SS}
L18	V_{DD_IO}	M18	V_{DD_IO}	N18	V_{DD}	P18	V_{DD_IO}	R18	V_{DD}
L19	V_{DD_IO}	M19	V_{DD}	N19	V_{DD_IO}	P19	V_{DD_IO}	R19	V_{DD_IO}
L20	$\overline{\text{BRST}}$	M20	HDQM	N20	$\overline{\text{SDWE}}$	P20	ADDR31	R20	ADDR28
L21	$\overline{\text{WRH}}$	M21	$\overline{\text{MS0}}$	N21	$\overline{\text{MSSD}}$	P21	$\overline{\text{RAS}}$	R21	ADDR29
L22	$\overline{\text{RD}}$	M22	$\overline{\text{MS1}}$	N22	LDQM	P22	SDCKE	R22	$\overline{\text{CAS}}$
T1	L1DIR	U1	NC	V1	DATA34	W1	DATA40	Y1	DATA42
T2	DATA36	U2	DATA38	V2	DATA41	W2	DATA43	Y2	DATA45
T3	DATA37	U3	DATA39	V3	DATA35	W3	DATA46	Y3	L2DAT5
T4	V_{DD_IO}	U4	V_{DD_IO}	V4	V_{DD_IO}	W4	V_{DD_IO}	Y4	DATA48
T5	V_{DD}	U5	V_{DD}	V5	V_{DD}	W5	V_{DD_IO}	Y5	DATA52
T6	V_{SS}	U6	V_{SS}	V6	V_{DD}	W6	V_{DD_IO}	Y6	DATA58
T7	V_{SS}	U7	V_{SS}	V7	V_{DD_IO}	W7	V_{DD_IO}	Y7	DATA60
T8	V_{SS}	U8	V_{SS}	V8	V_{DD}	W8	V_{DD_IO}	Y8	DATA63
T9	V_{SS}	U9	V_{SS}	V9	V_{DD}	W9	V_{DD_IO}	Y9	L2DAT4
T10	V_{SS}	U10	V_{SS}	V10	V_{DD}	W10	V_{DD_IO}	Y10	L2CLKOUT
T11	V_{SS}	U11	V_{SS}	V11	V_{DD}	W11	V_{DD_IO}	Y11	NC
T12	V_{SS}	U12	V_{SS}	V12	V_{DD_IO}	W12	V_{DD_IO}	Y12	$\overline{\text{BR4}}$
T13	V_{SS}	U13	V_{SS}	V13	V_{DD}	W13	V_{DD_IO}	Y13	ACK
T14	V_{SS}	U14	V_{SS}	V14	V_{SS}	W14	V_{DD_IO}	Y14	$\overline{\text{CPA}}$
T15	V_{SS}	U15	V_{SS}	V15	V_{DD}	W15	V_{DD_IO}	Y15	ADDR0
T16	V_{SS}	U16	V_{SS}	V16	V_{DD}	W16	V_{DD_IO}	Y16	$\overline{\text{BR7}}$
T17	V_{SS}	U17	V_{SS}	V17	V_{DD}	W17	V_{DD_IO}	Y17	$\overline{\text{HBG}}$
T18	V_{DD}	U18	V_{DD}	V18	V_{DD}	W18	V_{DD_IO}	Y18	ADDR1
T19	V_{DD_IO}	U19	V_{DD_IO}	V19	V_{DD_IO}	W19	V_{DD_IO}	Y19	ADDR11
T20	ADDR23	U20	ADDR30	V20	ADDR14	W20	ADDR12	Y20	ADDR21
T21	ADDR25	U21	ADDR22	V21	ADDR19	W21	ADDR17	Y21	ADDR18
T22	ADDR27	U22	ADDR26	V22	ADDR24	W22	ADDR20	Y22	ADDR16

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
A1	V_{SS}	B1	V_{SS}	C1	V_{SS}	D1	V_{SS}	E1	DATA23
A2	DATA17	B2	V_{SS}	C2	DATA20	D2	V_{SS}	E2	DATA22
A3	DATA14	B3	DATA16	C3	DATA21	D3	DATA19	E3	V_{SS}
A4	DATA11	B4	DATA13	C4	DATA18	D4	V_{DD_IO}	E4	V_{DD_IO}
A5	DATA9	B5	DATA12	C5	DATA15	D5	V_{DD_IO}	E5	V_{DD_IO}
A6	DATA7	B6	DATA10	C6	DATA8	D6	V_{DD_IO}	E6	V_{DD}
A7	DATA4	B7	DATA5	C7	DATA6	D7	V_{DD_IO}	E7	V_{DD}
A8	DATA1	B8	DATA2	C8	DATA3	D8	V_{DD_IO}	E8	V_{DD_IO}
A9	L0DIR	B9	NC	C9	DATA0	D9	V_{DD_IO}	E9	V_{DD_IO}
A10	L0DAT7	B10	L0CLKOUT	C10	L0CLKIN	D10	V_{DD_IO}	E10	V_{DD}
A11	L0DAT4	B11	L0DAT5	C11	L0DAT6	D11	V_{DD_IO}	E11	V_{DD}
A12	L0DAT1	B12	L0DAT2	C12	L0DAT3	D12	V_{DD_IO}	E12	V_{DD_IO}
A13	LCLK_N	B13	V_{SS}	C13	L0DAT0	D13	V_{DD_IO}	E13	V_{DD_IO}
A14	LCLK_P	B14	V_{SS}	C14	V_{SS_A}	D14	V_{DD_IO}	E14	V_{DD}
A15	V_{DD_A}	B15	V_{SS_A}	C15	V_{DD_A}	D15	V_{DD_IO}	E15	V_{DD}
A16	SCLK_N	B16	SCLK_P	C16	V_{SS}	D16	V_{DD_IO}	E16	V_{DD_IO}
A17	V_{REF}	B17	V_{SS}	C17	DS0	D17	V_{DD_IO}	E17	V_{DD_IO}
A18	DS1	B18	DS2	C18	CONTROLIMP0	D18	V_{DD_IO}	E18	V_{DD}
A19	CONTROLIMP2	B19	CONTROLIMP1	C19	$\overline{\text{DMAR1}}$	D19	V_{DD_IO}	E19	V_{DD}
A20	$\overline{\text{RESET}}$	B20	$\overline{\text{DMAR3}}$	C20	TDI	D20	V_{DD_IO}	E20	V_{DD_IO}
A21	$\overline{\text{DMAR2}}$	B21	$\overline{\text{DMAR0}}$	C21	$\overline{\text{IRQ2}}$	D21	V_{DD_IO}	E21	V_{DD_IO}
A22	$\overline{\text{EMU}}$	B22	$\overline{\text{IRQ3}}$	C22	LCLKRAT0	D22	V_{DD_IO}	E22	V_{DD_IO}
A23	$\overline{\text{TRST}}$	B23	TCK	C23	LCLKRAT1	D23	$\overline{\text{BMS}}$	E23	V_{SS}
A24	TMS	B24	$\overline{\text{IRQ1}}$	C24	$\overline{\text{IRQ0}}$	D24	V_{SS}	E24	SCLKFREQ
A25	V_{SS}	B25	TDO	C25	V_{SS}	D25	V_{SS}	E25	LCLKRAT2
F1	DATA26	G1	DATA29	H1	L3DAT0	J1	L3DAT3	K1	L3DAT6
F2	DATA25	G2	DATA28	H2	DATA31	J2	L3DAT2	K2	L3DAT5
F3	DATA24	G3	DATA27	H3	DATA30	J3	L3DAT1	K3	L3DAT4
F4	V_{DD_IO}	G4	V_{DD_IO}	H4	V_{DD_IO}	J4	V_{DD_IO}	K4	V_{DD_IO}
F5	V_{DD_IO}	G5	V_{DD}	H5	V_{DD}	J5	V_{DD_IO}	K5	V_{DD_IO}
F6	V_{DD}	G6	V_{DD}	H6	V_{DD}	J6	V_{DD}	K6	V_{DD}
F7	V_{DD}	G7	V_{SS}	H7	V_{SS}	J7	V_{SS}	K7	V_{SS}
F8	V_{DD}	G8	V_{SS}	H8	V_{SS}	J8	V_{SS}	K8	V_{SS}
F9	V_{DD}	G9	V_{SS}	H9	V_{SS}	J9	V_{SS}	K9	V_{SS}
F10	V_{DD}	G10	V_{SS}	H10	V_{SS}	J10	V_{SS}	K10	V_{SS}
F11	V_{DD}	G11	V_{SS}	H11	V_{SS}	J11	V_{SS}	K11	V_{SS}
F12	V_{DD}	G12	V_{SS}	H12	V_{SS}	J12	V_{SS}	K12	V_{SS}
F13	V_{DD}	G13	V_{SS}	H13	V_{SS}	J13	V_{SS}	K13	V_{SS}
F14	V_{DD}	G14	V_{SS}	H14	V_{SS}	J14	V_{SS}	K14	V_{SS}
F15	V_{DD}	G15	V_{SS}	H15	V_{SS}	J15	V_{SS}	K15	V_{SS}
F16	V_{DD}	G16	V_{SS}	H16	V_{SS}	J16	V_{SS}	K16	V_{SS}
F17	V_{DD}	G17	V_{SS}	H17	V_{SS}	J17	V_{SS}	K17	V_{SS}
F18	V_{DD}	G18	V_{SS}	H18	V_{SS}	J18	V_{SS}	K18	V_{SS}
F19	V_{DD}	G19	V_{SS}	H19	V_{SS}	J19	V_{SS}	K19	V_{SS}
F20	V_{DD}	G20	V_{DD}	H20	V_{DD}	J20	V_{DD}	K20	V_{DD}
F21	V_{DD}	G21	V_{DD}	H21	V_{DD_IO}	J21	V_{DD_IO}	K21	V_{DD}
F22	V_{DD_IO}	G22	V_{DD_IO}	H22	V_{DD_IO}	J22	V_{DD_IO}	K22	V_{DD_IO}
F23	$\overline{\text{BM}}$	G23	FLAG3	H23	FLAG0	J23	ID0	K23	NC
F24	$\overline{\text{BUSLOCK}}$	G24	FLAG2	H24	ID2	J24	NC	K24	NC
F25	TMR0E	G25	FLAG1	H25	ID1	J25	NC	K25	NC

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
L1	L3CLKIN	M1	L1DAT0	N1	L1DAT2	P1	L1DAT5	R1	L1CLKOUT
L2	L3CLKOUT	M2	NC	N2	NC	P2	L1DAT4	R2	L1DAT7
L3	L3DAT7	M3	L3DIR	N3	L1DAT1	P3	L1DAT3	R3	L1DAT6
L4	V_{DD_IO}	M4	V_{DD_IO}	N4	V_{DD_IO}	P4	V_{DD_IO}	R4	V_{DD_IO}
L5	V_{DD}	M5	V_{DD}	N5	V_{DD_IO}	P5	V_{DD_IO}	R5	V_{DD}
L6	V_{DD}	M6	V_{DD}	N6	V_{DD}	P6	V_{DD}	R6	V_{DD}
L7	V_{SS}	M7	V_{SS}	N7	V_{SS}	P7	V_{SS}	R7	V_{SS}
L8	V_{SS}	M8	V_{SS}	N8	V_{SS}	P8	V_{SS}	R8	V_{SS}
L9	V_{SS}	M9	V_{SS}	N9	V_{SS}	P9	V_{SS}	R9	V_{SS}
L10	V_{SS}	M10	V_{SS}	N10	V_{SS}	P10	V_{SS}	R10	V_{SS}
L11	V_{SS}	M11	V_{SS}	N11	V_{SS}	P11	V_{SS}	R11	V_{SS}
L12	V_{SS}	M12	V_{SS}	N12	V_{SS}	P12	V_{SS}	R12	V_{SS}
L13	V_{SS}	M13	V_{SS}	N13	V_{SS}	P13	V_{SS}	R13	V_{SS}
L14	V_{SS}	M14	V_{SS}	N14	V_{SS}	P14	V_{SS}	R14	V_{SS}
L15	V_{SS}	M15	V_{SS}	N15	V_{SS}	P15	V_{SS}	R15	V_{SS}
L16	V_{SS}	M16	V_{SS}	N16	V_{SS}	P16	V_{SS}	R16	V_{SS}
L17	V_{SS}	M17	V_{SS}	N17	V_{SS}	P17	V_{SS}	R17	V_{SS}
L18	V_{SS}	M18	V_{SS}	N18	V_{SS}	P18	V_{SS}	R18	V_{SS}
L19	V_{SS}	M19	V_{SS}	N19	V_{SS}	P19	V_{SS}	R19	V_{SS}
L20	V_{DD}	M20	V_{DD}	N20	V_{DD}	P20	V_{DD}	R20	V_{DD}
L21	V_{DD}	M21	V_{DD_IO}	N21	V_{DD_IO}	P21	V_{DD}	R21	V_{DD}
L22	V_{DD_IO}	M22	V_{DD_IO}	N22	V_{DD_IO}	P22	V_{DD_IO}	R22	V_{DD_IO}
L23	NC	M23	$\overline{\text{IOEN}}$	N23	$\overline{\text{WRH}}$	P23	$\overline{\text{MS1}}$	R23	LDQM
L24	NC	M24	$\overline{\text{MSH}}$	N24	$\overline{\text{WRL}}$	P24	$\overline{\text{MS0}}$	R24	NC
L25	$\overline{\text{FLYBY}}$	M25	$\overline{\text{BRST}}$	N25	$\overline{\text{RD}}$	P25	HDQM	R25	$\overline{\text{MSSD}}$
T1	NC	U1	DATA34	V1	DATA37	W1	DATA40	Y1	DATA43
T2	L1DIR	U2	DATA33	V2	DATA36	W2	DATA39	Y2	DATA42
T3	L1CLKIN	U3	DATA32	V3	DATA35	W3	DATA38	Y3	DATA41
T4	V_{DD_IO}	U4	V_{DD_IO}	V4	V_{DD_IO}	W4	V_{DD_IO}	Y4	V_{DD_IO}
T5	V_{DD}	U5	V_{DD_IO}	V5	V_{DD_IO}	W5	V_{DD}	Y5	V_{DD}
T6	V_{DD}	U6	V_{DD}	V6	V_{DD}	W6	V_{DD}	Y6	V_{DD}
T7	V_{SS}	U7	V_{SS}	V7	V_{SS}	W7	V_{SS}	Y7	V_{DD}
T8	V_{SS}	U8	V_{SS}	V8	V_{SS}	W8	V_{SS}	Y8	V_{DD}
T9	V_{SS}	U9	V_{SS}	V9	V_{SS}	W9	V_{SS}	Y9	V_{DD}
T10	V_{SS}	U10	V_{SS}	V10	V_{SS}	W10	V_{SS}	Y10	V_{DD}
T11	V_{SS}	U11	V_{SS}	V11	V_{SS}	W11	V_{SS}	Y11	V_{DD}
T12	V_{SS}	U12	V_{SS}	V12	V_{SS}	W12	V_{SS}	Y12	V_{DD}
T13	V_{SS}	U13	V_{SS}	V13	V_{SS}	W13	V_{SS}	Y13	V_{DD}
T14	V_{SS}	U14	V_{SS}	V14	V_{SS}	W14	V_{SS}	Y14	V_{DD}
T15	V_{SS}	U15	V_{SS}	V15	V_{SS}	W15	V_{SS}	Y15	V_{DD}
T16	V_{SS}	U16	V_{SS}	V16	V_{SS}	W16	V_{SS}	Y16	V_{DD}
T17	V_{SS}	U17	V_{SS}	V17	V_{SS}	W17	V_{SS}	Y17	V_{DD}
T18	V_{SS}	U18	V_{SS}	V18	V_{SS}	W18	V_{SS}	Y18	V_{DD}
T19	V_{SS}	U19	V_{SS}	V19	V_{SS}	W19	V_{SS}	Y19	V_{DD}
T20	V_{DD}	U20	V_{DD}	V20	V_{DD}	W20	V_{DD}	Y20	V_{DD}
T21	V_{DD_IO}	U21	V_{DD_IO}	V21	V_{DD}	W21	V_{DD}	Y21	V_{DD_IO}
T22	V_{DD_IO}	U22	V_{DD_IO}	V22	V_{DD_IO}	W22	V_{DD_IO}	Y22	V_{DD_IO}
T23	SDCKE	U23	$\overline{\text{CAS}}$	V23	ADDR31	W23	ADDR28	Y23	ADDR26
T24	NC	U24	NC	V24	ADDR30	W24	NC	Y24	ADDR25
T25	$\overline{\text{SDWE}}$	U25	$\overline{\text{RAS}}$	V25	ADDR29	W25	ADDR27	Y25	ADDR24

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
AA1	DATA46	AB1	DATA49	AC1	V_{SS}	AD1	V_{SS}	AE1	V_{SS}
AA2	DATA45	AB2	DATA48	AC2	V_{SS}	AD2	V_{SS}	AE2	V_{SS}
AA3	DATA44	AB3	DATA47	AC3	DATA50	AD3	V_{SS}	AE3	V_{SS}
AA4	V_{DD_IO}	AB4	V_{DD_IO}	AC4	DATA51	AD4	DATA52	AE4	DATA53
AA5	V_{DD_IO}	AB5	V_{DD_IO}	AC5	DATA54	AD5	DATA55	AE5	DATA56
AA6	V_{DD_IO}	AB6	V_{DD_IO}	AC6	DATA57	AD6	DATA58	AE6	DATA59
AA7	V_{DD}	AB7	V_{DD_IO}	AC7	DATA60	AD7	DATA61	AE7	DATA62
AA8	V_{DD}	AB8	V_{DD_IO}	AC8	DATA63	AD8	L2DAT0	AE8	L2DAT1
AA9	V_{DD_IO}	AB9	V_{DD_IO}	AC9	L2DAT2	AD9	L2DAT3	AE9	L2DAT4
AA10	V_{DD_IO}	AB10	V_{DD_IO}	AC10	L2DAT5	AD10	L2DAT6	AE10	L2DAT7
AA11	V_{DD}	AB11	V_{DD_IO}	AC11	L2CLKOUT	AD11	L2CLKIN	AE11	L2DIR
AA12	V_{DD}	AB12	V_{DD_IO}	AC12	NC	AD12	$\overline{BR0}$	AE12	$\overline{BR1}$
AA13	V_{DD_IO}	AB13	V_{DD_IO}	AC13	$\overline{BR2}$	AD13	$\overline{BR3}$	AE13	$\overline{BR4}$
AA14	V_{DD_IO}	AB14	V_{DD_IO}	AC14	$\overline{BR5}$	AD14	$\overline{BR6}$	AE14	$\overline{BR7}$
AA15	V_{DD}	AB15	V_{DD_IO}	AC15	ACK	AD15	$\overline{HBR}$	AE15	$\overline{BOFF}$
AA16	V_{DD}	AB16	V_{DD_IO}	AC16	$\overline{HBG}$	AD16	$\overline{CPA}$	AE16	$\overline{DPA}$
AA17	V_{DD_IO}	AB17	V_{DD_IO}	AC17	ADDR0	AD17	ADDR1	AE17	ADDR2
AA18	V_{DD_IO}	AB18	V_{DD_IO}	AC18	ADDR3	AD18	ADDR4	AE18	ADDR5
AA19	V_{DD}	AB19	V_{DD_IO}	AC19	ADDR6	AD19	ADDR7	AE19	ADDR8
AA20	V_{DD}	AB20	V_{DD_IO}	AC20	ADDR9	AD20	SDA10	AE20	ADDR10
AA21	V_{DD_IO}	AB21	V_{DD_IO}	AC21	ADDR11	AD21	ADDR12	AE21	ADDR13
AA22	V_{DD_IO}	AB22	V_{DD_IO}	AC22	ADDR14	AD22	ADDR15	AE22	V_{SS}
AA23	ADDR23	AB23	ADDR20	AC23	V_{SS}	AD23	V_{SS}	AE23	V_{SS}
AA24	ADDR22	AB24	ADDR19	AC24	ADDR17	AD24	V_{SS}	AE24	V_{SS}
AA25	ADDR21	AB25	ADDR18	AC25	ADDR16	AD25	V_{SS}	AE25	V_{SS}

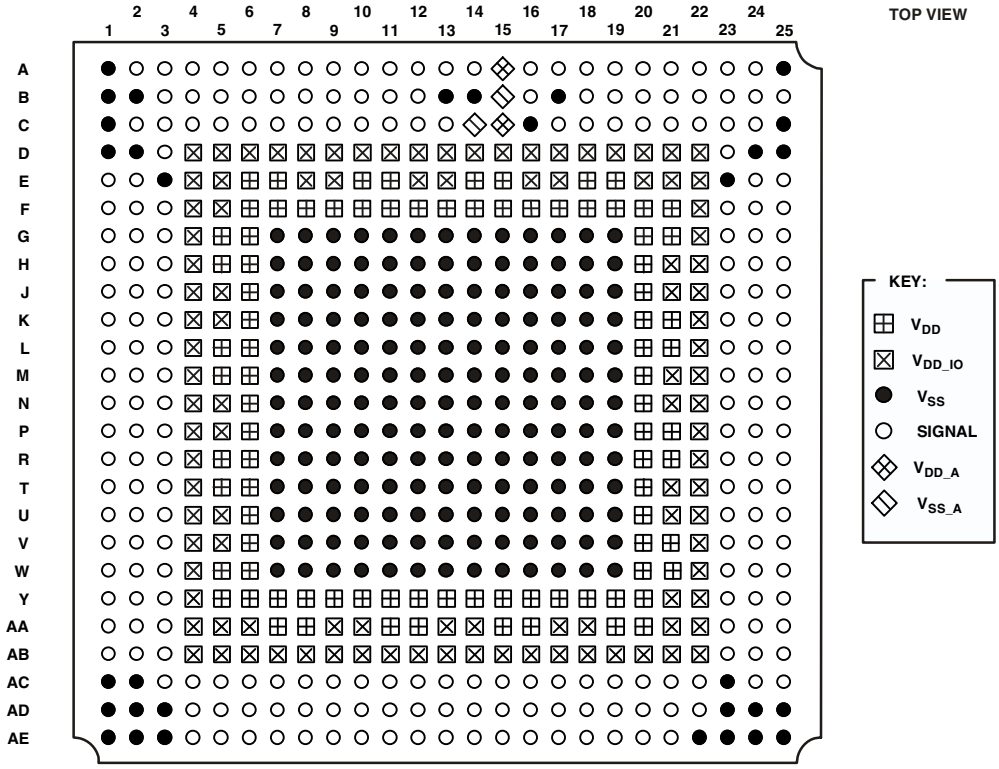

Figure 42. 625-Ball PBGA Pin Configurations (Top View, Summary)