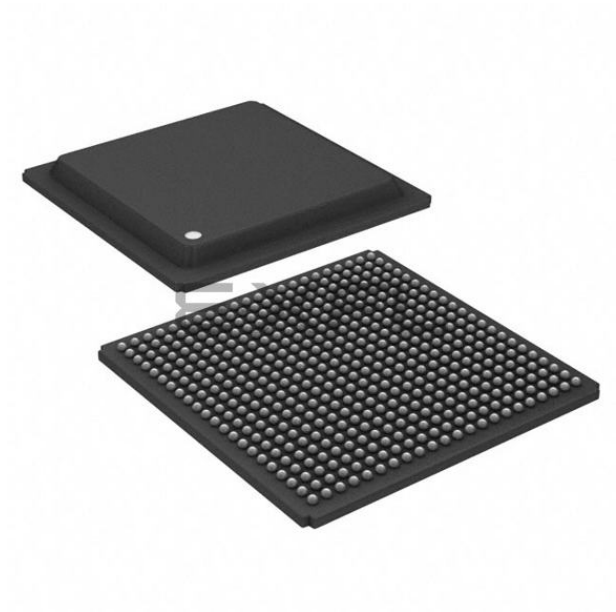

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	768kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	484-BFBGA
Supplier Device Package	484-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts101sab2-100

Data Sheet

- ADSP-TS101S: TigerSHARC Embedded Processor, 300 MHz, 6 Mbits, Data Sheet

Evaluation Kit Manuals

- ADSP-TS101S EZ-KIT Lite® Manual

Integrated Circuit Anomalies

- ADSP-TS101S TigerSHARC Anomaly List for Revision(s) 0.2, 0.4

Processor Manuals

- ADSP-TS101 TigerSHARC Processor Hardware Reference
- ADSP-TS101 TigerSHARC Processor Programming Reference
- TigerSHARC Processors: Manuals

Product Highlight

- General-Purpose TigerSHARC Processor Product Brief

Software Manuals

- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for TigerSHARC Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- TigerSHARC Evaluation Kits

TOOLS AND SIMULATIONS

- ADSP-TS101 TigerSHARC BSDL File 19x19mm PBGA Package for Revision 0.4, (11/2006)
- ADSP-TS101 TigerSHARC BSDL File 27x27mm PBGA Package for Revision 0.4, (11/2006)
- ADSP-TS101: 19x19mm PBGA Silicon Revision 0.0 and 0.1 [BSDL Original File], 02/08/2001
- ADSP-TS101: 19x19mm PBGA Package Silicon Revision 0.2, [BSDL Original File], 09/09/2003
- ADSP-TS101: 27x27 PBGA Package Siicon Revision 0.2, [BSDL Original File], 09/09/2003
- ADSP-TS101: 27x27 PBGA Package Silicon Revision 0.0 and 0.1 [BSDL Original File], 10/12/2001
- Designing with BGA
- TigerSHARC Processors: Software and Tools
- ADSP-TS101S IBIS Datafile BGA Package

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- A Software Solution for Chip Rate Processing in CDMA Wireless Infrastructure
- ADSP-TS101S MP System Simulation and Analysis
- Continuous Real-Time Signal Processing -- Comparing TigerSHARC and PowerPC Via Continuous cFFTs
- Rethinking Base Station, Baseband Processing for Wireless Communication
- SHARC Bites Back - The Memory Inside: TigerSHARC Swallows Its DRAM

White Papers

- ADSP-TS101S MP System Simulation and Analysis

DESIGN RESOURCES

- ADSP-TS101S Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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The IALUs have hardware support for circular buffers, bit reverse, and zero-overhead looping. Circular buffers facilitate efficient programming of delay lines and other data structures required in digital signal processing, and they are commonly used in digital filters and Fourier transforms. Each IALU provides registers for four circular buffers, so applications can set up a total of eight circular buffers. The IALUs handle address pointer wraparound automatically, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Because the IALU's computational pipeline is one cycle deep, in most cases, integer results are available in the next cycle. Hardware (register dependency check) causes a stall if a result is unavailable in a given cycle.

PROGRAM SEQUENCER

The ADSP-TS101S processor's program sequencer supports:

- A fully interruptible programming model with flexible programming in assembly and C/C++ languages; handles hardware interrupts with high throughput and no aborted instruction cycles.
- An eight-cycle instruction pipeline—three-cycle fetch pipe and five-cycle execution pipe—with computation results available two cycles after operands are available.
- The supply of instruction fetch memory addresses; the sequencer's instruction alignment buffer (IAB) caches up to five fetched instruction lines waiting to execute; the program sequencer extracts an instruction line from the IAB and distributes it to the appropriate core component for execution.
- The management of program structures and determination of program flow according to JUMP, CALL, RTI, RTS instructions, loop structures, conditions, interrupts, and software exceptions.
- Branch prediction and a 128-entry branch target buffer (BTB) to reduce branch delays for efficient execution of conditional and unconditional branch instructions and zero-overhead looping; correctly predicted branches that are taken occur with zero-to-two overhead cycles, overcoming the three-to-six stage branch penalty.
- Compact code without the requirement to align code in memory; the IAB handles alignment.

Interrupt Controller

The DSP supports nested and non-nested interrupts. Each interrupt type has a register in the interrupt vector table. Also, each has a bit in both the interrupt latch register and the interrupt mask register. All interrupts are fixed as either level sensitive or edge sensitive, except the $\overline{\text{IRQ3–0}}$ hardware interrupts, which are programmable.

The DSP distinguishes between hardware interrupts and software exceptions, handling them differently. When a software exception occurs, the DSP aborts all other instructions in the instruction pipe. When a hardware interrupt occurs, the DSP continues to execute instructions already in the instruction pipe.

Flexible Instruction Set

The 128-bit instruction line, which can contain up to four 32-bit instructions, accommodates a variety of parallel operations for concise programming. For example, one instruction line can direct the DSP to conditionally execute a multiply, an add, and a subtract in both computation blocks while it also branches to another location in the program. Some key features of the instruction set include:

- Enhanced instructions for communications infrastructure to govern trellis decoding (for example, Viterbi and turbo decoders) and despreading via complex correlations
- Algebraic assembly language syntax
- Direct support for all DSP, imaging, and video arithmetic types, eliminating hardware modes
- Branch prediction encoded in instruction, enables zero-overhead loops
- Parallelism encoded in instruction line
- Conditional execution optional for all instructions
- User-defined, programmable partitioning between program and data memory

ON-CHIP SRAM MEMORY

The ADSP-TS101S has 6M bits of on-chip SRAM memory, divided into three blocks of 2M bits (64K words × 32 bits). Each block—M0, M1, and M2—can store program, data, or both, so applications can configure memory to suit specific needs. Placing program instructions and data in different memory blocks, however, enables the DSP to access data while performing an instruction fetch.

The DSP's internal and external memory (Figure 3) is organized into a unified memory map, which defines the location (address) of all elements in the system. The memory map is divided into four memory areas—host space, external memory, multiprocessor space, and internal memory—and each memory space, except host memory, is subdivided into smaller memory spaces.

Each internal memory block connects to one of the 128-bit-wide internal buses—block M0 to bus MD0, block M1 to bus MD1, and block M2 to bus MD2—enabling the DSP to perform three memory transfers in the same cycle. The DSP's internal bus architecture provides a total memory bandwidth of 14.4G bytes per second, enabling the core and I/O to access eight 32-bit data words (256 bits) and four 32-bit instructions each cycle. The DSP's flexible memory structure enables:

- DSP core and I/O access of different memory blocks in the same cycle
- DSP core access of all three memory blocks in parallel—one instruction and two data accesses
- Programmable partitioning of program and data memory
- Program access of all memory as 32-, 64-, or 128-bit words—16-bit words with the DAB
- Complete context switch in less than 20 cycles (66 ns)

The DMA controller also supports two-dimensional transfers. The DMA controller can access and transfer two-dimensional memory arrays on any DMA transmit or receive channel. These transfers are implemented with index, count, and modify registers for both the X and Y dimensions.

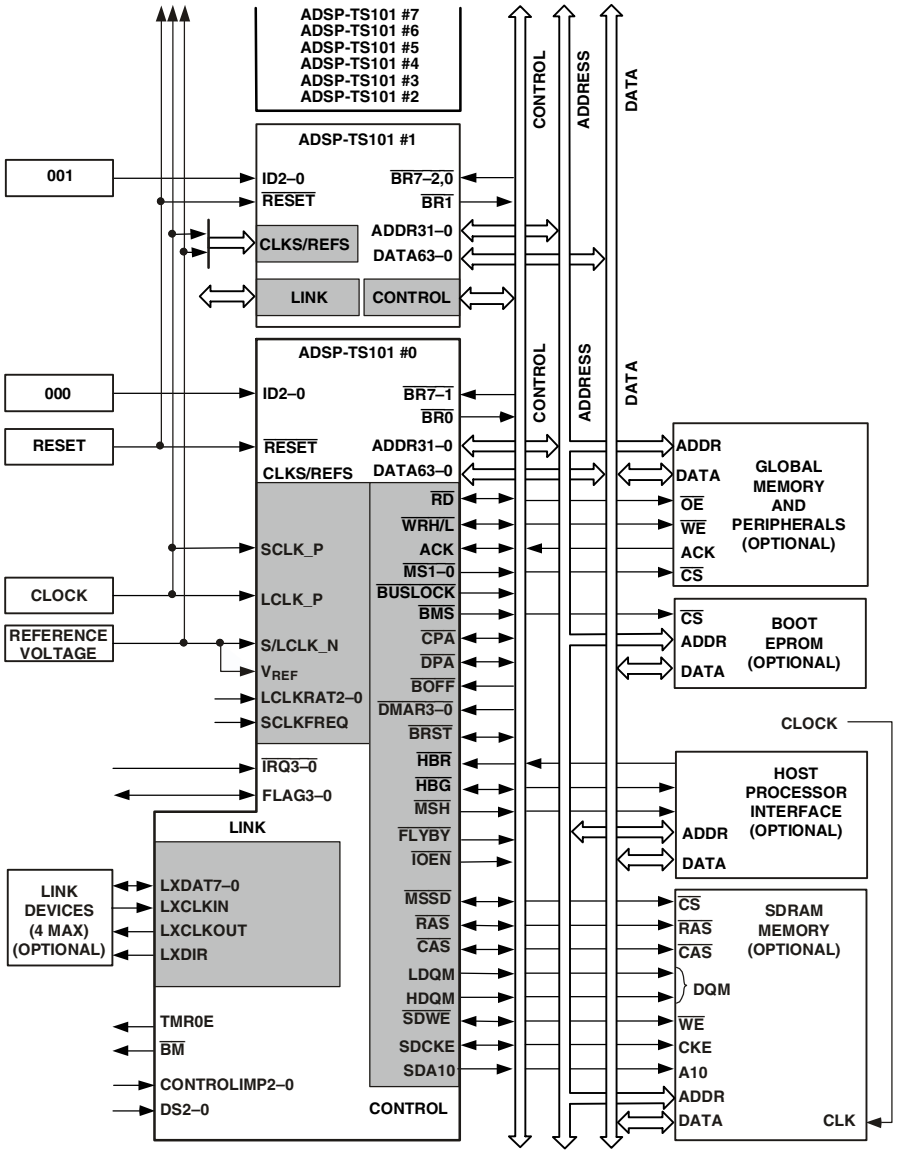

Figure 4. Shared Memory Multiprocessing System

The DMA controller performs the following DMA operations:

- External port block transfers. Four dedicated bidirectional DMA channels transfer blocks of data between the DSP's internal memory and any external memory or memory-mapped peripheral on the external bus. These transfers support master mode and handshake mode protocols.
- Link port transfers. Eight dedicated DMA channels (four transmit and four receive) transfer quad word data only between link ports and between a link port and internal or external memory. These transfers only use handshake mode protocol. DMA priority rotates between the four receive channels.
- AutoDMA transfers. Two dedicated unidirectional DMA channels transfer data received from an external bus master to internal memory or to link port I/O. These transfers only use slave mode protocol, and an external bus master must initiate the transfer.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ integrated development and debugging environment (IDDE) lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the TigerSHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command-line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command-line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the DSP or external memory with a drag of the mouse, examine run-time stack and heap usage. The Expert Linker is fully compatible with existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices DSP emulators use the IEEE 1149.1 JTAG Test Access Port of the ADSP-TS101S processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the TigerSHARC processor family. Hardware tools include TigerSHARC processor PC plug-in cards. Third-party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

DESIGNING AN EMULATOR-COMPATIBLE DSP BOARD (TARGET)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG DSP. The emulator uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-TS101S processor's architecture and functionality. For detailed information on the ADSP-TS101S processor's core architecture and instruction set, see the *ADSP-TS101 TigerSHARC Processor Programming Reference* and the *ADSP-TS101 TigerSHARC Processor Hardware Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

PIN FUNCTION DESCRIPTIONS

While most of the ADSP-TS101S processor's input pins are normally synchronous—tied to a specific clock—a few are asynchronous. For these asynchronous signals, an on-chip synchronization circuit prevents metastability problems. The synchronous ac specification for asynchronous signals is used only when predictable cycle-by-cycle behavior is required.

All inputs are sampled by a clock reference, therefore input specifications (asynchronous minimum pulse widths or synchronous input setup and hold) must be met to guarantee recognition.

PIN STATES AT RESET

The output pins can be three-stated during normal operation. The DSP three-states all outputs during reset, allowing these pins to get to their internal pull-up or pull-down state. Some output pins (control signals) have a pull-up or pull-down that maintains a known value during transitions between different drivers.

PIN DEFINITIONS

The Type column in the following pin definitions tables describes the pin type, when the pin is used in the system. The Term (for termination) column describes the pin termination type if the pin is not used by the system. Note that some pins are always used (indicated with au symbol).

Table 3. Pin Definitions—Clocks and Reset

Signal	Type	Term	Description
LCLK_N	I	au	Local Clock Reference. Connect this pin to V_{REF} as shown in Figure 6.
LCLK_P	I	au	Local Clock Input. DSP clock input. The instruction cycle rate = n × LCLK, where n is user-programmable to 2, 2.5, 3, 3.5, 4, 5, or 6. For more information, see Clock Domains on Page 9.
LCLKRAT2–0[1]	I (pd[2])	au	LCLK Ratio. The DSP's core clock (instruction cycle rate) = n × LCLK, where n is user-programmable to 2, 2.5, 3, 3.5, 4, 5, or 6 as shown in Table 4. These pins must have a constant value while the DSP is powered.
SCLK_N	I	au	System Clock Reference. Connect this pin to V_{REF} as shown in Figure 6.
SCLK_P	I	au	System Clock Input. The DSP's system input clock for cluster bus. This pin must be connected to the same clock source as LCLK_P. For more information, see Clock Domains on Page 9.
SCLKFREQ[3]	I (pu[2])	au	SCLK Frequency. SCLKFREQ = 1 is required. The SCLKFREQ pin must have a constant value while the DSP is powered.
$\overline{\text{RESET}}$	I/A	au	Reset. Sets the DSP to a known state and causes program to be in idle state. $\overline{\text{RESET}}$ must be asserted at specified time according to the type of reset operation. For details, see Reset and Booting on Page 9.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 4. LCLK Ratio

LCLKRAT2–0	Ratio
000 (default)	2
001	2.5
010	3
011	3.5
100	4
101	5
110	6
111	Reserved

Table 6. Pin Definitions—External Port Arbitration (Continued)

Signal	Type	Term	Description
$\overline{HBG}$[3]	I/O/T (pu[2])	nc	Host Bus Grant. Acknowledges $\overline{HBR}$ and indicates that the host can take control of the external bus. When relinquishing the bus, the master DSP three-states the ADDR31–0, DATA63–0, $\overline{MSH}$, $\overline{MSSD}$, $\overline{MS1–0}$, $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{BMS}$, $\overline{BRST}$, $\overline{FLYBY}$, $\overline{IOEN}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, SDCKE, LDQM and HDQM pins, and the DSP puts the SDRAM in self-refresh mode. The DSP asserts $\overline{HBG}$ until the host deasserts $\overline{HBR}$. In multiprocessor systems, the current bus master DSP drives $\overline{HBG}$, and all slave DSPs monitor $\overline{HBG}$.
$\overline{CPA}$	I/O (o/d)	See next column	Core Priority Access. Asserted while the DSP's core accesses external memory. This pin enables a slave DSP to interrupt a master DSP's background DMA transfers and gain control of the external bus for core-initiated transactions. $\overline{CPA}$ is an open drain output, connected to all DSPs in the system. The $\overline{CPA}$ pin has an internal 500 Ω pull-up resistor, which is only enabled on the DSP with ID2–0 = 0. If ID0 is not used, terminate this pin as either epu or nc. If ID7–1 is not used, terminate this pin as epu.
$\overline{DPA}$	I/O (o/d)	See next column	DMA Priority Access. Asserted while a high-priority DSP DMA channel accesses external memory. This pin enables a high-priority DMA channel on a slave DSP to interrupt transfers of a normal-priority DMA channel on a master DSP and gain control of the external bus for DMA-initiated transactions. $\overline{DPA}$ is an open drain output, connected to all DSPs in the system. The $\overline{DPA}$ pin has an internal 500 Ω pull-up resistor, which is only enabled on the DSP with ID2–0 = 0. If ID0 is not used, terminate this pin as either epu or nc. If ID7–1 is not used, terminate this pin as epu.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 7. Pin Definitions—External Port DMA/Flyby

Signal	Type	Term	Description
$\overline{DMAR3–0}$	I/A	epu	DMA Request Pins. Enable external I/O devices to request DMA services from the DSP. In response to $\overline{DMARx}$, the DSP performs DMA transfers according to the DMA channel's initialization. The DSP ignores DMA requests from uninitialized channels.
$\overline{FLYBY}$[1]	O/T (pu[2])	nc	Flyby Mode. When a DSP DMA channel is initiated in $\overline{FLYBY}$ mode, it generates flyby transactions on the external bus. During flyby transactions, the DSP asserts $\overline{FLYBY}$, which signals the source or destination I/O device to latch the next data or strobe the current data, respectively, and to prepare for the next data on the next cycle.
$\overline{IOEN}$[1]	O/T (pu[2])	nc	I/O Device Output Enable. Enables the output buffers of an external I/O device for flyby transactions between the device and external memory. Active on flyby transactions.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.

Table 8. Pin Definitions—External Port SDRAM Controller

Signal	Type	Term	Description
$\overline{\text{MSSD}}$[1]	I/O/T (pu[2])	nc	Memory Select SDRAM. $\overline{\text{MSSD}}$ is asserted whenever the DSP accesses SDRAM memory space. $\overline{\text{MSSD}}$ is a decoded memory address pin that is asserted whenever the DSP issues an SDRAM command cycle (access to ADDR31:26 = 0b000001). MSSD in a multiprocessor system is driven by the master DSP.
$\overline{\text{RAS}}$[1]	I/O/T (pu[2])	nc	Row Address Select. When sampled low, $\overline{\text{RAS}}$ indicates that a row address is valid in a read or write of SDRAM. In other SDRAM accesses, RAS defines the type of operation to execute according to SDRAM specification.
$\overline{\text{CAS}}$[1]	I/O/T (pu[2])	nc	Column Address Select. When sampled low, $\overline{\text{CAS}}$ indicates that a column address is valid in a read or write of SDRAM. In other SDRAM accesses, $\overline{\text{CAS}}$ defines the type of operation to execute according to the SDRAM specification.
LDQM[1]	O/T (pu[2])	nc	Low Word SDRAM Data Mask. When LDQM is sampled high, the DSP three-states the SDRAM DQ buffers. LDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted and is inactive on read transactions. On write transactions, LDQM is active when accessing an odd address word on a 64-bit memory bus to disable the write of the low word.
HDQM[1]	O/T (pu[2])	nc	High Word SDRAM Data Mask. When HDQM is sampled high, the DSP three-states the SDRAM DQ buffers. HDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted and is inactive on read transactions. On write transactions, HDQM is active when accessing an even address in word accesses or is active when memory is configured for a 32-bit bus to disable the write of the high word.
SDA10[1]	O/T (pu[2])	nc	SDRAM Address bit 10 pin. Separate A10 signals enable SDRAM refresh operation while the DSP executes non-SDRAM transactions.
SDCKE[1, 3]	I/O/T (pu/pd[2])	nc	SDRAM Clock Enable. Activates the SDRAM clock for SDRAM self-refresh or suspend modes. A slave DSP in a multiprocessor system does not have the pull-up or pull-down. A master DSP (or ID = 0 in a single processor system) has a 100 kΩ pull-up before granting the bus to the host, except when the SDRAM is put in self-refresh mode. In self-refresh mode, the master has a 100 kΩ pull-down before granting the bus to the host.
$\overline{\text{SDWE}}$[1]	I/O/T (pu[2])	nc	SDRAM Write Enable. When sampled low while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM write access. When sampled high while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM read access. In other SDRAM accesses, $\overline{\text{SDWE}}$ defines the type of operation to execute according to SDRAM specification.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

[1] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.

Table 9. Pin Definitions—JTAG Port

Signal	Type	Term	Description
$\overline{\text{EMU}}$	O (o/d)	nc[1]	Emulation. Connected only to the DSP's JTAG emulator target board connector.
TCK	I	epd or epu[1]	Test Clock (JTAG). Provides an asynchronous clock for JTAG scan.
TDI[2]	I (pu[3])	nc[1]	Test Data Input (JTAG). A serial data input of the scan path.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to $V_{DD\text{-}IO}$, nc = not connected; au = always used.

Table 15. Pin Definitions—Power, Ground, and Reference

Signal	Type	Term	Description
V_{DD}	P	au	V_{DD} pins for internal logic.
V_{DD_A}	P	au	V_{DD} pins for analog circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	au	V_{DD} pins for I/O buffers.
V_{REF}	I	au	Reference voltage defines the trip point for all input buffers, except $\overline{RESET}$, $\overline{IRQ3–0}$, $\overline{DMAR3–0}$, ID2–0, CONTROLIMP2–0, TCK, TDI, TMS, and $\overline{TRST}$. The value is 1.5 V ± 100 mV (which is the TTL trip point). V_{REF} can be connected to a power supply or set by a voltage divider circuit. The voltage divider should have an HF decoupling capacitor (1 nF HF SMD) connected to V_{SS}. Tie the decoupling capacitor between V_{REF} input and V_{SS}, as close to the DSP's pins as possible. For more information, see Filtering Reference Voltage and Clocks on Page 10.
V_{SS}	G	au	Ground pins.
V_{SS_A}	G	au	Ground pins for analog circuits.
NC			No connect. Do not connect these pins to anything (not to any supply, signal, or each other), because they are reserved and must be left unconnected.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set DSP operating modes. During reset, the DSP samples the strap option pins. Strap pins have an approximately 100 kΩ pull-down for the default value. If a strap pin is not connected to an external pull-up or logic load, the DSP samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up. In a multiprocessor system, up to eight DSPs may be connected on the cluster bus, resulting in parallel combination of strap pin pull-down resistors. Table 16 lists and describes each of the DSP's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	On Pin …	Description
EBOOT	$\overline{BMS}$	EPROM boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot DSP through the external port or a link port
IRQEN	$\overline{BM}$	Interrupt Enable. 0 = disable and set $\overline{IRQ3–0}$ interrupts to level sensitive after reset (default) 1 = enable and set $\overline{IRQ3–0}$ interrupts to edge sensitive immediately after reset
TM1	L2DIR	Test Mode 1. 0 = required setting during reset. 1 = reserved.
TM2	TMR0E	Test Mode 2. 0 = required setting during reset. 1 = reserved.

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{DD}	Internal Supply Voltage		1.14		1.26	V
V_{DD_A}	Analog Supply Voltage		1.14		1.26	V
V_{DD_IO}	I/O Supply Voltage		3.15		3.45	V
T_{CASE}	Case Operating Temperature		–40		+85	°C
V_{IH}	High Level Input Voltage[1]	@ V_{DD}, V_{DD_IO} = max	2		V_{DD_IO} + 0.5	V
V_{IL}	Low Level Input Voltage[1]	@ V_{DD}, V_{DD_IO} = min	–0.5		+0.8	V
I_{DD}	V_{DD} Supply Current for Typical Activity[2]	@ CCLK = 250 MHz, V_{DD} = 1.25 V, T_{CASE} = 25°C		1.2		A
I_{DD}	V_{DD} Supply Current for Typical Activity[2]	@ CCLK = 300 MHz, V_{DD} = 1.25 V, T_{CASE} = 25°C		1.5		A
$I_{DDIDLELP}$	V_{DD} Supply Current for IDLELP Instruction Execution	@ CCLK = 300 MHz, V_{DD} = 1.20 V, T_{CASE} = 25°C		173		mA
I_{DD_IO}	V_{DD_IO} Supply Current for Typical Activity[2]	@ SCLK = 100 MHz, V_{DD_IO} = 3.3 V, T_{CASE} = 25°C		137		mA
I_{DD_A}	V_{DD_A} Supply Current	@ V_{DD} = 1.25 V, T_{CASE} = 25°C		25	31.25	mA
V_{REF}	Voltage Reference		1.4		1.6	V

[1] Applies to input and bidirectional pins.
[2] For details on internal and external power estimation, including: power vector definitions, current usage descriptions, and formulas, see *EE-169, Estimating Power for the ADSP-TS101S* on the Analog Devices website—use site search on "EE-169" (www.analog.com). This document is updated regularly to keep pace with silicon revisions.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@V_{DD_IO} = min, I_{OH} = –2 mA	2.4		V
V_{OL}	Low Level Output Voltage[1]	@V_{DD_IO} = min, I_{OL} = 4 mA		0.4	V
I_{IH}	High Level Input Current[2]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max		10	µA
I_{IHP}	High Level Input Current (pd)[2]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max	17.2	44.5	µA
I_{IL}	Low Level Input Current[3]	@V_{DD_IO} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current (pu)[4]	@V_{DD_IO} = max, V_{IN} = 0 V	–69	–23	µA
I_{OZH}	Three-State Leakage Current High[5, 6]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max		10	µA
I_{OZHP}	Three-State Leakage Current High (pd)[7]	@V_{DD_IO} = max, V_{IN} = V_{DD_IO} max	17.2	44.5	µA
I_{OZL}	Three-State Leakage Current Low[8]	@V_{DD_IO} = max, V_{IN} = 0 V		10	µA
I_{OZLP}	Three-State Leakage Current Low (pu)[9]	@V_{DD_IO} = max, V_{IN} = 0 V	–69	–23	µA
I_{OZLO}	Three-State Leakage Current Low (od)[7]	@V_{DD_IO} = max, V_{IN} = 0 V	–9.8	–4.6	mA
C_{IN}	Input Capacitance[10, 11]	@f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		5	pF

[1] Applies to output and bidirectional pins.
[2] Applies to input pins with internal pull-downs (pd).
[3] Applies to input pins without internal pull-ups (pu).
[4] Applies to input pins with internal pull-ups (pu).
[5] Applies to three-stateable pins without internal pull-downs (pd).
[6] Applies to open drain (od) pins with 500 Ω pull-ups (pu).
[7] Applies to three-stateable pins with internal pull-downs (pd).
[8] Applies to three-stateable pins without internal pull-ups (pu).
[9] Applies to three-stateable pins with internal pull-ups (pu).
[10] Applies to all signals.
[11] Guaranteed but not tested.

Table 25. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{START_LO}	$\overline{RESET}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, SCLK/LCLK, and Static/Strap Pins Are Stable and Within Specification	2		ms
t_{PULSE1_HI}	$\overline{RESET}$ Deasserted for First Pulse	$50 \times t_{SCLK}$	$100 \times t_{SCLK}$	ns
t_{PULSE2_LO}	$\overline{RESET}$ Asserted for Second Pulse	$100 \times t_{SCLK}$		ns
t_{TRST_PWR}[1]	$\overline{TRST}$ Asserted During Power-Up Reset	$2 \times t_{SCLK}$		ns

[1] Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, and SCLK/LCLK and static/strap pins are stable and within specification, and before $\overline{RESET}$ is deasserted.

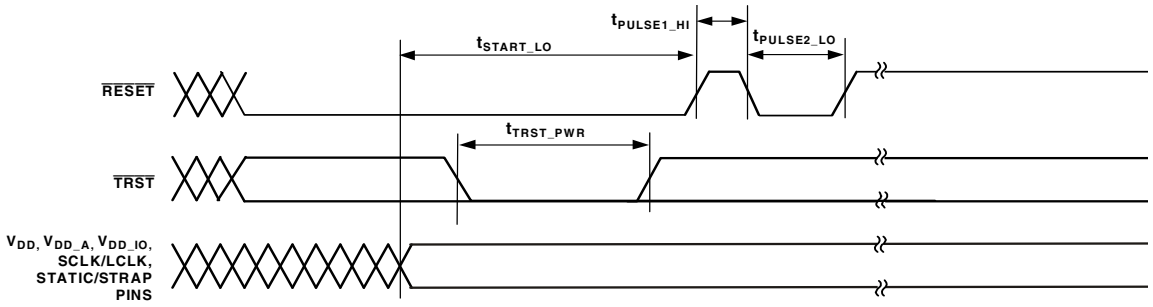

Figure 14. Power-Up Reset Timing

Table 26. Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RST_IN}	$\overline{RESET}$ Asserted	$100 \times t_{SCLK}$		ns
t_{STRAP}	$\overline{RESET}$ Deasserted After Strap Pins Stable	2		ms

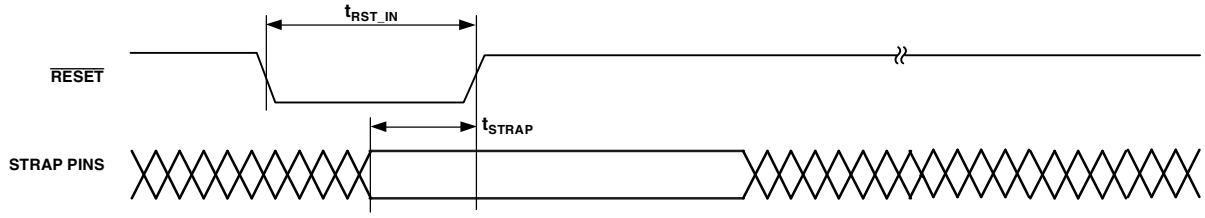

Figure 15. Normal Reset (Hot Reset) Timing

Table 28. AC Signal Specifications (for 16.7 ns <SCLK <25 ns) (All values in this table are in nanoseconds) (Continued)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	0.8			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

[1] The output valid (max) value in this column applies for the standard 30 pF capacitive load used in testing. To see how output valid varies with capacitive loading, see Figure 40 on Page 36.

[2] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.

[3] $\overline{\text{CPA}}$ and $\overline{\text{DPA}}$ pins are open drains and have 0.5 kΩ internal pull-ups.

[4] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference. These synchronous specifications only apply for recognition in the current clock reference cycle.

[5] This pin is a strap option. During reset, an internal resistor pulls the pin low.

[6] For input specifications, see Table 21.

[7] For additional requirement details, see Reset and Booting on Page 9.

[8] TCK_FE indicates TCK falling edge.

[9] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.

[10] Reference clock depends on function.

[11] System inputs are: $\overline{\text{IRQ3–0}}$, $\overline{\text{BMS}}$, LCLKRAT2–0, SCLKFREQ, $\overline{\text{BM}}$, TMR0E, FLAG3–0, ID2–0, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, $\overline{\text{BOFF}}$, $\overline{\text{HBR}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKIN, L0DAT7–0, L1CLKIN, L1DAT7–0, L2CLKIN, L2DAT7–0, L2DIR, L3CLKIN, L3DAT7–0, DS2–0, CONTROLIMP2–0, $\overline{\text{RESET}}$, $\overline{\text{DMAR3–0}}$.

[12] System outputs are: $\overline{\text{BMS}}$, $\overline{\text{BM}}$, $\overline{\text{BUSLOCK}}$, TMR0E, FLAG3–0, $\overline{\text{FLYBY}}$, $\overline{\text{IOEN}}$, $\overline{\text{MSH}}$, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MS1–0}}$, HDQM, LDQM, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKOUT, L0DAT7–0, L0DIR, L1CLKOUT, L1DAT7–0, L1DIR, L2CLKOUT, L2DAT7–0, L2DIR, L3CLKOUT, L3DAT7–0, L3DIR, $\overline{\text{EMU}}$.

Link Ports Data Transfer and Token Switch Timing

Table 31, Table 32, Table 33, and Table 34 with Figure 17, Figure 18, Figure 19, and Figure 20 provide the timing specifications for the link ports data transfer and token switch.

Table 29. Link Ports—Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{CONNS}[1]	Connectivity Pulse Setup	$2 \times t_{CCLK} + 3.5$		ns
t_{CONNS}[2]	Connectivity Pulse Setup	8		ns
t_{CONNIW}[3]	Connectivity Pulse Input Width	$t_{LxCLK\_Tx} + 1$		ns
t_{ACKS}	Acknowledge Setup	$0.5 \times t_{LxCLK\_Tx}$		ns
Switching Characteristics				
t_{LxCLK_Tx}[4]	Transmit Link Clock Period	$0.9 \times LR \times t_{CCLK}$	$1.1 \times LR \times t_{CCLK}$	ns
t_{LxCLKH_Tx}[1]	Transmit Link Clock Width High	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKH_Tx}[2]	Transmit Link Clock Width High	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[1]	Transmit Link Clock Width Low	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[2]	Transmit Link Clock Width Low	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{DIRS}	LxDIR Transmit Setup	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DIRH}	LxDIR Transmit Hold	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DOS}[1]	LxDAT7–0 Output Setup	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[1]	LxDAT7–0 Output Hold	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOS}[2]	LxDAT7–0 Output Setup	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[2]	LxDAT7–0 Output Hold	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{LDOE}	LxDAT7–0 Output Enable	1		ns
t_{LDOD}[5]	LxDAT7–0 Output Disable	1		ns

[1] The formula for this parameter applies when LR is 2.
[2] The formula for this parameter applies when LR is 3, 4, or 8.
[3] LxCLKIN shows the connectivity pulse with each of the three possible transitions to "Acknowledge." After a connectivity pulse low minimum, LxCLKIN may [1] return high and remain high for "Acknowledge," [2] return high and subsequently go low (meeting t_{ACKS}) for "Not Acknowledge," or [3] remain low for "Not Acknowledge."
[4] The Link clock Ratio (LR) is 2, 3, 4, or 8 as set by the SPD bits in the LCTLx register. The maximum LxCLK is 125 MHz. LR = 2 may not be used when CCLK ≥ 250 MHz.
[5] This specification applies to the last data byte or the "Dummy" byte that follows the verification byte if enabled. For more information, see the *ADSP-TS101* TigerSHARC *Processor Hardware Reference*.

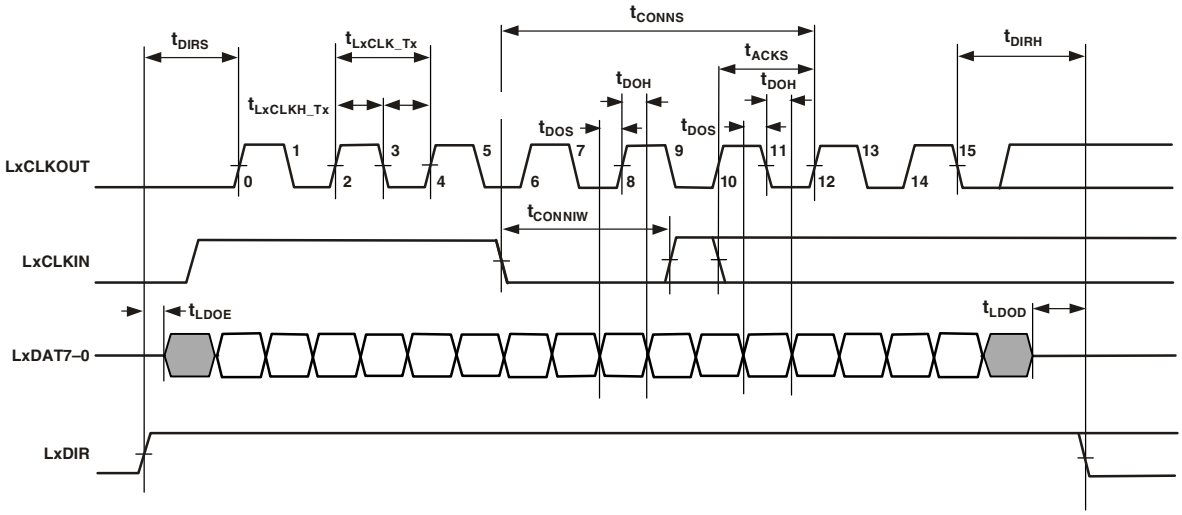

Figure 17. Link Ports—Transmit

TEST CONDITIONS

The test conditions for timing parameters appearing in Table 29 on Page 29 and Table 30 on Page 30 include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 29.

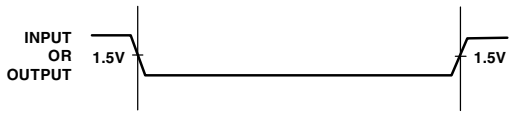

Figure 29. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

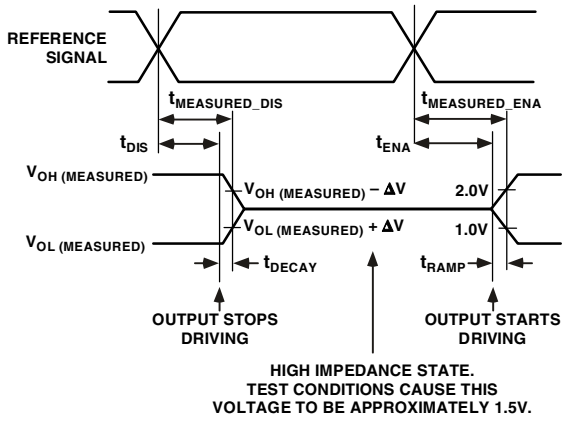

Figure 30. Output Enable/Disable

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED\_DIS}$ and t_{DECAY} as shown in Figure 30. The time $t_{MEASURED\_DIS}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. The t_{DECAY} value is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The time for the voltage on the bus to ramp by ΔV is dependent on the capacitive load, C_L, and the drive current, I_D. This ramp time can be approximated by the following equation:

$$t_{RAMP} = \frac{C_L \Delta V}{I_D}$$

The output enable time t_{ENA} is the difference between $t_{MEASURED\_ENA}$ and t_{RAMP} as shown in Figure 30. The time $t_{MEASURED\_ENA}$ is the interval from when the reference signal switches to when the output voltage ramps ΔV from the measured three-stated output level. The t_{RAMP} value is calculated with test load C_L, drive current I_D, and with ΔV equal to 0.5 V.

Capacitive Loading

Figure 31 shows the circuit with variable capacitance that is used for measuring typical output rise and fall times. Figure 32 through Figure 39 show how output rise time varies with capacitance. Figure 40 graphically shows how output valid varies with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 34.) The graphs of Figure 32 through Figure 40 may not be linear outside the ranges shown.

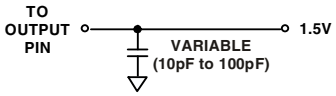

Figure 31. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

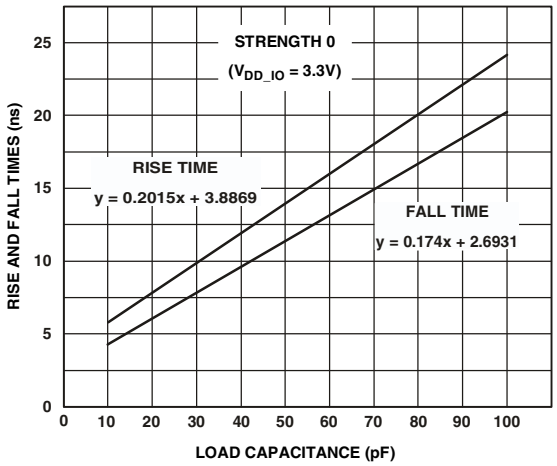

Figure 32. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 0

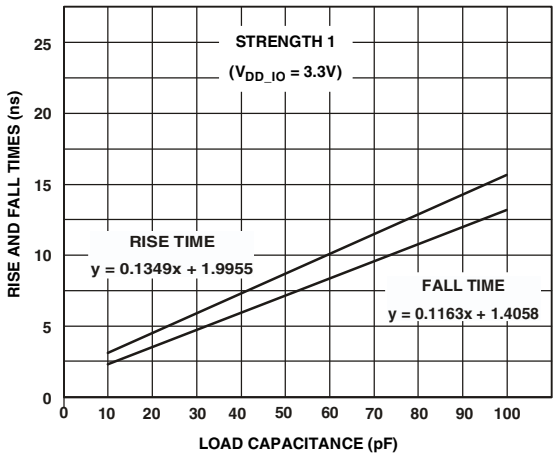

Figure 33. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 1

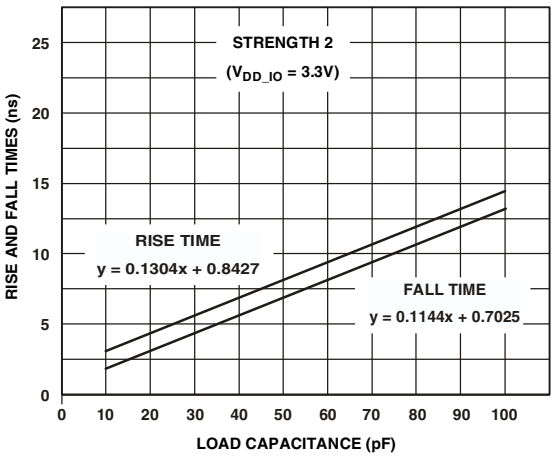

Figure 34. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 2

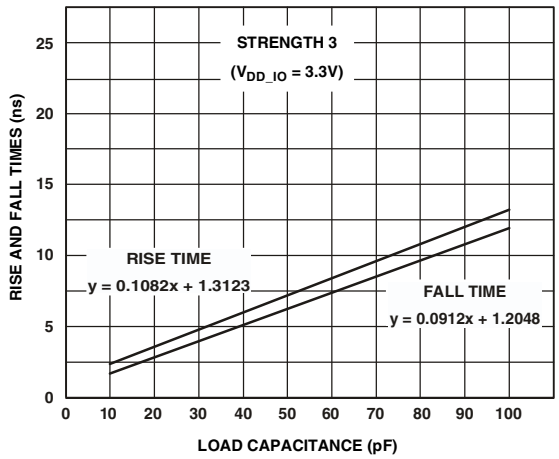

Figure 35. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 3

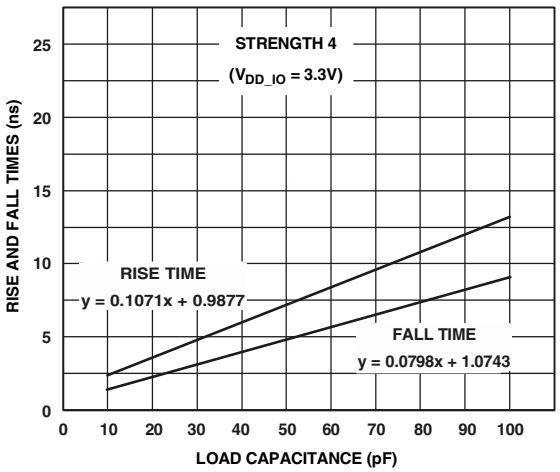

Figure 36. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 4

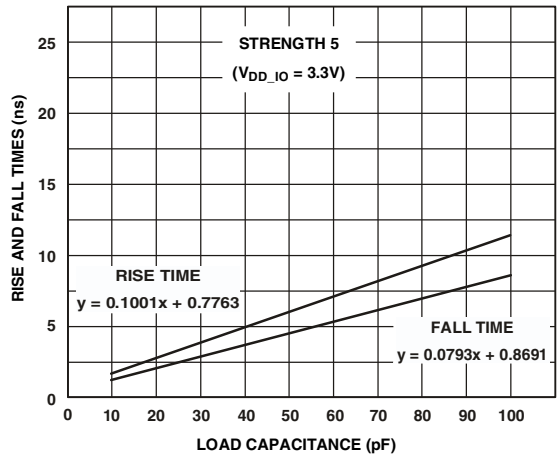

Figure 37. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 5

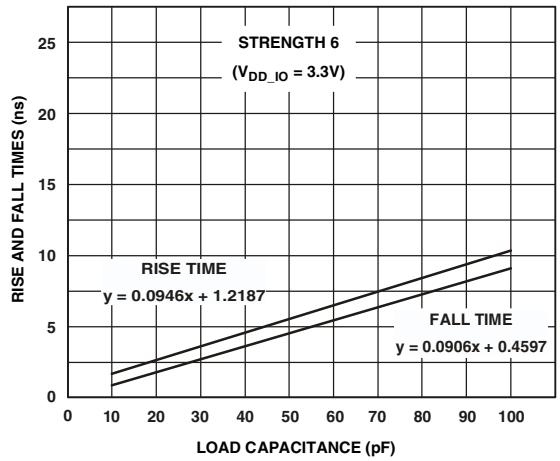

Figure 38. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 6

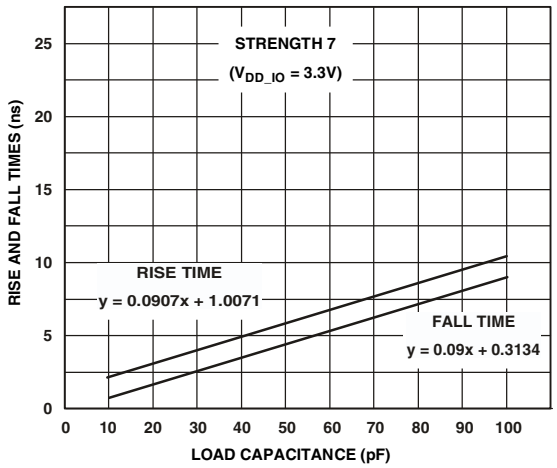

Figure 39. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 7

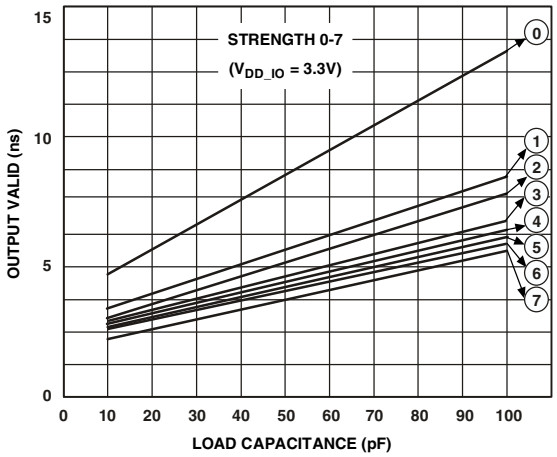

Figure 40. Typical Output Valid (V_{DD_IO} = 3.3 V) vs. Load Capacitance at Max Case Temperature and Strength 0–7[1]

[1] The line equations for the output valid vs. load capacitance are:
Strength 0: y = 0.0956x + 3.5662
Strength 1: y = 0.0523x + 3.2144
Strength 2: y = 0.0433x + 3.1319
Strength 3: y = 0.0391x + 2.9675
Strength 4: y = 0.0393x + 2.7653
Strength 5: y = 0.0373x + 2.6515
Strength 6: y = 0.0379x + 2.1206
Strength 7: y = 0.0399x + 1.9080

ENVIRONMENTAL CONDITIONS

The ADSP-TS101S is rated for performance over the extended commercial temperature range, T_{CASE} = –40°C to +85°C.

Thermal Characteristics

The ADSP-TS101S is packaged in a 19 mm × 19 mm and 27 mm × 27 mm Plastic Ball Grid Array (PBGA). The ADSP-TS101S is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heat sink and/or an air flow source may be used. See Table 33 and Table 34 for thermal data.

Table 33. Thermal Characteristics for 19 mm × 19 mm Package

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow[2] = 0 m/s	16.6	°C/W
	Airflow[3] = 1 m/s	14.0	°C/W
	Airflow[3] = 2 m/s	12.9	°C/W
θ_{JC}		6.7	°C/W
θ_{JB}		5.8	°C/W

[1] Determination of parameter is system dependent and is based on a number of factors, including device power dissipation, package thermal resistance, board thermal characteristics, ambient temperature, and air flow.
[2] Per JEDEC JESD51-2 procedure using a four layer board (compliant with JEDEC JESD51-9).
[3] Per SEMI Test Method G38-87 using a four layer board (compliant with JEDEC JESD51-9).

Table 34. Thermal Characteristics for 27 mm × 27 mm Package

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow[2] = 0 m/s	13.8	°C/W
	Airflow[3] = 1 m/s	11.7	°C/W
	Airflow[3] = 2 m/s	10.8	°C/W
θ_{JC}		3.1	°C/W
θ_{JB}		5.9	°C/W

[1] Determination of parameter is system dependent and is based on a number of factors, including device power dissipation, package thermal resistance, board thermal characteristics, ambient temperature, and air flow.
[2] Per JEDEC JESD51-2 procedure using a four layer board (compliant with JEDEC JESD51-9).
[3] Per SEMI Test Method G38-87 using a four layer board (compliant with JEDEC JESD51-9).

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
A1	V_{SS}	B1	V_{SS}	C1	V_{SS}	D1	V_{SS}	E1	DATA23
A2	DATA17	B2	V_{SS}	C2	DATA20	D2	V_{SS}	E2	DATA22
A3	DATA14	B3	DATA16	C3	DATA21	D3	DATA19	E3	V_{SS}
A4	DATA11	B4	DATA13	C4	DATA18	D4	V_{DD_IO}	E4	V_{DD_IO}
A5	DATA9	B5	DATA12	C5	DATA15	D5	V_{DD_IO}	E5	V_{DD_IO}
A6	DATA7	B6	DATA10	C6	DATA8	D6	V_{DD_IO}	E6	V_{DD}
A7	DATA4	B7	DATA5	C7	DATA6	D7	V_{DD_IO}	E7	V_{DD}
A8	DATA1	B8	DATA2	C8	DATA3	D8	V_{DD_IO}	E8	V_{DD_IO}
A9	L0DIR	B9	NC	C9	DATA0	D9	V_{DD_IO}	E9	V_{DD_IO}
A10	L0DAT7	B10	L0CLKOUT	C10	L0CLKIN	D10	V_{DD_IO}	E10	V_{DD}
A11	L0DAT4	B11	L0DAT5	C11	L0DAT6	D11	V_{DD_IO}	E11	V_{DD}
A12	L0DAT1	B12	L0DAT2	C12	L0DAT3	D12	V_{DD_IO}	E12	V_{DD_IO}
A13	LCLK_N	B13	V_{SS}	C13	L0DAT0	D13	V_{DD_IO}	E13	V_{DD_IO}
A14	LCLK_P	B14	V_{SS}	C14	V_{SS_A}	D14	V_{DD_IO}	E14	V_{DD}
A15	V_{DD_A}	B15	V_{SS_A}	C15	V_{DD_A}	D15	V_{DD_IO}	E15	V_{DD}
A16	SCLK_N	B16	SCLK_P	C16	V_{SS}	D16	V_{DD_IO}	E16	V_{DD_IO}
A17	V_{REF}	B17	V_{SS}	C17	DS0	D17	V_{DD_IO}	E17	V_{DD_IO}
A18	DS1	B18	DS2	C18	CONTROLIMP0	D18	V_{DD_IO}	E18	V_{DD}
A19	CONTROLIMP2	B19	CONTROLIMP1	C19	$\overline{\text{DMAR1}}$	D19	V_{DD_IO}	E19	V_{DD}
A20	$\overline{\text{RESET}}$	B20	$\overline{\text{DMAR3}}$	C20	TDI	D20	V_{DD_IO}	E20	V_{DD_IO}
A21	$\overline{\text{DMAR2}}$	B21	$\overline{\text{DMAR0}}$	C21	$\overline{\text{IRQ2}}$	D21	V_{DD_IO}	E21	V_{DD_IO}
A22	$\overline{\text{EMU}}$	B22	$\overline{\text{IRQ3}}$	C22	LCLKRAT0	D22	V_{DD_IO}	E22	V_{DD_IO}
A23	$\overline{\text{TRST}}$	B23	TCK	C23	LCLKRAT1	D23	$\overline{\text{BMS}}$	E23	V_{SS}
A24	TMS	B24	$\overline{\text{IRQ1}}$	C24	$\overline{\text{IRQ0}}$	D24	V_{SS}	E24	SCLKFREQ
A25	V_{SS}	B25	TDO	C25	V_{SS}	D25	V_{SS}	E25	LCLKRAT2
F1	DATA26	G1	DATA29	H1	L3DAT0	J1	L3DAT3	K1	L3DAT6
F2	DATA25	G2	DATA28	H2	DATA31	J2	L3DAT2	K2	L3DAT5
F3	DATA24	G3	DATA27	H3	DATA30	J3	L3DAT1	K3	L3DAT4
F4	V_{DD_IO}	G4	V_{DD_IO}	H4	V_{DD_IO}	J4	V_{DD_IO}	K4	V_{DD_IO}
F5	V_{DD_IO}	G5	V_{DD}	H5	V_{DD}	J5	V_{DD_IO}	K5	V_{DD_IO}
F6	V_{DD}	G6	V_{DD}	H6	V_{DD}	J6	V_{DD}	K6	V_{DD}
F7	V_{DD}	G7	V_{SS}	H7	V_{SS}	J7	V_{SS}	K7	V_{SS}
F8	V_{DD}	G8	V_{SS}	H8	V_{SS}	J8	V_{SS}	K8	V_{SS}
F9	V_{DD}	G9	V_{SS}	H9	V_{SS}	J9	V_{SS}	K9	V_{SS}
F10	V_{DD}	G10	V_{SS}	H10	V_{SS}	J10	V_{SS}	K10	V_{SS}
F11	V_{DD}	G11	V_{SS}	H11	V_{SS}	J11	V_{SS}	K11	V_{SS}
F12	V_{DD}	G12	V_{SS}	H12	V_{SS}	J12	V_{SS}	K12	V_{SS}
F13	V_{DD}	G13	V_{SS}	H13	V_{SS}	J13	V_{SS}	K13	V_{SS}
F14	V_{DD}	G14	V_{SS}	H14	V_{SS}	J14	V_{SS}	K14	V_{SS}
F15	V_{DD}	G15	V_{SS}	H15	V_{SS}	J15	V_{SS}	K15	V_{SS}
F16	V_{DD}	G16	V_{SS}	H16	V_{SS}	J16	V_{SS}	K16	V_{SS}
F17	V_{DD}	G17	V_{SS}	H17	V_{SS}	J17	V_{SS}	K17	V_{SS}
F18	V_{DD}	G18	V_{SS}	H18	V_{SS}	J18	V_{SS}	K18	V_{SS}
F19	V_{DD}	G19	V_{SS}	H19	V_{SS}	J19	V_{SS}	K19	V_{SS}
F20	V_{DD}	G20	V_{DD}	H20	V_{DD}	J20	V_{DD}	K20	V_{DD}
F21	V_{DD}	G21	V_{DD}	H21	V_{DD_IO}	J21	V_{DD_IO}	K21	V_{DD}
F22	V_{DD_IO}	G22	V_{DD_IO}	H22	V_{DD_IO}	J22	V_{DD_IO}	K22	V_{DD_IO}
F23	$\overline{\text{BM}}$	G23	FLAG3	H23	FLAG0	J23	ID0	K23	NC
F24	$\overline{\text{BUSLOCK}}$	G24	FLAG2	H24	ID2	J24	NC	K24	NC
F25	TMR0E	G25	FLAG1	H25	ID1	J25	NC	K25	NC

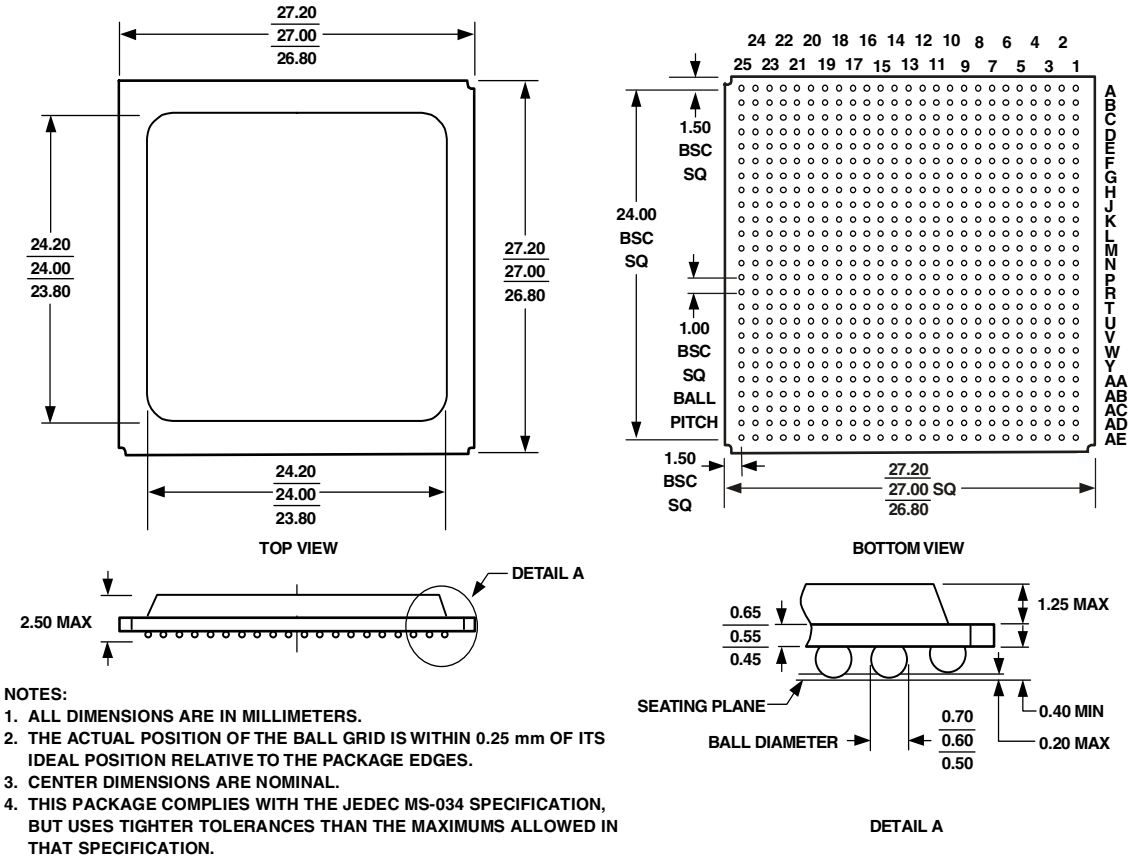

Figure 44. 625-Ball PBGA (B-625)

SURFACE-MOUNT DESIGN

The following table is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
625-ball (27 mm) PBGA	Solder Mask Defined (SMD)	0.45 mm diameter	0.60 mm diameter
484-ball (19 mm) PBGA	Solder Mask Defined (SMD)	0.40 mm diameter	0.53 mm diameter

ORDERING GUIDE

Part Number[1, 2, 3, 4]	Temperature Range (Case)	Core Clock (CCLK) Rate[5]	On-Chip SRAM	Package Description	Package Option
ADSP-TS101SAB1-000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1-100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z000	–40°C to +85°C	250 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB1Z100	–40°C to +85°C	300 MHz	6M Bit	625-Ball Plastic Ball Grid Array (PBGA)	B-625[6]
ADSP-TS101SAB2-000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2-100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z000	–40°C to +85°C	250 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]
ADSP-TS101SAB2Z100	–40°C to +85°C	300 MHz	6M Bit	484-Ball Plastic Ball Grid Array (PBGA)	B-484[7]

[1] S indicates 1.2 V and 3.3 V supplies.
[2] A indicates –40°C to +85°C temperature.
[3] 000 indicates 250 MHz speed grade; 100 indicates 300 MHz speed grade.
[4] Z indicates RoHS compliant part.
[5] The instruction rate runs at the internal DSP clock (CCLK) rate.
[6] The B-625 package measures 27 mm × 27 mm.
[7] The B-484 package measures 19 mm × 19 mm.