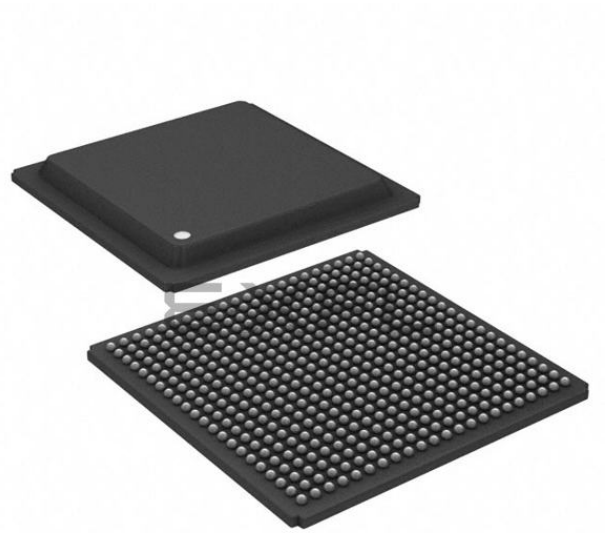

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	768kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	484-BFBGA
Supplier Device Package	484-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts101sab2z100

Data Sheet

- ADSP-TS101S: TigerSHARC Embedded Processor, 300 MHz, 6 Mbits, Data Sheet

Evaluation Kit Manuals

- ADSP-TS101S EZ-KIT Lite® Manual

Integrated Circuit Anomalies

- ADSP-TS101S TigerSHARC Anomaly List for Revision(s) 0.2, 0.4

Processor Manuals

- ADSP-TS101 TigerSHARC Processor Hardware Reference
- ADSP-TS101 TigerSHARC Processor Programming Reference
- TigerSHARC Processors: Manuals

Product Highlight

- General-Purpose TigerSHARC Processor Product Brief

Software Manuals

- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for TigerSHARC Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- TigerSHARC Evaluation Kits

TOOLS AND SIMULATIONS

- ADSP-TS101 TigerSHARC BSDL File 19x19mm PBGA Package for Revision 0.4, (11/2006)
- ADSP-TS101 TigerSHARC BSDL File 27x27mm PBGA Package for Revision 0.4, (11/2006)
- ADSP-TS101: 19x19mm PBGA Silicon Revision 0.0 and 0.1 [BSDL Original File], 02/08/2001
- ADSP-TS101: 19x19mm PBGA Package Silicon Revision 0.2, [BSDL Original File], 09/09/2003
- ADSP-TS101: 27x27 PBGA Package Siicon Revision 0.2, [BSDL Original File], 09/09/2003
- ADSP-TS101: 27x27 PBGA Package Silicon Revision 0.0 and 0.1 [BSDL Original File], 10/12/2001
- Designing with BGA
- TigerSHARC Processors: Software and Tools
- ADSP-TS101S IBIS Datafile BGA Package

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- A Software Solution for Chip Rate Processing in CDMA Wireless Infrastructure
- ADSP-TS101S MP System Simulation and Analysis
- Continuous Real-Time Signal Processing -- Comparing TigerSHARC and PowerPC Via Continuous cFFTs
- Rethinking Base Station, Baseband Processing for Wireless Communication
- SHARC Bites Back - The Memory Inside: TigerSHARC Swallows Its DRAM

White Papers

- ADSP-TS101S MP System Simulation and Analysis

DESIGN RESOURCES

- ADSP-TS101S Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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The ADSP-TS101S, in most cases, has a two-cycle arithmetic execution pipeline that is fully interlocked, so whenever a computation result is unavailable for another operation dependent on it, the DSP automatically inserts one or more stall cycles as needed. Efficient programming with dependency-free instructions can eliminate most computational and memory transfer data dependencies.

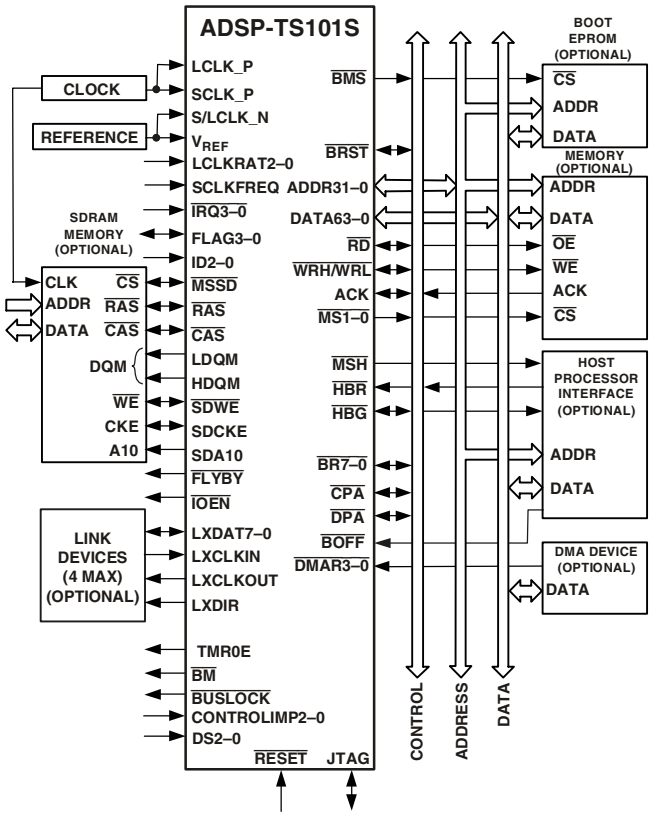

Figure 2. Single-Processor System with External SDRAM

In addition, the ADSP-TS101S supports SIMD operations two ways—SIMD compute blocks and SIMD computations. The programmer can direct both compute blocks to operate on the same data (broadcast distribution) or on different data (merged distribution). In addition, each compute block can execute four 16-bit or eight 8-bit SIMD computations in parallel.

DUAL COMPUTE BLOCKS

The ADSP-TS101S has compute blocks that can execute computations either independently or together as a SIMD engine. The DSP can issue up to two compute instructions per compute block each cycle, instructing the ALU, multiplier, or shifter to perform independent, simultaneous operations.

The compute blocks are referred to as X and Y in assembly syntax, and each block contains three computational units—an ALU, a multiplier, a 64-bit shifter, and a 32-word register file.

- Register file—each compute block has a multiported 32-word, fully orthogonal register file used for transferring data between the computation units and data buses and for storing intermediate results. Instructions can access the registers in the register file individually (word aligned), or in sets of two (dual aligned) or four (quad aligned).
- ALU—the ALU performs a standard set of arithmetic operations in both fixed- and floating-point formats. It also performs logic operations.
- Multiplier—the multiplier performs both fixed- and floating-point multiplication and fixed-point multiply and accumulate.
- Shifter—the 64-bit shifter performs logical and arithmetic shifts, bit and bit stream manipulation, and field deposit and extraction operations.
- Accelerator—128-bit unit for trellis decoding (for example, Viterbi and turbo decoders) and complex correlations for communication applications.

Using these features, the compute blocks can:

- Provide 8 MACs per cycle peak and 7.1 MACs per cycle sustained 16-bit performance and provide 2 MACs per cycle peak and 1.8 MACs per cycle sustained 32-bit performance (based on FIR)
- Execute six single-precision, floating-point or execute 24 fixed-point (16-bit) operations per cycle, providing 1,800 MFLOPS or 7.3 GOPS performance
- Perform two complex 16-bit MACs per cycle
- Execute eight trellis butterflies in one cycle

DATA ALIGNMENT BUFFER (DAB)

The DAB is a quad word FIFO that enables loading of quad word data from nonaligned addresses. Normally, load instructions must be aligned to their data size so that quad words are loaded from a quad-aligned address. Using the DAB significantly improves the efficiency of some applications, such as FIR filters.

DUAL INTEGER ALUS (IALUS)

The ADSP-TS101S has two IALUs that provide powerful address generation capabilities and perform many general-purpose integer operations. Each of the IALUs:

- Provides memory addresses for data and update pointers
- Supports circular buffering and bit-reverse addressing
- Performs general-purpose integer operations, increasing programming flexibility
- Includes a 31-word register file for each IALU

As address generators, the IALUs perform immediate or indirect (pre- and post-modify) addressing. They perform modulus and bit-reverse operations with no constraints placed on memory addresses for the modulus data buffer placement. Each IALU can specify either a single, dual, or quad word access from memory.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ integrated development and debugging environment (IDDE) lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the TigerSHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command-line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command-line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

Use the Expert Linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the DSP or external memory with a drag of the mouse, examine run-time stack and heap usage. The Expert Linker is fully compatible with existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices DSP emulators use the IEEE 1149.1 JTAG Test Access Port of the ADSP-TS101S processor to monitor and control the target board processor during emulation. The emulator provides full speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the TigerSHARC processor family. Hardware tools include TigerSHARC processor PC plug-in cards. Third-party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

DESIGNING AN EMULATOR-COMPATIBLE DSP BOARD (TARGET)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG DSP. The emulator uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-TS101S processor's architecture and functionality. For detailed information on the ADSP-TS101S processor's core architecture and instruction set, see the *ADSP-TS101 TigerSHARC Processor Programming Reference* and the *ADSP-TS101 TigerSHARC Processor Hardware Reference*. For detailed information on the development tools for this processor, see the *VisualDSP++ User's Guide*.

PIN FUNCTION DESCRIPTIONS

While most of the ADSP-TS101S processor's input pins are normally synchronous—tied to a specific clock—a few are asynchronous. For these asynchronous signals, an on-chip synchronization circuit prevents metastability problems. The synchronous ac specification for asynchronous signals is used only when predictable cycle-by-cycle behavior is required.

All inputs are sampled by a clock reference, therefore input specifications (asynchronous minimum pulse widths or synchronous input setup and hold) must be met to guarantee recognition.

PIN STATES AT RESET

The output pins can be three-stated during normal operation. The DSP three-states all outputs during reset, allowing these pins to get to their internal pull-up or pull-down state. Some output pins (control signals) have a pull-up or pull-down that maintains a known value during transitions between different drivers.

PIN DEFINITIONS

The Type column in the following pin definitions tables describes the pin type, when the pin is used in the system. The Term (for termination) column describes the pin termination type if the pin is not used by the system. Note that some pins are always used (indicated with au symbol).

Table 3. Pin Definitions—Clocks and Reset

Signal	Type	Term	Description
LCLK_N	I	au	Local Clock Reference. Connect this pin to V_{REF} as shown in Figure 6.
LCLK_P	I	au	Local Clock Input. DSP clock input. The instruction cycle rate = n × LCLK, where n is user-programmable to 2, 2.5, 3, 3.5, 4, 5, or 6. For more information, see Clock Domains on Page 9.
LCLKRAT2–0[1]	I (pd[2])	au	LCLK Ratio. The DSP's core clock (instruction cycle rate) = n × LCLK, where n is user-programmable to 2, 2.5, 3, 3.5, 4, 5, or 6 as shown in Table 4. These pins must have a constant value while the DSP is powered.
SCLK_N	I	au	System Clock Reference. Connect this pin to V_{REF} as shown in Figure 6.
SCLK_P	I	au	System Clock Input. The DSP's system input clock for cluster bus. This pin must be connected to the same clock source as LCLK_P. For more information, see Clock Domains on Page 9.
SCLKFREQ[3]	I (pu[2])	au	SCLK Frequency. SCLKFREQ = 1 is required. The SCLKFREQ pin must have a constant value while the DSP is powered.
$\overline{\text{RESET}}$	I/A	au	Reset. Sets the DSP to a known state and causes program to be in idle state. $\overline{\text{RESET}}$ must be asserted at specified time according to the type of reset operation. For details, see Reset and Booting on Page 9.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

[1] The internal pull-down may not be sufficient. A stronger pull-down may be necessary.
[2] See Electrical Characteristics on Page 20 for maximum and minimum current consumption for pull-up and pull-down resistances.
[3] The internal pull-up may not be sufficient. A stronger pull-up may be necessary.

Table 4. LCLK Ratio

LCLKRAT2–0	Ratio
000 (default)	2
001	2.5
010	3
011	3.5
100	4
101	5
110	6
111	Reserved

Table 5. Pin Definitions—External Port Bus Controls

Signal	Type	Term	Description
ADDR31–0[1]	I/O/T	nc	Address Bus. The DSP issues addresses for accessing memory and peripherals on these pins. In a multiprocessor system, the bus master drives addresses for accessing internal memory or I/O processor registers of other ADSP-TS101S processors. The DSP inputs addresses when a host or another DSP accesses its internal memory or I/O processor registers.
DATA63–0[1]	I/O/T	nc	External Data Bus. Data and instructions are received, and driven by the DSP, on these pins.
$\overline{RD}$[2]	I/O/T (pu[3])	nc	Memory Read. $\overline{RD}$ is asserted whenever the DSP reads from any slave in the system, excluding SDRAM. When the DSP is a slave, $\overline{RD}$ is an input and indicates read transactions that access its internal memory or universal registers. In a multiprocessor system, the bus master drives $\overline{RD}$. The $\overline{RD}$ pin changes concurrently with ADDR pins.
$\overline{WRL}$[2]	I/O/T (pu[3])	nc	Write Low. $\overline{WRL}$ is asserted in two cases: When the ADSP-TS101S writes to an even address word of external memory or to another external bus agent; and when the ADSP-TS101S writes to a 32-bit zone (host, memory, or DSP programmed to 32-bit bus). An external master (host or DSP) asserts $\overline{WRL}$ for writing to a DSP's low word of internal memory. In a multiprocessor system, the bus master drives $\overline{WRL}$. The $\overline{WRL}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRL}$ is an input and indicates write transactions that access its internal memory or universal registers.
$\overline{WRH}$[2]	I/O/T (pu[3])	nc	Write High. $\overline{WRH}$ is asserted when the ADSP-TS101S writes a long word (64 bits) or writes to an odd address word of external memory or to another external bus agent on a 64-bit data bus. An external master (host or another DSP) must assert $\overline{WRH}$ for writing to a DSP's high word of 64-bit data bus. In a multiprocessing system, the bus master drives $\overline{WRH}$. The $\overline{WRH}$ pin changes concurrently with ADDR pins. When the DSP is a slave, $\overline{WRH}$ is an input and indicates write transactions that access its internal memory or universal registers.
ACK	I/O/T	epu	Acknowledge. External slave devices can deassert ACK to add wait states to external memory accesses. ACK is used by I/O devices, memory controllers, and other peripherals on the data phase. The DSP can deassert ACK to add wait states to read accesses of its internal memory. The ADSP-TS101S does not drive ACK during slave writes. Therefore, an external (approximately 10 kΩ) pull-up is required.
$\overline{BMS}$[2, 4]	O/T (pu/pd[3])	au	Boot Memory Select. $\overline{BMS}$ is the chip select for boot EPROM or flash memory. During reset, the DSP uses $\overline{BMS}$ as a strap pin (EBOOT) for EPROM boot mode. When the DSP is configured to boot from EPROM, $\overline{BMS}$ is active during the boot sequence. Pull-down enabled during $\overline{RESET}$ (asserted); pull-up enabled after $\overline{RESET}$ (deasserted). In a multiprocessor system, the DSP bus master drives $\overline{BMS}$. For details see Reset and Booting on Page 9 and the EBOOT signal description in Table 16 on Page 19.
$\overline{MS1–0}$[2]	O/T (pu[3])	nc	Memory Select. $\overline{MS0}$ or $\overline{MS1}$ is asserted whenever the DSP accesses memory banks 0 or 1, respectively. $\overline{MS1–0}$ are decoded memory address pins that change concurrently with ADDR pins. When ADDR31:26 = 0b000010, $\overline{MS0}$ is asserted. When ADDR31:26 = 0b000011, $\overline{MS1}$ is asserted. In multiprocessor systems, the master DSP drives $\overline{MS1–0}$.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

Table 15. Pin Definitions—Power, Ground, and Reference

Signal	Type	Term	Description
V_{DD}	P	au	V_{DD} pins for internal logic.
V_{DD_A}	P	au	V_{DD} pins for analog circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	au	V_{DD} pins for I/O buffers.
V_{REF}	I	au	Reference voltage defines the trip point for all input buffers, except $\overline{RESET}$, $\overline{IRQ3–0}$, $\overline{DMAR3–0}$, ID2–0, CONTROLIMP2–0, TCK, TDI, TMS, and $\overline{TRST}$. The value is 1.5 V ± 100 mV (which is the TTL trip point). V_{REF} can be connected to a power supply or set by a voltage divider circuit. The voltage divider should have an HF decoupling capacitor (1 nF HF SMD) connected to V_{SS}. Tie the decoupling capacitor between V_{REF} input and V_{SS}, as close to the DSP's pins as possible. For more information, see Filtering Reference Voltage and Clocks on Page 10.
V_{SS}	G	au	Ground pins.
V_{SS_A}	G	au	Ground pins for analog circuits.
NC			No connect. Do not connect these pins to anything (not to any supply, signal, or each other), because they are reserved and must be left unconnected.

Type column symbols: A = asynchronous; G = ground; I = input; O = output; o/d = open drain output; P = power supply; pd = internal pull-down approximately 100 kΩ; pu = internal pull-up approximately 100 kΩ; T = three-state

Term (for termination) column symbols: epd = external pull-down approximately 10 kΩ to V_{SS}; epu = external pull-up approximately 10 kΩ to V_{DD-IO}, nc = not connected; au = always used.

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set DSP operating modes. During reset, the DSP samples the strap option pins. Strap pins have an approximately 100 kΩ pull-down for the default value. If a strap pin is not connected to an external pull-up or logic load, the DSP samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up. In a multiprocessor system, up to eight DSPs may be connected on the cluster bus, resulting in parallel combination of strap pin pull-down resistors. Table 16 lists and describes each of the DSP's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	On Pin …	Description
EBOOT	$\overline{BMS}$	EPROM boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot DSP through the external port or a link port
IRQEN	$\overline{BM}$	Interrupt Enable. 0 = disable and set $\overline{IRQ3–0}$ interrupts to level sensitive after reset (default) 1 = enable and set $\overline{IRQ3–0}$ interrupts to edge sensitive immediately after reset
TM1	L2DIR	Test Mode 1. 0 = required setting during reset. 1 = reserved.
TM2	TMR0E	Test Mode 2. 0 = required setting during reset. 1 = reserved.

Table 22. Reference Clocks—System Clock (SCLK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{SCLK}[1, 2, 3, 4]	System Clock Cycle Time	10	25	ns
t_{SCLKH}	System Clock Cycle High Time	$0.4 \times t_{SCLK}$	$0.6 \times t_{SCLK}$	ns
t_{SCLKL}	System Clock Cycle Low Time	$0.4 \times t_{SCLK}$	$0.6 \times t_{SCLK}$	ns
t_{SCLKJ}[5, 6]	System Clock Jitter Tolerance		500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] LCLK_P and SCLK_P must be connected to the same source.
[4] The value of (t_{SCLK} / LCLKRAT2-0) must not violate the specification for t_{CCLK}.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

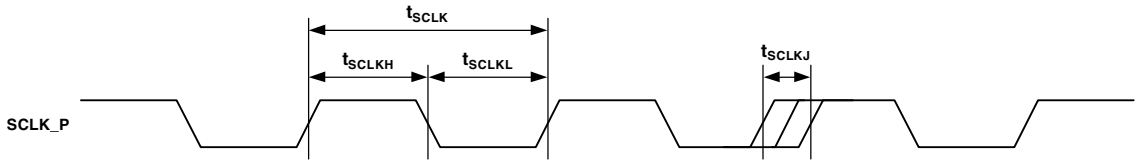

Figure 11. Reference Clocks—System Clock (SCLK) Cycle Time

Table 23. Reference Clocks—Test Clock (TCK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{TCK}	Test Clock (JTAG) Cycle Time	Greater of 30 or $t_{CCLK} \times 4$		ns
t_{TCKH}	Test Clock (JTAG) Cycle High Time	12.5		ns
t_{TCKL}	Test Clock (JTAG) Cycle Low Time	12.5		ns

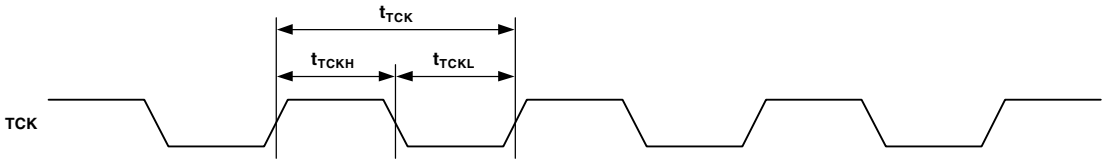

Figure 12. Reference Clocks—Test Clock (TCK) Cycle Time

Table 24. Power-Up Timing[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{VDD_IO}	V_{DD_IO} Stable and Within Specification After V_{DD} and V_{DD_A} Are Stable and Within Specification	>0		ms

[1] For information about power supply sequencing and monitoring solutions, please visit http://www.analog.com/sequencing.

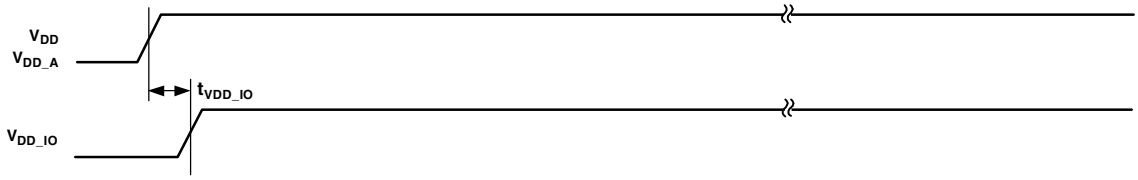

Figure 13. Power-Up Sequencing Timing

Table 25. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{START_LO}	$\overline{RESET}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, SCLK/LCLK, and Static/Strap Pins Are Stable and Within Specification	2		ms
t_{PULSE1_HI}	$\overline{RESET}$ Deasserted for First Pulse	$50 \times t_{SCLK}$	$100 \times t_{SCLK}$	ns
t_{PULSE2_LO}	$\overline{RESET}$ Asserted for Second Pulse	$100 \times t_{SCLK}$		ns
t_{TRST_PWR}[1]	$\overline{TRST}$ Asserted During Power-Up Reset	$2 \times t_{SCLK}$		ns

[1] Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, and SCLK/LCLK and static/strap pins are stable and within specification, and before $\overline{RESET}$ is deasserted.

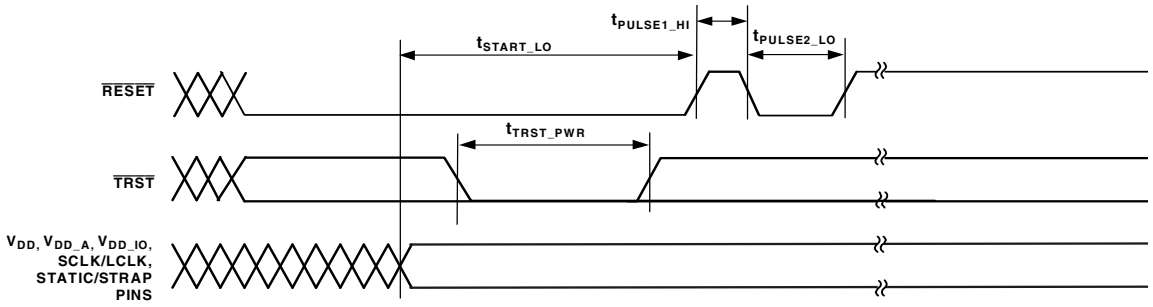

Figure 14. Power-Up Reset Timing

Table 26. Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RST_IN}	$\overline{RESET}$ Asserted	$100 \times t_{SCLK}$		ns
t_{STRAP}	$\overline{RESET}$ Deasserted After Strap Pins Stable	2		ms

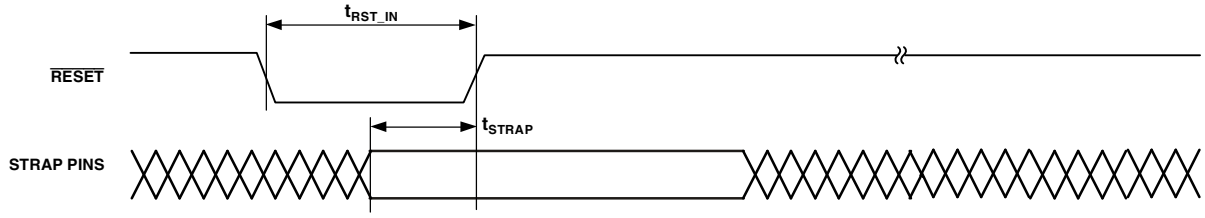

Figure 15. Normal Reset (Hot Reset) Timing

Table 27. AC Signal Specifications (for SCLK <16.7 ns) (All values in this table are in nanoseconds)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
ADDR31–0	External Address Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
DATA63–0	External Data Bus	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSH}}$	Memory Select Host Line			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MSSD}}$	Memory Select SDRAM Line	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RD}}$	Memory Read	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRL}}$	Write Low Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{WRH}}$	Write High Word	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
ACK	Acknowledge for Data	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
SDCKE	SDRAM Clock Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{RAS}}$	Row Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CAS}}$	Column Address Select	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
LDQM	Low Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
HDQM	High Word SDRAM Data Mask			4.2	1.0	0.9	2.5	SCLK
SDA10	SDRAM ADDR10			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{HBR}}$	Host Bus Request	2.6	0.5					SCLK
$\overline{\text{HBG}}$	Host Bus Grant	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BOFF}}$	Back Off Request	2.6	0.5					SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BRST}}$	Burst Access	2.6	0.5	4.2	1.0	0.9	2.5	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request	2.6	0.5	4.2	1.0			SCLK
$\overline{\text{FLYBY}}$	Flyby Mode Selection			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{IOEN}}$	Flyby I/O Enable			4.2	1.0	0.9	2.5	SCLK
$\overline{\text{CPA}}$ [3, 4]	Core Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{DPA}}$ [3, 4]	DMA Priority Access	2.6	0.5	5.8			2.5	SCLK
$\overline{\text{BMS}}$[5]	Boot Memory Select			4.2	1.0	0.9	2.5	SCLK
FLAG3–0[6]	FLAG Pins			4.2	1.0	1.0	4.0	SCLK
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	1.0			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

Table 28. AC Signal Specifications (for 16.7 ns <SCLK <25 ns) (All values in this table are in nanoseconds) (Continued)

Name	Description	Input Setup (min)	Input Hold (min)	Output Valid (max)[1]	Output Hold (min)	Output Enable (min)[2]	Output Disable (max)[2]	Reference Clock
$\overline{\text{RESET}}$[4, 7]	Global Reset							SCLK
TMS[4]	Test Mode Select (JTAG)	1.5	1.0					TCK
TDI[4]	Test Data Input (JTAG)	1.5	1.0					TCK
TDO	Test Data Output (JTAG)			6.0	1.0	1.0	5.0	TCK_FE[8]
$\overline{\text{TRST}}$[4, 7, 9]	Test Reset (JTAG)							TCK
$\overline{\text{BM}}$[5]	Bus Master Debug Aid Only			4.2	0.8			SCLK
$\overline{\text{EMU}}$[10]	Emulation			5.5			5.0	TCK or LCLK
JTAG_SYS_IN[11]	System Input	1.5	11.0					TCK
JTAG_SYS_OUT[12]	System Output			16.0				TCK_FE[8]
ID2–0[9]	Chip ID—Must Be Constant							
CONTROLIMP2–0[9]	Static Pins—Must Be Constant							
DS2–0[9]	Static Pins—Must Be Constant							
LCLKRAT2–0[9]	Static Pins—Must Be Constant							
SCLKFREQ[9]	Static Pins—Must Be Constant							

[1] The output valid (max) value in this column applies for the standard 30 pF capacitive load used in testing. To see how output valid varies with capacitive loading, see Figure 40 on Page 36.

[2] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.

[3] $\overline{\text{CPA}}$ and $\overline{\text{DPA}}$ pins are open drains and have 0.5 kΩ internal pull-ups.

[4] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference. These synchronous specifications only apply for recognition in the current clock reference cycle.

[5] This pin is a strap option. During reset, an internal resistor pulls the pin low.

[6] For input specifications, see Table 21.

[7] For additional requirement details, see Reset and Booting on Page 9.

[8] TCK_FE indicates TCK falling edge.

[9] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.

[10] Reference clock depends on function.

[11] System inputs are: $\overline{\text{IRQ3–0}}$, $\overline{\text{BMS}}$, LCLKRAT2–0, SCLKFREQ, $\overline{\text{BM}}$, TMR0E, FLAG3–0, ID2–0, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, $\overline{\text{BOFF}}$, $\overline{\text{HBR}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKIN, L0DAT7–0, L1CLKIN, L1DAT7–0, L2CLKIN, L2DAT7–0, L2DIR, L3CLKIN, L3DAT7–0, DS2–0, CONTROLIMP2–0, $\overline{\text{RESET}}$, $\overline{\text{DMAR3–0}}$.

[12] System outputs are: $\overline{\text{BMS}}$, $\overline{\text{BM}}$, $\overline{\text{BUSLOCK}}$, TMR0E, FLAG3–0, $\overline{\text{FLYBY}}$, $\overline{\text{IOEN}}$, $\overline{\text{MSH}}$, $\overline{\text{BRST}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{RD}}$, $\overline{\text{MS1–0}}$, HDQM, LDQM, $\overline{\text{MSSD}}$, SDCKE, $\overline{\text{SDWE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, ADDR31–0, DATA63–0, $\overline{\text{DPA}}$, $\overline{\text{CPA}}$, $\overline{\text{HBG}}$, ACK, $\overline{\text{BR7–0}}$, L0CLKOUT, L0DAT7–0, L0DIR, L1CLKOUT, L1DAT7–0, L1DIR, L2CLKOUT, L2DAT7–0, L2DIR, L3CLKOUT, L3DAT7–0, L3DIR, $\overline{\text{EMU}}$.

Link Ports Data Transfer and Token Switch Timing

Table 31, Table 32, Table 33, and Table 34 with Figure 17, Figure 18, Figure 19, and Figure 20 provide the timing specifications for the link ports data transfer and token switch.

Table 29. Link Ports—Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{CONNS}[1]	Connectivity Pulse Setup	$2 \times t_{CCLK} + 3.5$		ns
t_{CONNS}[2]	Connectivity Pulse Setup	8		ns
t_{CONNIW}[3]	Connectivity Pulse Input Width	$t_{LxCLK\_Tx} + 1$		ns
t_{ACKS}	Acknowledge Setup	$0.5 \times t_{LxCLK\_Tx}$		ns
Switching Characteristics				
t_{LxCLK_Tx}[4]	Transmit Link Clock Period	$0.9 \times LR \times t_{CCLK}$	$1.1 \times LR \times t_{CCLK}$	ns
t_{LxCLKH_Tx}[1]	Transmit Link Clock Width High	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKH_Tx}[2]	Transmit Link Clock Width High	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[1]	Transmit Link Clock Width Low	$0.33 \times t_{LxCLK\_Tx}$	$0.66 \times t_{LxCLK\_Tx}$	ns
t_{LxCLKL_Tx}[2]	Transmit Link Clock Width Low	$0.4 \times t_{LxCLK\_Tx}$	$0.6 \times t_{LxCLK\_Tx}$	ns
t_{DIRS}	LxDIR Transmit Setup	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DIRH}	LxDIR Transmit Hold	$0.5 \times t_{LxCLK\_Tx}$	$2 \times t_{LxCLK\_Tx}$	ns
t_{DOS}[1]	LxDAT7–0 Output Setup	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[1]	LxDAT7–0 Output Hold	$0.25 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOS}[2]	LxDAT7–0 Output Setup	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{DOH}[2]	LxDAT7–0 Output Hold	Greater of 0.8 or $0.17 \times t_{LxCLK\_Tx} - 1$		ns
t_{LDOE}	LxDAT7–0 Output Enable	1		ns
t_{LDOD}[5]	LxDAT7–0 Output Disable	1		ns

[1] The formula for this parameter applies when LR is 2.
[2] The formula for this parameter applies when LR is 3, 4, or 8.
[3] LxCLKIN shows the connectivity pulse with each of the three possible transitions to "Acknowledge." After a connectivity pulse low minimum, LxCLKIN may [1] return high and remain high for "Acknowledge," [2] return high and subsequently go low (meeting t_{ACKS}) for "Not Acknowledge," or [3] remain low for "Not Acknowledge."
[4] The Link clock Ratio (LR) is 2, 3, 4, or 8 as set by the SPD bits in the LCTLx register. The maximum LxCLK is 125 MHz. LR = 2 may not be used when CCLK ≥ 250 MHz.
[5] This specification applies to the last data byte or the "Dummy" byte that follows the verification byte if enabled. For more information, see the *ADSP-TS101* TigerSHARC *Processor Hardware Reference*.

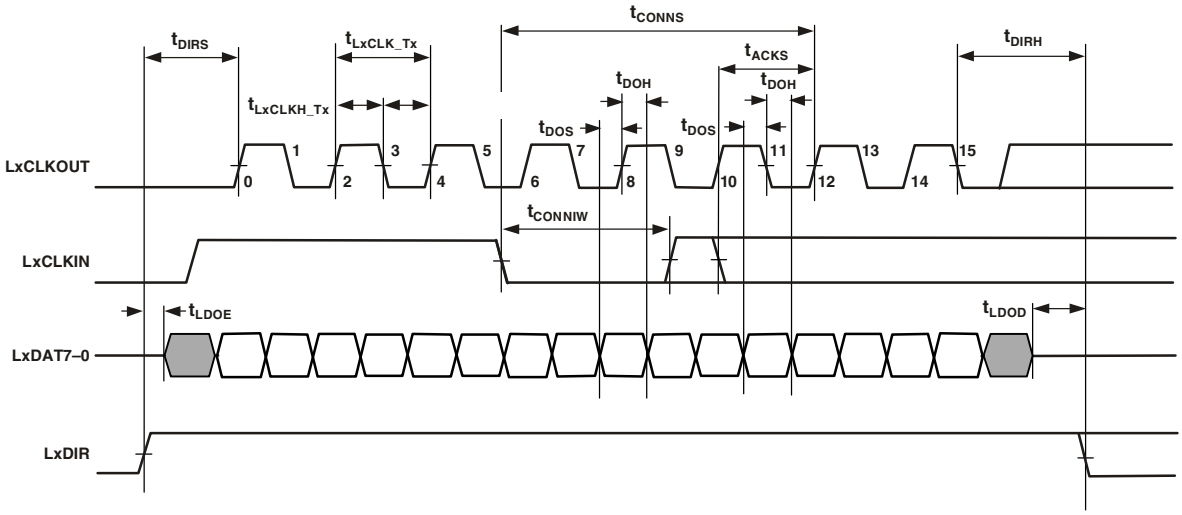

Figure 17. Link Ports—Transmit

Table 30. Link Ports—Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{LxCLK_Rx}[1, 2]	Receive Link Clock Period	$0.9 \times LR \times t_{CCLK}$	$1.1 \times LR \times t_{CCLK}$	ns
t_{LxCLKH_Rx}[3]	Receive Link Clock Width High	$0.33 \times t_{LxCLK\_Rx}$	$0.66 \times t_{LxCLK\_Rx}$	ns
t_{LxCLKH_Rx}[4]	Receive Link Clock Width High	$0.4 \times t_{LxCLK\_Rx}$	$0.6 \times t_{LxCLK\_Rx}$	ns
t_{LxCLKL_Rx}[3]	Receive Link Clock Width Low	$0.33 \times t_{LxCLK\_Rx}$	$0.66 \times t_{LxCLK\_Rx}$	ns
t_{LxCLKL_Rx}[4]	Receive Link Clock Width Low	$0.4 \times t_{LxCLK\_Rx}$	$0.6 \times t_{LxCLK\_Rx}$	ns
t_{DIS}	LxDAT7–0 Input Setup	0.6		ns
t_{DIH}	LxDAT7–0 Input Hold	0.6		ns
Switching Characteristics				
t_{CONNV}	Connectivity Pulse Valid	0	$2.5 \times t_{LxCLK\_Rx}$	ns
t_{CONNOW}	Connectivity Pulse Output Width	$1.5 \times t_{LxCLK\_Rx}$		ns

[1] The link clock ratio (LR) is 2, 3, 4, or 8 as set by the SPD bits in the LCTLx register.
[2] The maximum LxCLK is 125 MHz. LR = 2 may not be used when CCLK ≥ 250 MHz.
[3] The formula for this parameter applies when LR is 2.
[4] The formula for this parameter applies when LR is 3, 4, or 8.

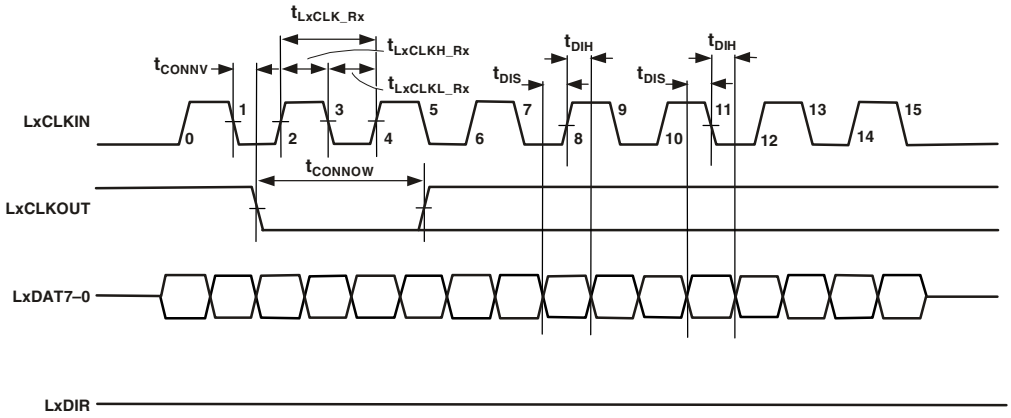

Figure 18. Link Ports—Receive

Table 31. Link Ports—Token Switch, Token Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{REQI}	Token Request Input Width	$5.0 \times t_{LxCLK\_Rx}$		ns
t_{TKRQ}	Token Request from Token Enable[1]		$3.0 \times t_{LxCLK\_Tx}$	ns
Switching Characteristics				
t_{TKENO}	Token Switch Enable Output	$8.0 \times t_{LxCLK\_Tx}$		ns
t_{REQO}	Token Request Output Width[2]	$6.0 \times t_{LxCLK\_Tx}$		ns

[1] For guaranteeing token switch during token enable.
[2] LxCLKOUT shows both possible responses to the token request: [1] a "Token Grant" (LxCLKOUT remains high), and [2] a "Token Regret" (LxCLKOUT goes low).

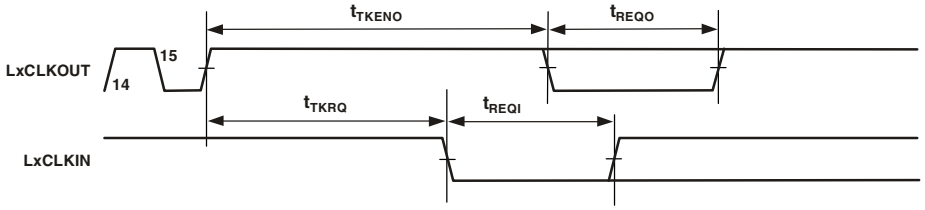

Figure 19. Link Ports—Token Switch, Token Master

Table 32. Link Ports—Token Switch, Token Requester

Parameter		Min	Max	Unit
Timing Requirements				
t_{TKENI}[1]	Token Switch Enable Input	$8.0 \times t_{LxCLK\_Rx}$		ns
Switching Characteristics				
t_{REQO}	Token Request Output Width[2]	$6.0 \times t_{LxCLK\_Rx}$		ns

[1] Required whenever there is a break in transmission.
[2] LxCLKOUT shows both possible responses to the token request: [1] a "Token Grant" (LxCLKOUT remains high), and [2] a "Token Regret" (LxCLKOUT goes low).

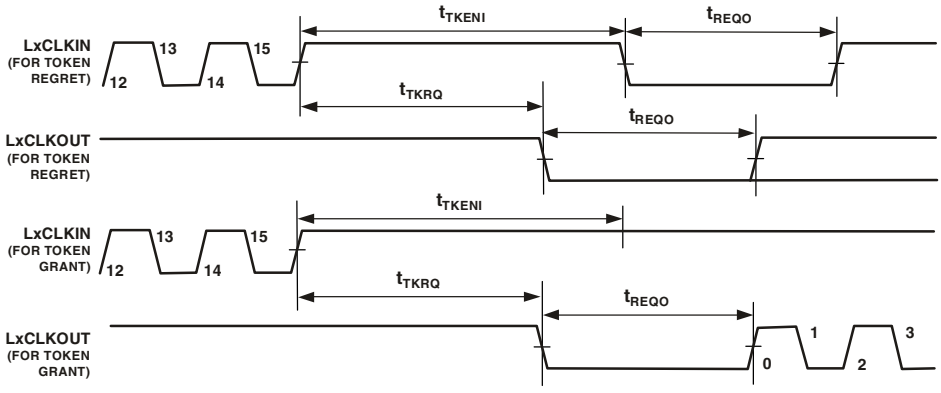

Figure 20. Link Ports—Token Switch, Token Requester

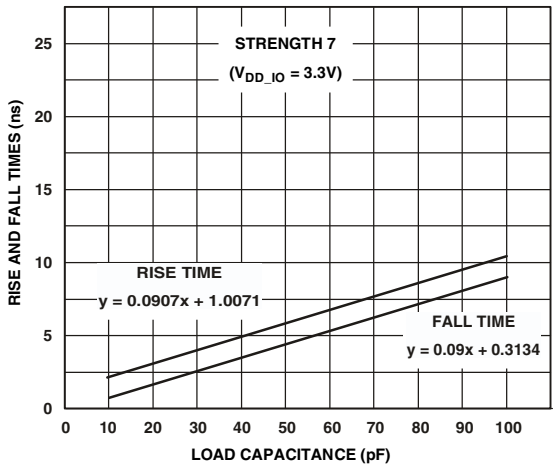

Figure 39. Typical Output Rise and Fall Time (10%–90%, V_{DD_IO} = 3.3 V) vs. Load Capacitance at Strength 7

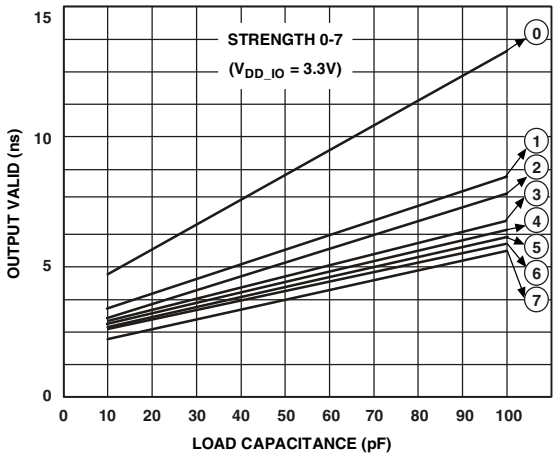

Figure 40. Typical Output Valid (V_{DD_IO} = 3.3 V) vs. Load Capacitance at Max Case Temperature and Strength 0–7[1]

[1] The line equations for the output valid vs. load capacitance are:
Strength 0: y = 0.0956x + 3.5662
Strength 1: y = 0.0523x + 3.2144
Strength 2: y = 0.0433x + 3.1319
Strength 3: y = 0.0391x + 2.9675
Strength 4: y = 0.0393x + 2.7653
Strength 5: y = 0.0373x + 2.6515
Strength 6: y = 0.0379x + 2.1206
Strength 7: y = 0.0399x + 1.9080

ENVIRONMENTAL CONDITIONS

The ADSP-TS101S is rated for performance over the extended commercial temperature range, T_{CASE} = –40°C to +85°C.

Thermal Characteristics

The ADSP-TS101S is packaged in a 19 mm × 19 mm and 27 mm × 27 mm Plastic Ball Grid Array (PBGA). The ADSP-TS101S is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heat sink and/or an air flow source may be used. See Table 33 and Table 34 for thermal data.

Table 33. Thermal Characteristics for 19 mm × 19 mm Package

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow[2] = 0 m/s	16.6	°C/W
	Airflow[3] = 1 m/s	14.0	°C/W
	Airflow[3] = 2 m/s	12.9	°C/W
θ_{JC}		6.7	°C/W
θ_{JB}		5.8	°C/W

[1] Determination of parameter is system dependent and is based on a number of factors, including device power dissipation, package thermal resistance, board thermal characteristics, ambient temperature, and air flow.
[2] Per JEDEC JESD51-2 procedure using a four layer board (compliant with JEDEC JESD51-9).
[3] Per SEMI Test Method G38-87 using a four layer board (compliant with JEDEC JESD51-9).

Table 34. Thermal Characteristics for 27 mm × 27 mm Package

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow[2] = 0 m/s	13.8	°C/W
	Airflow[3] = 1 m/s	11.7	°C/W
	Airflow[3] = 2 m/s	10.8	°C/W
θ_{JC}		3.1	°C/W
θ_{JB}		5.9	°C/W

[1] Determination of parameter is system dependent and is based on a number of factors, including device power dissipation, package thermal resistance, board thermal characteristics, ambient temperature, and air flow.
[2] Per JEDEC JESD51-2 procedure using a four layer board (compliant with JEDEC JESD51-9).
[3] Per SEMI Test Method G38-87 using a four layer board (compliant with JEDEC JESD51-9).

PBGA PIN CONFIGURATIONS

The 484-ball PBGA pin configurations appear in Table 35 and Figure 41. The 625-ball PBGA pin configurations appear in Table 36 and Figure 42.

Table 35. 484-Ball (19 mm × 19 mm) PBGA Pin Assignments

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
A1	V_{SS}	B1	DATA21	C1	DATA23	D1	DATA24	E1	DATA25
A2	DATA14	B2	DATA18	C2	DATA17	D2	DATA19	E2	DATA22
A3	DATA11	B3	DATA12	C3	DATA15	D3	DATA16	E3	DATA20
A4	DATA8	B4	DATA13	C4	DATA9	D4	V_{DD_IO}	E4	V_{DD_IO}
A5	DATA4	B5	DATA7	C5	DATA10	D5	V_{DD}	E5	V_{DD}
A6	DATA1	B6	DATA5	C6	DATA6	D6	V_{DD}	E6	V_{DD}
A7	L0DIR	B7	DATA2	C7	DATA3	D7	V_{DD_IO}	E7	V_{DD_IO}
A8	L0CLKIN	B8	NC	C8	DATA0	D8	V_{DD_IO}	E8	V_{DD}
A9	L0DAT6	B9	L0DAT7	C9	L0CLKOUT	D9	V_{DD_IO}	E9	V_{DD}
A10	L0DAT3	B10	L0DAT4	C10	L0DAT5	D10	V_{DD_IO}	E10	V_{DD}
A11	L0DAT1	B11	L0DAT0	C11	L0DAT2	D11	V_{DD_IO}	E11	V_{DD_IO}
A12	V_{SS}	B12	V_{SS}	C12	LCLK_P	D12	V_{DD_IO}	E12	V_{DD}
A13	LCLK_N	B13	V_{DD_A}	C13	V_{SS}	D13	V_{DD_IO}	E13	V_{DD_IO}
A14	V_{SS_A}	B14	V_{SS_A}	C14	V_{DD_A}	D14	V_{DD_IO}	E14	V_{DD}
A15	SCLK_N	B15	V_{SS}	C15	DS0	D15	V_{DD_IO}	E15	V_{DD_IO}
A16	SCLK_P	B16	DS1	C16	DS2	D16	V_{DD}	E16	V_{DD}
A17	CONTROLIMP2	B17	CONTROLIMP0	C17	V_{REF}	D17	V_{DD_IO}	E17	V_{DD_IO}
A18	CONTROLIMP1	B18	$\overline{\text{DMAR2}}$	C18	TRST	D18	V_{DD}	E18	V_{DD_IO}
A19	$\overline{\text{RESET}}$	B19	$\overline{\text{DMAR0}}$	C19	$\overline{\text{DMAR3}}$	D19	V_{DD_IO}	E19	V_{DD_IO}
A20	$\overline{\text{DMAR1}}$	B20	TMS	C20	TCK	D20	TDO	E20	$\overline{\text{BM}}$
A21	$\overline{\text{EMU}}$	B21	TDI	C21	$\overline{\text{IRQ3}}$	D21	$\overline{\text{IRQ2}}$	E21	$\overline{\text{BMS}}$
A22	V_{SS}	B22	$\overline{\text{IRQ1}}$	C22	$\overline{\text{IRQ0}}$	D22	LCLKRAT1	E22	LCLKRAT2
F1	DATA29	G1	L3DAT1	H1	L3DAT2	J1	L3DAT5	K1	L3CLKOUT
F2	DATA30	G2	DATA28	H2	L3DAT0	J2	L3DAT3	K2	L3DAT7
F3	DATA26	G3	DATA27	H3	DATA31	J3	L3DAT4	K3	L3DAT6
F4	V_{DD_IO}	G4	V_{DD}	H4	V_{DD}	J4	V_{DD_IO}	K4	V_{DD_IO}
F5	V_{DD_IO}	G5	V_{DD}	H5	V_{DD}	J5	V_{DD_IO}	K5	V_{DD_IO}
F6	V_{SS}	G6	V_{SS}	H6	V_{SS}	J6	V_{SS}	K6	V_{SS}
F7	V_{SS}	G7	V_{SS}	H7	V_{SS}	J7	V_{SS}	K7	V_{SS}
F8	V_{SS}	G8	V_{SS}	H8	V_{SS}	J8	V_{SS}	K8	V_{SS}
F9	V_{SS}	G9	V_{SS}	H9	V_{SS}	J9	V_{SS}	K9	V_{SS}
F10	V_{SS}	G10	V_{SS}	H10	V_{SS}	J10	V_{SS}	K10	V_{SS}
F11	V_{SS}	G11	V_{SS}	H11	V_{SS}	J11	V_{SS}	K11	V_{SS}
F12	V_{SS}	G12	V_{SS}	H12	V_{SS}	J12	V_{SS}	K12	V_{SS}
F13	V_{SS}	G13	V_{SS}	H13	V_{SS}	J13	V_{SS}	K13	V_{SS}
F14	V_{SS}	G14	V_{SS}	H14	V_{SS}	J14	V_{SS}	K14	V_{SS}
F15	V_{SS}	G15	V_{SS}	H15	V_{SS}	J15	V_{SS}	K15	V_{SS}
F16	V_{SS}	G16	V_{SS}	H16	V_{SS}	J16	V_{SS}	K16	V_{SS}
F17	V_{DD}	G17	V_{SS}	H17	V_{SS}	J17	V_{SS}	K17	V_{SS}
F18	V_{DD_IO}	G18	V_{DD}	H18	V_{DD_IO}	J18	V_{DD}	K18	V_{DD}
F19	V_{DD_IO}	G19	V_{DD_IO}	H19	V_{DD_IO}	J19	V_{DD_IO}	K19	V_{DD_IO}
F20	LCLKRAT0	G20	FLAG3	H20	FLAG1	J20	ID0	K20	$\overline{\text{IOEN}}$
F21	SCLKFREQ	G21	$\overline{\text{BUSLOCK}}$	H21	FLAG2	J21	ID2	K21	$\overline{\text{FLYBY}}$

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
L1	L3CLKIN	M1	L1DAT0	N1	L1DAT2	P1	L1DAT5	R1	L1CLKOUT
L2	L3CLKOUT	M2	NC	N2	NC	P2	L1DAT4	R2	L1DAT7
L3	L3DAT7	M3	L3DIR	N3	L1DAT1	P3	L1DAT3	R3	L1DAT6
L4	V_{DD_IO}	M4	V_{DD_IO}	N4	V_{DD_IO}	P4	V_{DD_IO}	R4	V_{DD_IO}
L5	V_{DD}	M5	V_{DD}	N5	V_{DD_IO}	P5	V_{DD_IO}	R5	V_{DD}
L6	V_{DD}	M6	V_{DD}	N6	V_{DD}	P6	V_{DD}	R6	V_{DD}
L7	V_{SS}	M7	V_{SS}	N7	V_{SS}	P7	V_{SS}	R7	V_{SS}
L8	V_{SS}	M8	V_{SS}	N8	V_{SS}	P8	V_{SS}	R8	V_{SS}
L9	V_{SS}	M9	V_{SS}	N9	V_{SS}	P9	V_{SS}	R9	V_{SS}
L10	V_{SS}	M10	V_{SS}	N10	V_{SS}	P10	V_{SS}	R10	V_{SS}
L11	V_{SS}	M11	V_{SS}	N11	V_{SS}	P11	V_{SS}	R11	V_{SS}
L12	V_{SS}	M12	V_{SS}	N12	V_{SS}	P12	V_{SS}	R12	V_{SS}
L13	V_{SS}	M13	V_{SS}	N13	V_{SS}	P13	V_{SS}	R13	V_{SS}
L14	V_{SS}	M14	V_{SS}	N14	V_{SS}	P14	V_{SS}	R14	V_{SS}
L15	V_{SS}	M15	V_{SS}	N15	V_{SS}	P15	V_{SS}	R15	V_{SS}
L16	V_{SS}	M16	V_{SS}	N16	V_{SS}	P16	V_{SS}	R16	V_{SS}
L17	V_{SS}	M17	V_{SS}	N17	V_{SS}	P17	V_{SS}	R17	V_{SS}
L18	V_{SS}	M18	V_{SS}	N18	V_{SS}	P18	V_{SS}	R18	V_{SS}
L19	V_{SS}	M19	V_{SS}	N19	V_{SS}	P19	V_{SS}	R19	V_{SS}
L20	V_{DD}	M20	V_{DD}	N20	V_{DD}	P20	V_{DD}	R20	V_{DD}
L21	V_{DD}	M21	V_{DD_IO}	N21	V_{DD_IO}	P21	V_{DD}	R21	V_{DD}
L22	V_{DD_IO}	M22	V_{DD_IO}	N22	V_{DD_IO}	P22	V_{DD_IO}	R22	V_{DD_IO}
L23	NC	M23	$\overline{\text{IOEN}}$	N23	$\overline{\text{WRH}}$	P23	$\overline{\text{MS1}}$	R23	LDQM
L24	NC	M24	$\overline{\text{MSH}}$	N24	$\overline{\text{WRL}}$	P24	$\overline{\text{MS0}}$	R24	NC
L25	$\overline{\text{FLYBY}}$	M25	$\overline{\text{BRST}}$	N25	$\overline{\text{RD}}$	P25	HDQM	R25	$\overline{\text{MSSD}}$
T1	NC	U1	DATA34	V1	DATA37	W1	DATA40	Y1	DATA43
T2	L1DIR	U2	DATA33	V2	DATA36	W2	DATA39	Y2	DATA42
T3	L1CLKIN	U3	DATA32	V3	DATA35	W3	DATA38	Y3	DATA41
T4	V_{DD_IO}	U4	V_{DD_IO}	V4	V_{DD_IO}	W4	V_{DD_IO}	Y4	V_{DD_IO}
T5	V_{DD}	U5	V_{DD_IO}	V5	V_{DD_IO}	W5	V_{DD}	Y5	V_{DD}
T6	V_{DD}	U6	V_{DD}	V6	V_{DD}	W6	V_{DD}	Y6	V_{DD}
T7	V_{SS}	U7	V_{SS}	V7	V_{SS}	W7	V_{SS}	Y7	V_{DD}
T8	V_{SS}	U8	V_{SS}	V8	V_{SS}	W8	V_{SS}	Y8	V_{DD}
T9	V_{SS}	U9	V_{SS}	V9	V_{SS}	W9	V_{SS}	Y9	V_{DD}
T10	V_{SS}	U10	V_{SS}	V10	V_{SS}	W10	V_{SS}	Y10	V_{DD}
T11	V_{SS}	U11	V_{SS}	V11	V_{SS}	W11	V_{SS}	Y11	V_{DD}
T12	V_{SS}	U12	V_{SS}	V12	V_{SS}	W12	V_{SS}	Y12	V_{DD}
T13	V_{SS}	U13	V_{SS}	V13	V_{SS}	W13	V_{SS}	Y13	V_{DD}
T14	V_{SS}	U14	V_{SS}	V14	V_{SS}	W14	V_{SS}	Y14	V_{DD}
T15	V_{SS}	U15	V_{SS}	V15	V_{SS}	W15	V_{SS}	Y15	V_{DD}
T16	V_{SS}	U16	V_{SS}	V16	V_{SS}	W16	V_{SS}	Y16	V_{DD}
T17	V_{SS}	U17	V_{SS}	V17	V_{SS}	W17	V_{SS}	Y17	V_{DD}
T18	V_{SS}	U18	V_{SS}	V18	V_{SS}	W18	V_{SS}	Y18	V_{DD}
T19	V_{SS}	U19	V_{SS}	V19	V_{SS}	W19	V_{SS}	Y19	V_{DD}
T20	V_{DD}	U20	V_{DD}	V20	V_{DD}	W20	V_{DD}	Y20	V_{DD}
T21	V_{DD_IO}	U21	V_{DD_IO}	V21	V_{DD}	W21	V_{DD}	Y21	V_{DD_IO}
T22	V_{DD_IO}	U22	V_{DD_IO}	V22	V_{DD_IO}	W22	V_{DD_IO}	Y22	V_{DD_IO}
T23	SDCKE	U23	$\overline{\text{CAS}}$	V23	ADDR31	W23	ADDR28	Y23	ADDR26
T24	NC	U24	NC	V24	ADDR30	W24	NC	Y24	ADDR25
T25	$\overline{\text{SDWE}}$	U25	$\overline{\text{RAS}}$	V25	ADDR29	W25	ADDR27	Y25	ADDR24

Table 36. 625-Ball (27 mm × 27 mm) PBGA Pin Assignments (Continued)

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
AA1	DATA46	AB1	DATA49	AC1	V_{SS}	AD1	V_{SS}	AE1	V_{SS}
AA2	DATA45	AB2	DATA48	AC2	V_{SS}	AD2	V_{SS}	AE2	V_{SS}
AA3	DATA44	AB3	DATA47	AC3	DATA50	AD3	V_{SS}	AE3	V_{SS}
AA4	V_{DD_IO}	AB4	V_{DD_IO}	AC4	DATA51	AD4	DATA52	AE4	DATA53
AA5	V_{DD_IO}	AB5	V_{DD_IO}	AC5	DATA54	AD5	DATA55	AE5	DATA56
AA6	V_{DD_IO}	AB6	V_{DD_IO}	AC6	DATA57	AD6	DATA58	AE6	DATA59
AA7	V_{DD}	AB7	V_{DD_IO}	AC7	DATA60	AD7	DATA61	AE7	DATA62
AA8	V_{DD}	AB8	V_{DD_IO}	AC8	DATA63	AD8	L2DAT0	AE8	L2DAT1
AA9	V_{DD_IO}	AB9	V_{DD_IO}	AC9	L2DAT2	AD9	L2DAT3	AE9	L2DAT4
AA10	V_{DD_IO}	AB10	V_{DD_IO}	AC10	L2DAT5	AD10	L2DAT6	AE10	L2DAT7
AA11	V_{DD}	AB11	V_{DD_IO}	AC11	L2CLKOUT	AD11	L2CLKIN	AE11	L2DIR
AA12	V_{DD}	AB12	V_{DD_IO}	AC12	NC	AD12	$\overline{BR0}$	AE12	$\overline{BR1}$
AA13	V_{DD_IO}	AB13	V_{DD_IO}	AC13	$\overline{BR2}$	AD13	$\overline{BR3}$	AE13	$\overline{BR4}$
AA14	V_{DD_IO}	AB14	V_{DD_IO}	AC14	$\overline{BR5}$	AD14	$\overline{BR6}$	AE14	$\overline{BR7}$
AA15	V_{DD}	AB15	V_{DD_IO}	AC15	ACK	AD15	$\overline{HBR}$	AE15	$\overline{BOFF}$
AA16	V_{DD}	AB16	V_{DD_IO}	AC16	$\overline{HBG}$	AD16	$\overline{CPA}$	AE16	$\overline{DPA}$
AA17	V_{DD_IO}	AB17	V_{DD_IO}	AC17	ADDR0	AD17	ADDR1	AE17	ADDR2
AA18	V_{DD_IO}	AB18	V_{DD_IO}	AC18	ADDR3	AD18	ADDR4	AE18	ADDR5
AA19	V_{DD}	AB19	V_{DD_IO}	AC19	ADDR6	AD19	ADDR7	AE19	ADDR8
AA20	V_{DD}	AB20	V_{DD_IO}	AC20	ADDR9	AD20	SDA10	AE20	ADDR10
AA21	V_{DD_IO}	AB21	V_{DD_IO}	AC21	ADDR11	AD21	ADDR12	AE21	ADDR13
AA22	V_{DD_IO}	AB22	V_{DD_IO}	AC22	ADDR14	AD22	ADDR15	AE22	V_{SS}
AA23	ADDR23	AB23	ADDR20	AC23	V_{SS}	AD23	V_{SS}	AE23	V_{SS}
AA24	ADDR22	AB24	ADDR19	AC24	ADDR17	AD24	V_{SS}	AE24	V_{SS}
AA25	ADDR21	AB25	ADDR18	AC25	ADDR16	AD25	V_{SS}	AE25	V_{SS}

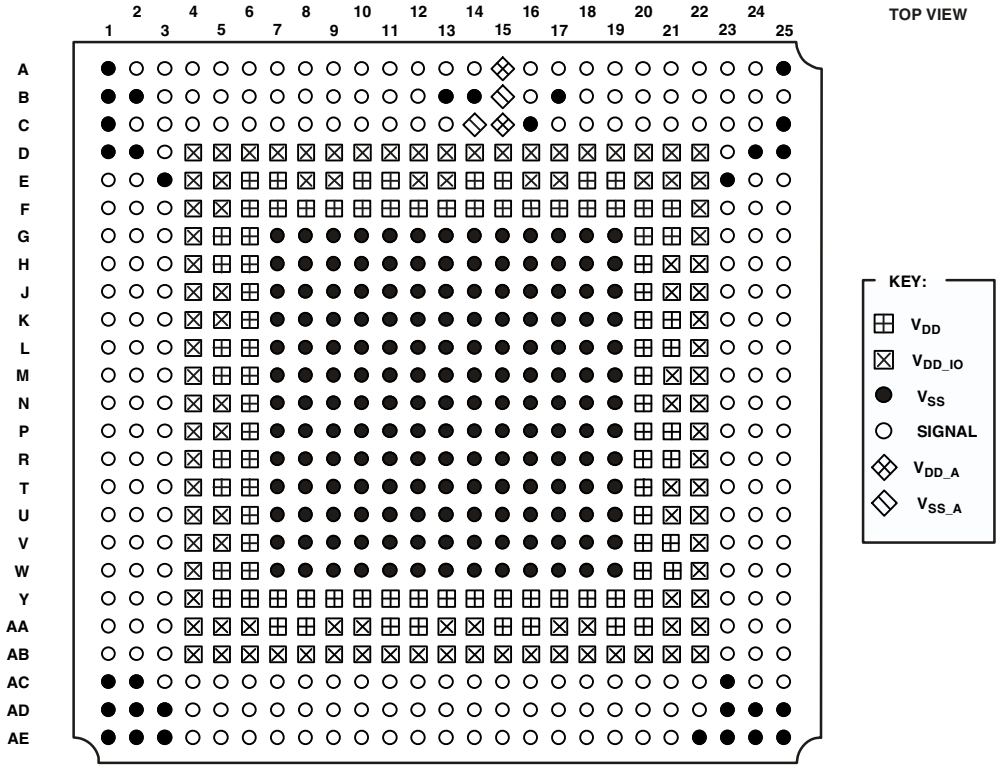

Figure 42. 625-Ball PBGA Pin Configurations (Top View, Summary)

OUTLINE DIMENSIONS

The ADSP-TS101S is available in a 19 mm × 19 mm, 484-ball PBGA package with 22 rows of balls (B-484); the DSP also is available in a 27 mm × 27 mm, 625-ball PBGA package with 25 rows of balls (B-625).

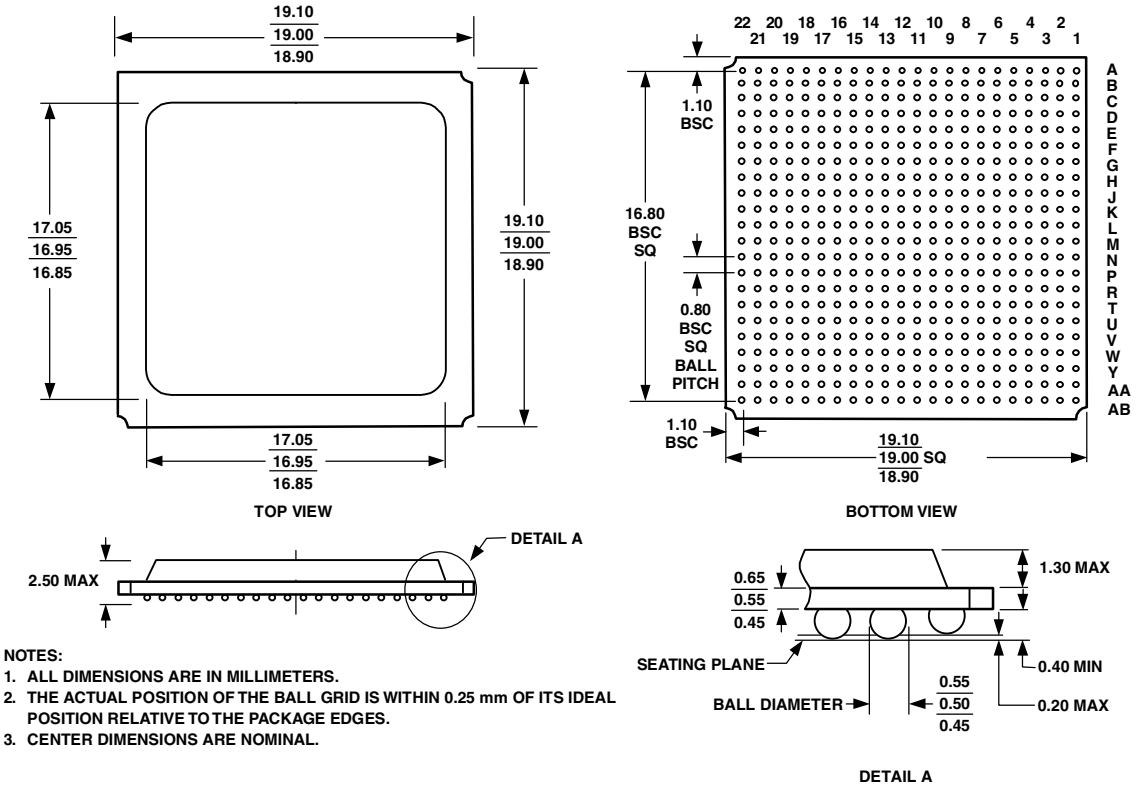

Figure 43. 484-Ball PBGA (B-484)