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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306n4fcfp-ukj

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M16C/6N Group (M16C/6N4) Renesas MCU

1. Overview

The M16C/6N Group (M16C/6N4) of MCUs are built using the high-performance silicon gate CMOS process using the M16C/60 Series CPU core and are packaged in 100-pin plastic molded QFP and LQFP. These MCUs operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. Being equipped with two CAN (Controller Area Network) modules in the M16C/6N Group (M16C/6N4), the MCU is suited to drive automotive and industrial control systems. The CAN modules comply with the 2.0B specification. In addition, this MCU contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/ logic operations.

1.1 Applications

- Automotive, industrial control systems and other automobile, other (T/V-ver. product)
- Car audio and industrial control systems, other (Normal-ver. product)

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.



2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits. Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt. Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

2.8.10 Reserved Area

When white to this bit, write 0. When read, its content is undefined.

Table 4.3 SFR Information (3)

Address	Register	Symbol	After Reset
0080h			XXh
0081h			XXh
0082h	CANO Massaga Box 2: Identifiar / DLC		XXh
0083h	CANO Message Dox 2. Identifier / DEO		XXh
0084h			XXh
0085h			XXh
0086h			XXh
0087h			XXh
0088h			XXh
0089h	CAN0 Message Box 2: Data Field		XXh
008Ah			XXh
008Bh			XXh
008Ch			XXh
008Dh			XXh
008Eh	CAN0 Message Box 2 ⁻ Time Stamp		XXh
008Fh			XXh
0090h			XXh
0091h			XXh
0092h	CAN0 Message Box 3: Identifier / DLC		XXh
0093h			XXh
0094h			XXh
0095h			XXh
0096h			XXh
0097h			XXn
0098h			
0099h	CAN0 Message Box 3: Data Field		
009Ah			XXII
009Bh			XXII XXb
00900	•		XXII XXb
009Dn			XXII XXb
009EN	CAN0 Message Box 3: Time Stamp		XXh
009111 0040b			XXh
00A01			XXh
00A2h			XXh
00A3h	CAN0 Message Box 4: Identifier / DLC		XXh
00A4h			XXh
00A5h			XXh
00A6h			XXh
00A7h			XXh
00A8h			XXh
00A9h	CANO Massage Day & Data Field		XXh
00AAh	CAINO Message Box 4: Data Field		XXh
00ABh			XXh
00ACh			XXh
00ADh			XXh
00AEh	CANO Message Box 4: Time Stamp		XXh
00AFh	Univo iviessaye dux 4. Tittle Stattip		XXh
00B0h			XXh
00B1h			XXh
00B2h	CANO Massaga Bay 5: Identifiar / DLC		XXh
00B3h	CANO Message Dox 5. Identifier / DEC		XXh
00B4h			XXh
00B5h			XXh
00B6h	4		XXh
00B7h			XXh
00B8h	4		XXh
00B9h	CAN0 Message Box 5: Data Field		XXh
00BAh			XXh
00BBh			XXh
00BCh			XXh
00BDh			XXh
00BEh	CAN0 Message Box 5: Time Stamp		XXh
00BFh	с r		XXh

X: Undefined



Table 4.5 SFR Information (5)

Address	Register	Symbol	After Reset
0100h			XXh
0101h			XXh
0102h	CANO Massage Devidor Identifier (DLO		XXh
0103h	CANO Message box To: Identifier / DLC		XXh
0104h			XXh
0105h			XXh
0106h			XXh
0107h			XXh
0108h			XXh
0109h	CANO Massage Day 10: Data Field		XXh
010Ah	CAINO Message Box TO: Data Fleid		XXh
010Bh			XXh
010Ch			XXh
010Dh			XXh
010Eh			XXh
010Fh	CANU Message Box 10: Time Stamp		XXh
0110h			XXh
0111h			XXh
0112h			XXh
0113h	CAN0 Message Box 11: Identifier / DLC		XXh
0114h			XXh
0115h			XXh
0116h			XXh
0117h			XXh
0118h			XXh
0119h			XXh
011Ah	CAN0 Message Box 11: Data Field		XXh
011Bh			XXh
011Ch			XXh
011Dh			XXh
011Eh			XXh
011Eh	CAN0 Message Box 11: Time Stamp		XXh
0120h			XXh
0120h			XXh
012111			XXh
0122h	CAN0 Message Box 12: Identifier / DLC		XXh
0120h			XXh
0125h			XXh
0126h			XXh
0120H			XXh
0128h			XXh
0120h			XXh
0123h	CAN0 Message Box 12: Data Field		XXh
012Rh			XXh
012Ch			XXh
0120h			XXh
012Fh			XXh
012Fh	CAN0 Message Box 12: Time Stamp		XXh
0130h			XXh
0131h			XXh
0132h			XXh
0133h	CAN0 Message Box 13: Identifier / DLC		XXh
0134h			XXh
0135h			XXh
0136h			XXh
0137h			XXh
0138h			XXh
0139h			XXh
0134h	CAN0 Message Box 13: Data Field		XXh
013Bh			XXh
013Ch			XXh
013Dh			XXh
013Eh			XXh
013Eh	CAN0 Message Box 13: Time Stamp		XXh

X: Undefined



Table 4.12 SFR Information (12)

Address	Register	Symbol	After Reset
02C0h			XXh
02C1h			XXh
02C2h			XXh
02C3h	CAN1 Message Box 6: Identifier / DLC		XXh
02C4h			XXh
02C5h			XXh
0200h			XXh
02C011			XXh
020711			XXII XXb
02080			XXII XXb
02C9n	CAN1 Message Box 6: Data Field		
02CAh			XXII
02CBh			XXn
02CCh			XXn
02CDh			XXh
02CEh	CAN1 Message Box 6 ⁻ Time Stamp		XXh
02CFh			XXh
02D0h			XXh
02D1h			XXh
02D2h	CAN1 Massage Box 7: Identifier / DLC		XXh
02D3h	CANT Message box 7. Identifier / DEC		XXh
02D4h			XXh
02D5h			XXh
02D6h			XXh
02D7h			XXh
02D8h			XXh
02D9h			XXh
02DAh	CAN1 Message Box 7: Data Field		XXh
02DBh			XXh
02DCh			XXh
02DDh			XXh
02DEh			XXh
02DEh	CAN1 Message Box 7: Time Stamp		XXh
02E0h			XXh
02E1h			XXh
02E2h			XXh
02E3h	CAN1 Message Box 8: Identifier / DLC		XXh
02E4h			XXh
02E5h			XXh
02E6h			XXh
02E7h			XXh
02E8h			XXh
02E9h			XXh
02EAh	CAN1 Message Box 8: Data Field		XXh
02E8h			XXh
02EDh			XXh
02E0h			XXh
02ED11			XYh
02000	CAN1 Message Box 8: Time Stamp		XVh
02E0h			XXII XXb
02F011			XXII XXb
02F111			XXII XXb
	CAN1 Message Box 9: Identifier / DLC		
02F30			
02F4h			
02F50		1	
02F60			
02F/N			
02F8h			<u> </u>
02F9h	CAN1 Message Box 9: Data Field		<u> </u>
02FAh	-		<u> </u>
U2FBh			<u> </u>
U2FCh			<u> </u>
U2FDh		1	AXN VVL
U2FEN	CAN1 Message Box 9: Time Stamp		<u> </u>
02FFh	, i		XXh

X: Undefined



Table 5.4 Electrical Characteristics (1) (1)

Cumbol		Do	ramator	Manauring Condition	S	tandar	ď	Linit
Symbol		Pa	rameter	Measuring Condition	Min.	Тур.	Max.	Unit
Vон	HIGH output	P0_0 to P	0_7, P1_0 to P1_7, P2_0 to P2_7,	Іон = –5 mA	Vcc-2.0		Vcc	V
	voltage	P3_0 to P	3_7, P4_0 to P4_7, P5_0 to P5_7,					
		P6_0 to F	P6_7, P7_0, P7_2 to P7_7,					
		P8_0 to F	P8_4, P8_6, P8_7, P9_0,					
		P9_2 to F	P9_7, P10_0 to P10_7					
Vон	HIGH output	P0_0 to P	0_7, P1_0 to P1_7, P2_0 to P2_7,	Іон = –200 µА	Vcc-0.3		Vcc	V
	voltage	P3_0 to P	3_7, P4_0 to P4_7, P5_0 to P5_7,					
		P6_0 to F	P6_7, P7_0, P7_2 to P7_7,					
		P8_0 to F	P8_4, P8_6, P8_7, P9_0,					
		P9_2 to F	P9_7, P10_0 to P10_7					
Vон	HIGH output	XOUT	HIGHPOWER	Іон = —1 mA	3.0		Vcc	V
	voltage		LOWPOWER	Iон = -0.5 mA	3.0		Vcc	
	HIGH output	XCOUT	HIGHPOWER	With no load applied		2.5		V
	voltage		LOWPOWER	With no load applied		1.6		
Vol	LOW output	P0_0 to P	0_7, P1_0 to P1_7, P2_0 to P2_7,	lo∟ = 5 mA			2.0	V
	voltage	P3_0 to P	3_7, P4_0 to P4_7, P5_0 to P5_7,					
		P6_0 to P	6_7, P7_0 to P7_7, P8_0 to P8_4,					
		P8_6, P8_	_7, P9_0 to P9_7, P10_0 to P10_7					
Vol	LOW output	P0_0 to P	0_7, P1_0 to P1_7, P2_0 to P2_7,	loι = 200 μA			0.45	V
	voltage	P3_0 to P	3_7, P4_0 to P4_7, P5_0 to P5_7,					
		P6_0 to P	6_7, P7_0 to P7_7, P8_0 to P8_4,					
		P8_6, P8_	7, P9_0 to P9_7, P10_0 to P10_7					
Vol	LOW output	XOUT	HIGHPOWER	lo∟ = 1 mA			2.0	V
	voltage		LOWPOWER	lo∟ = 0.5 mA			2.0	1
	LOW output	XCOUT	HIGHPOWER	With no load applied		0		V
	voltage		LOWPOWER	With no load applied		0]
V⊤+-V⊤-	Hysteresis	HOLD, RD	Y, TAOIN to TA4IN, TB0IN to TB5IN,		0.2		1.0	V
		INTO to IN	T5, NMI, ADTRG, CTS0 to CTS2,					
		SCL0 to S	CL2, SDA0 to SDA2, CLK0 to CLK3,					
		TA0OUT	to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$,					
		RXD0 to	RXD2, SIN3					
V⊤+-V⊤-	Hysteresis	RESET			0.2		2.5	V
Ін	HIGH input	P0_0 to P	0_7, P1_0 to P1_7, P2_0 to P2_7,	$V_1 = 5 V$			5.0	μA
	current	P3_0 to P	3_7, P4_0 to P4_7, P5_0 to P5_7,					
		P6_0 to P	6_7, P7_0 to P7_7, P8_0 to P8_7,					
		P9_0 to P	9_7, P10_0 to P10_7,					
		XIN, RES	SET, CNVSS, BYTE					
lı∟	LOW input	P0_0 to P	0_7, P1_0 to P1_7, P2_0 to P2_7,	$V_{I} = 0 V$			-5.0	μA
	current	P3_0 to P	3_7, P4_0 to P4_7, P5_0 to P5_7,					
		P6_0 to P	6_7, P7_0 to P7_7, P8_0 to P8_7,					
		P9_0 to P	9_7, P10_0 to P10_7,					
		XIN, RES	SET, CNVSS, BYTE					
RPULLUP	Pull-up	P0_0 to P	0_7, P1_0 to P1_7, P2_0 to P2_7,	$V_I = 0 V$	30	50	170	kΩ
	resistance	P3_0 to P	3_7, P4_0 to P4_7, P5_0 to P5_7,					
		P6_0 to P	6_7, P7_0, P7_2 to P7_7, P8_0 to					
		P8_4, P8	_6, P8_7, P9_0, P9_2 to P9_7,					
		P10_0 to	P10_7					
Rfxin	Feedback resist	tance	XIN			1.5		MΩ
Rfxcin	Feedback resist	tance	XCIN			15		MΩ
VRAM	RAM retention v	voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V, VSS = 0 V at Topr = -40 to 85° C, f(BCLK) = 20 MHz unless otherwise specified.

Switching Characteristics

VCC = 5 V

Symbol	Parameter	Measuring	Standard		Linit
Symbol	Farameter	Condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time	Figure 5.2		25	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE signal output delay time			15	ns
th(BCLK-ALE)	ALE signal output hold time		-4		ns
td(BCLK-RD)	RD signal output delay time			25	ns
th(BCLK-RD)	RD signal output hold time		0		ns
td(BCLK-WR)	WR signal output delay time			25	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time			40	ns

Table 5.23 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

NOTES:

1. Calculated according to the BCLK frequency as follows:

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \text{ [ns]} \qquad f(BCLK) \text{ is 12.5 MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in $t = - CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is





Figure 5.2 Port P0 to P10 Measurement Circuit



Switching Characteristics VCC = 5 V(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Symbol	Parameter	Measuring	Standard		Linit
Symbol	Falameter	Condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time	Figure 5.2		25	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE signal output delay time			15	ns
th(BCLK-ALE)	ALE signal output hold time		-4		ns
td(BCLK-RD)	RD signal output delay time			25	ns
th(BCLK-RD)	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time]		40	ns

Table 5.24 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

2. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

 $t = -CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is





Figure 5.5 Timing Diagram (3)



Figure 5.7 Timing Diagram (5)

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Symbol	Parameter	Measuring	Standard		Linit
Symbol	Faranieter	Condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time	Figure 5.12		25	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE signal output delay time			15	ns
th(BCLK-ALE)	ALE signal output hold time		-4		ns
td(BCLK-RD)	RD signal output delay time			25	ns
th(BCLK-RD)	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time			40	ns

Table 5.48 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

NOTES:

1. Calculated according to the BCLK frequency as follows:

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \text{ [ns]} \qquad f(BCLK) \text{ is } 12.5 \text{ MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

 $t = -CR \times ln (1 - V_{OL} / V_{CC})$ by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is





Figure 5.12 Port P0 to P10 Measurement Circuit



Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Symbol	Doromotor	Measuring	Standard		Linit
Symbol	Falalletei	Condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time	Figure 5.12		25	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)]	(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time			40	ns

Table 5.49 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

2. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

 $t = -CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is





Figure 5.15 Timing Diagram (3)



Figure 5.19 Timing Diagram (7)



Figure 5.20 Timing Diagram (8)

Timing Requirements VCC = 3.3 V (Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)

Table 5.60 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Stan	Linit	
		Min.	Max.	Unit
tc(TB)	TBiIN input cycle time (counted on one edge)	150		ns
tw(TBH)	TBiIN input HIGH pulse width (counted on one edge)	60		ns
tw(TBL)	TBiIN input LOW pulse width (counted on one edge)	60		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	300		ns
tw(TBH)	TBiIN input HIGH pulse width (counted on both edges)	120		ns
tw(TBL)	TBiIN input LOW pulse width (counted on both edges)	120		ns

Table 5.61 Timer B Input (Pulse Period Measurement Mode)

Symbol	Symbol Parameter	Standard		Linit
Symbol		Min.	Max.	Unit
t _{c(TB)}	TBiIN input cycle time	600		ns
tw(TBH)	TBiIN input HIGH pulse width	300		ns
tw(TBL)	TBiIN input LOW pulse width	300		ns

Table 5.62 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Linit
		Min.	Max.	
tc(TB)	TBiIN input cycle time	600		ns
t _{w(TBH)}	TBIIN input HIGH pulse width	300		ns
tw(TBL)	TBiIN input LOW pulse width	300		ns

Table 5.63 A/D Trigger Input

Symbol	Parameter	Standard		Linit
		Min.	Max.	Unit
tc(AD)	ADTRG input cycle time (trigger able minimum)	1500		ns
tw(ADL)	ADTRG input LOW pulse width	200		ns

Table 5.64 Serial Interface

Symbol	Parameter	Standard		Linit
		Min.	Max.	Unit
tc(CK)	CLKi input cycle time	300		ns
t _{w(CKH)}	CLKi input HIGH pulse width	150		ns
tw(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TXDi output delay time		160	ns
th(C-Q)	TXDi hold time	0		ns
tsu(D-C)	RXDi input setup time	100		ns
th(C-D)	RXDi input hold time	90		ns

Table 5.65 External Interrupt INTi Input

Symbol	Parameter	Standard		Linit
		Min.	Max.	Unit
t _{w(INH)}	INTi input HIGH pulse width	380		ns
tw(INL)	INTi input LOW pulse width	380		ns



Figure 5.24 Timing Diagram (3)



Figure 5.25 Timing Diagram (4)



Figure 5.28 Timing Diagram (7)

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