E. Renesas Electronics America Inc - M306N4MGT-151FPUSQ Datasheet



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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	87
Program Memory Size	256КВ (256К х 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10К х 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306n4mgt-151fpusq

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1.3 Block Diagram

Figure 1.1 shows a Block Diagram.



Figure 1.1 Block Diagram



Table 1.4 List of Pin Names (2)

Pin	No.	Control	Port	Interrupt	Timor Pin		Analog	CAN Module	Rue Control Din
FP	GP	Pin	FUIL	Pin		UANTEIII	Pin	Pin	Bus Control Fill
51	49		P4_3						A19
52	50		P4_2						A18
53	51		P4_1						A17
54	52		P4_0						A16
55	53		P3_7						A15
56	54		P3 6						A14
57	55		P3 5						A13
58	56		P3 4						A12
59	57		P3 3						A11
60	58		P3 2						A10
61	59		P3 1						A9
62	60	VCC2							
63	61	1002	P3 0						A8(/-/D7)
64	62	VSS							10(, 121)
65	63		P2 7				AN2 7		A7(/D7/D6)
66	64		P2 6				AN2 6		A6(/D6/D5)
67	65		P2 5				$\Delta N_2 5$		A5(/D5/D4)
68	66		P2 /				AN2 4		A3(/D3/D4)
60	67		D2 3				AN2 3		A4(/D4/D3)
70	60		FZ_3				AN2_3		A3(/D3/D2)
70	60		FZ_Z				ANZ_Z		A2(/D2/D1)
	09 70		P2_1				AN2_1		A1(/D1/D0)
72	70		P2_0	INITE			AN2_0		AU(/DU/-)
73	/1		PI_/						DI5
/4	72		P1_6						D14
75	73		P1_5	IN13					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7				AN0_7		D7
82	80		P0_6				AN0_6		D6
83	81		P0_5				AN0_5		D5
84	82		P0_4				AN0_4		D4
85	83		P0_3				AN0_3		D3
86	84		P0_2				AN0_2		D2
87	85		P0_1				AN0_1		D1
88	86		P0_0				AN0_0		D0
89	87		P10_7	KI3			AN7		
90	88		P10_6	KI2			AN6		
91	89		P10_5	KI1			AN5		
92	90		P10_4	KI0			AN4		
93	91		P10_3				AN3		
94	92		P10_2				AN2		
95	93		P10_1				AN1		
96	94	AVSS							
97	95		P10_0				AN0		
98	96	VREF							
99	97	AVCC							
100	98		P9 7				ADTRG		
	- -	I	<u> </u>	I				L	

FP: PRQP0100JB-A (100P6S-A), GP: PLQP0100KB-A (100P6Q-A)



2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits. Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt. Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

2.8.10 Reserved Area

When white to this bit, write 0. When read, its content is undefined.

Table 4.8 SFR Information (8) ⁽¹⁾

Address	Register	Symbol	After Reset
01C0h	Timer B3, B4, B5 Count Start Flag	TBSR	000XXXXXb
01C1h			
01C2h	The Add Devider	TAIL	XXh
01C3h	Timer AT-T Register	IAII	XXh
01C4h	Timer 40.1 Desister	TAO1	XXh
01C5h	Timer Az-T Register	TAZT	XXh
01C6h	Timer A4.1 Decistor	TA 41	XXh
01C7h		1A41	XXh
01C8h	Three-Phase PWM Control Register 0	INVC0	00h
01C9h	Three-Phase PWM Control Register 1	INVC1	00h
01CAh	Three-Phase Output Buffer Register 0	IDB0	00111111b
01CBh	Three-Phase Output Buffer Register 1	IDB1	00111111b
01CCh	Dead Time Timer	DTT	XXh
01CDh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
01CEh			
01CFh			
01D0h	Timer B3 Register	твз	XXh
01D1h	·······		XXh
01D2h	Timer B4 Register	TB4	XXh
01D3h	5		XXh
01D4h	Timer B5 Register	TB5	XXh
01D5h			xXn
01D6h			
01D/h			
01D8h			
01D9h			
01DAII	Timer B3 Mode Register	TB3MB	00XX0000b
01DDh	Timer B4 Mode Register	TB4MR	00XX0000b
	Timer B5 Mode Register	TB5MB	00XX0000b
01DEh	Interrupt Source Select Begister 0	IESB0	00XXX000b
01DEh	Interrupt Source Select Register 1	IFSB1	00h
01E0h	SI/O3 Transmit/Receive Register	S3TRR	XXh
01E1h			
01E2h	SI/O3 Control Register	S3C	0100000b
01E3h	SI/O3 Bit Rate Register	S3BRG	XXh
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh	UARTO Special Mode Register 4	U0SMR4	00h
01EDh	UARI0 Special Mode Register 3	U0SMR3	000X0X0Xb
01EEh	UARTU Special Mode Register 2	U0SMR2	X000000b
01EFh	UARTU Special Mode Register	UUSMR	X000000b
01F0h	UARTI Special Mode Register 4	U1SMR4	
01F1h	UARTI Special Mode Register 3		VOODCOCK
01F2h	UARTI Special Mode Register 2		
01530	UART I Special Node Register		
01F40	UART2 Special Mode Register 2		000202026
01566	UART2 Special Mode Register 2		X000000h
01F01	UART2 Special Mode Register		X0000000
01E8h	UART2 Transmit/Receive Mode Register	U2MB	00h
01FQh	LIART2 Rit Bate Benister	U2BBG	χχh
01FAh			XXh
01FBh	UART2 Transmit Buffer Register	U2TB	XXh
01FCh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
01FDh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
01FEh			XXh
01FFh		U2RB	XXh

X: Undefined

NOTE:

1. Blank spaces are reserved. No access is allowed.



Timing Requirements VCC = 5 V(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)

Table 5.9 External Clock Input (XIN Input)

Symbol Parameter tc External clock input cycle time tw(H) External clock input HIGH pulse width tw(L) External clock input LOW pulse width	Baramatar	Stan	Linit	
	Falailletei	Min.	Max.	Unit
tc	External clock input cycle time	62.5		ns
tw(H)	External clock input HIGH pulse width	25		ns
tw(L)	External clock input LOW pulse width	25		ns
tr	External clock rise time		15	ns
tr	External clock fall time		15	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Doromotor	Standard		Lloit
Symbol	Farameter	Min.	Max.	Unit
tac1(RD-DB)	Data input access time (for setting with no wait)		(NOTE 1)	ns
tac2(RD-DB)	Data input access time (for setting with wait)		(NOTE 2)	ns
tac3(RD-DB)	Data input access time (when accessing multiplexed bus area)		(NOTE 3)	ns
tsu(DB-RD)	Data input setup time	40		ns
tsu(RDY-BCLK)	RDY input setup time	30		ns
tsu(HOLD-BCLK)	HOLD input setup time	40		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK-RDY)	RDY input hold time	0		ns
th(BCLK-HOLD)	HOLD input hold time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45 [ns]$$

2. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 \text{ [ns]}$ n is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 \text{ [ns]} \qquad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

Switching Characteristics VCC = 5 V(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Symbol	Baramotor	Measuring	Stan	dard	Linit
Symbol	Falameter	Condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time	Figure 5.2		25	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE signal output delay time			15	ns
th(BCLK-ALE)	ALE signal output hold time		-4		ns
td(BCLK-RD)	RD signal output delay time			25	ns
th(BCLK-RD)	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time]		40	ns

Table 5.24 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

2. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

 $t = -CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is





Figure 5.5 Timing Diagram (3)



Figure 5.7 Timing Diagram (5)



Figure 5.9 Timing Diagram (7)

5.2 Electrical Characteristics (Normal-ver.)

Symbol			Parameter	Condition	Rated Value	Unit
Vcc	Supply voltage (VCC1 = VCC2)			VCC = AVCC	-0.3 to 6.5	V
AVcc	Analog su	pply volta	age	VCC = AVCC	-0.3 to 6.5	V
Vi	Input	RESET,	CNVSS, BYTE,		-0.3 to VCC+0.3	V
	voltage	P0_0 to	P0_7, P1_0 to P1_7, P2_0 to P2_7,			
		P3_0 to	P3_7, P4_0 to P4_7, P5_0 to P5_7,			
		P6_0 to F	P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7,			
		P9_0, P	9_2 to P9_7, P10_0 to P10_7,			
		VREF, >	(IN			
		P7_1, P	9_1		-0.3 to 6.5	V
Vo	Output	P0_0 to	P0_7, P1_0 to P1_7, P2_0 to P2_7,		-0.3 to VCC+0.3	V
	voltage	P3_0 to	P3_7, P4_0 to P4_7, P5_0 to P5_7,			
		P6_0 to	P6_7, P7_0, P7_2 to P7_7,			
		P8_0 to I	P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7,			
	P10_0		o P10_7, XOUT			
		P7_1, P	9_1		-0.3 to 6.5	V
Pd	Power dis	sipation		Topr = 25°C	700	mW
Topr	Operating	ambient	During MCU operation		-40 to 85	°C
	temperature		During flash memory program and		0 to 60	
			erase operation			
Tstg	Storage te	emperatu	re		-65 to 150	°C

Table 5.26 Absolute Maximum Ratings



Timing Requirements VCC = 5 V(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)

Table 5.36 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Baramatar	Stan	- Unit	
Symbol	Farameter	Standard Min. Max. 100 40 40 40		
tc(TA)	TAIIN input cycle time	100		ns
tw(TAH)	TAIIN input HIGH pulse width	40		ns
tw(TAL)	TAiIN input LOW pulse width	40		ns

Table 5.37 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Stan	Linit	
Symbol	Farameter	Min.	Max.	Unit
tc(TA)	TAilN input cycle time	400		ns
tw(TAH)	TAIIN input HIGH pulse width	200		ns
tw(TAL)	TAilN input LOW pulse width	200		ns

Table 5.38 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Stan	Linit	
Symbol	Parameter		Standard Uni Min. Max. 200 ns 100 ns 100 ns	Unit
tc(TA)	TAIIN input cycle time	200		ns
tw(TAH)	TAIIN input HIGH pulse width	100		ns
tw(TAL)	TAIIN input LOW pulse width	100		ns

Table 5.39 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Dorometer		Standard		
Symbol	Falameter	StandardMin.Max.100100	Max.	Unit	
tw(TAH)	TAIIN input HIGH pulse width	100		ns	
tw(TAL)	TAIIN input LOW pulse width	100		ns	

Table 5.40 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Devemeter	Stan	Linit	
	Falameter	Min.	Max.	Unit
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input HIGH pulse width	1000		ns
tw(UPL)	TAiOUT input LOW pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

Table 5.41 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol Parameter	Parameter	Standard		Lloit
	Falailletei	Min.	Max.	
t _{c(TA)}	TAIIN input cycle rime	800		ns
tsu(tain-taout)	TAiOUT input setup time	200		ns
tsu(taout-tain)	TAIIN input setup time	200		ns

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Symbol	Parameter	Measuring	Standard		Lloit
Symbol		Condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time	Figure 5.12		25	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)]	(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time			40	ns

Table 5.49 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

2. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

 $t = -CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is





Figure 5.17 Timing Diagram (5)

Timing Requirements VCC = 3.3 V (Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)

Table 5.54 Timer A Input (Counter Input in Event Counter Mode)

Symbol Parameter	Dorometer	Stan	Linit	
	Farameter	Min.	Max.	
tc(TA)	TAIIN input cycle time	150		ns
tw(TAH)	TAIIN input HIGH pulse width	60		ns
tw(TAL)	TAiIN input LOW pulse width	60		ns

Table 5.55 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Linit
		Min.	Max.	
tc(TA)	TAilN input cycle time	600		ns
tw(TAH)	TAiIN input HIGH pulse width	300		ns
tw(TAL)	TAilN input LOW pulse width	300		ns

Table 5.56 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol Parameter	Devemeter	Standard		Unit
	Min.	Max.		
tc(TA)	TAIIN input cycle time	300		ns
tw(TAH)	TAIIN input HIGH pulse width	150		ns
tw(TAL)	TAIIN input LOW pulse width	150		ns

Table 5.57 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Cumbol	Symbol Parameter	Standard		Linit
Symbol		Min.	Max.	Unit
tw(TAH)	TAIIN input HIGH pulse width	150		ns
tw(TAL)	TAIIN input LOW pulse width	150		ns

Table 5.58 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Cumbal	Darameter	Stan	Linit	
Symbol	Falameter	Min.	Max.	Unit
tc(UP)	TAiOUT input cycle time	3000		ns
tw(UPH)	TAiOUT input HIGH pulse width	1500		ns
tw(UPL)	TAiOUT input LOW pulse width	1500		ns
tsu(UP-TIN)	TAiOUT input setup time	600		ns
th(TIN-UP)	TAiOUT input hold time	600		ns

Table 5.59 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol Parameter	Parametar	Standard		Lloit
	Falailletei	Min.	Max.	
tc(TA)	TAIIN input cycle time	2		μs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		ns
tsu(TAOUT-TAIN)	TAIIN input setup time	500		ns

Switching Characteristics

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Symbol	Parameter	Measuring	Standard		Linit
Symbol	Faranieler	Condition	Min.	Max.	
td(BCLK-AD)	Address output delay time	Figure 5.21		30	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
th(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
td(BCLK-CS)	Chip select output delay time			30	ns
th(BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
td(BCLK-ALE)	ALE signal output delay time			25	ns
th(BCLK-ALE)	ALE signal output hold time		-4		ns
td(BCLK-RD)	RD signal output delay time			30	ns
th(BCLK-RD)	RD signal output hold time		0		ns
td(BCLK-WR)	WR signal output delay time			30	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
td(DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)]	(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time]		40	ns

Table 5.66 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)

NOTES:

1. Calculated according to the BCLK frequency as follows:

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \text{ [ns]} \qquad f(BCLK) \text{ is } 12.5 \text{ MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in $t = - CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is





Figure 5.21 Port P0 to P10 Measurement Circuit



Switching Characteristics

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = -40 to 85 °C unless otherwise specified)

Symbol	Parameter	Measuring	Standard		Lloit
Symbol	i alametei	Condition	Min.	Max.	
td(BCLK-AD)	Address output delay time	Figure 5.21		30	ns
th(BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
t h(RD-AD)	Address output hold time (in relation to RD)		0		ns
th(WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
th(BCLK-DB)	Data output hold time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
th(WR-DB)	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
td(BCLK-HLDA)	HLDA output delay time			40	ns

Table 5.67 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

2. Calculated according to the BCLK frequency as follows:

 $\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

 $t = -CR \times ln (1 - V_{OL} / V_{CC})$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, C = 30 pF,

R =1 k Ω , hold time of output "L" level is



Memory Expansion Mode and Microprocessor Mode (Effective for setting with wait)	VCC = 3.3 V
BCLK RD (Separate bus) WR, WRL, WRH (Separate bus) RD (Multiplexed bus) WR, WRL, WRH	
RDY input	
(Common to setting with wait and setting without wait)	
HOLD input	
HLDA output	
P0, P1, P2, td(BCLK-HLDA) td(BCLK-HLDA) P3, P4, Hi–Z Hi–Z (
NOTE: 1. The above pins are set to high-impedance regardless of the input level of the E the PM06 bit in the PM0 register, and the PM11 bit in the PM1 register.	3YTE pin,
Measuring conditions : • VCC = 3.3 V • Input timing voltage : Determined with V _{IL} = 0.6 V , V _{IH} = 2.7 V • Output timing voltage: Determined with V _{OL} = 1.65 V , V _{OH} = 1.65 V	

Figure 5.23 Timing Diagram (2)



Figure 5.27 Timing Diagram (6)



Figure 5.29 Timing Diagram (8)

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