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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306n4mgt-158fpuf1

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

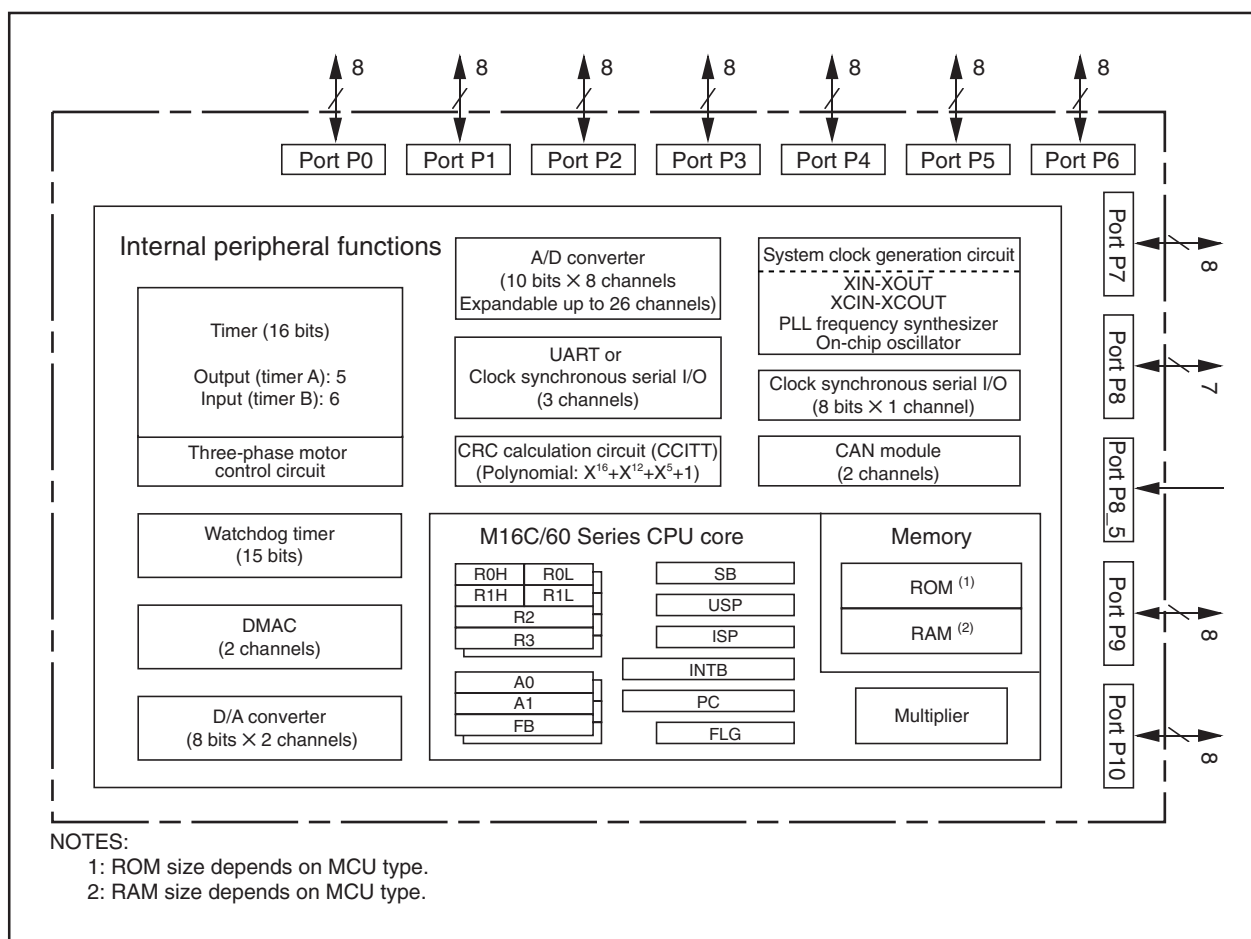


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the Product Information and Figure 1.2 shows the Type Number, Memory Size, and Packages.

Table 1.2 Product Information

As of Aug. 2006

Type No.	ROM Capacity	RAM Capacity	Package Type ⁽²⁾	Remarks	
M306N4FCFP	128 K + 4 Kbytes	5 Kbytes	PRQP0100JB-A	Flash memory version ⁽¹⁾	Normal-ver.
M306N4FCGP			PLQP0100KB-A		
M306N4FGFP	256 K + 4 Kbytes	10 Kbytes	PRQP0100JB-A		T-ver.
M306N4FGGP			PLQP0100KB-A		
M306N4FCTFP	128 K + 4 Kbytes	5 Kbytes	PRQP0100JB-A		V-ver.
M306N4FCTGP			PLQP0100KB-A		
M306N4FGTFP	256 K + 4 Kbytes	10 Kbytes	PRQP0100JB-A		
M306N4FGTGP			PLQP0100KB-A		
M306N4FCVFP	128 K + 4 Kbytes	5 Kbytes	PRQP0100JB-A	Mask ROM version	Normal-ver.
M306N4FCVGP			PLQP0100KB-A		
M306N4FGVFP	256 K + 4 Kbytes	10 Kbytes	PRQP0100JB-A		T-ver.
M306N4FGVGP			PLQP0100KB-A		
M306N4MC-XXXGP	128 Kbytes	5 Kbytes	PLQP0100KB-A		
M306N4MG-XXXGP	256 Kbytes	10 Kbytes	PLQP0100KB-A		
M306N4MCT-XXXFP	128 Kbytes	5 Kbytes	PRQP0100JB-A		V-ver.
M306N4MCT-XXXGP			PLQP0100KB-A		
M306N4MGT-XXXFP	256 Kbytes	10 Kbytes	PRQP0100JB-A		
M306N4MGT-XXXGP			PLQP0100KB-A		
M306N4MCV-XXXFP	128 Kbytes	5 Kbytes	PRQP0100JB-A		
M306N4MCV-XXXGP (D)			PLQP0100KB-A		
M306N4MGV-XXXFP	256 Kbytes	10 Kbytes	PRQP0100JB-A		
M306N4MGV-XXXGP (D)			PLQP0100KB-A		

(D): Under development

NOTES:

1. Data flash memory provides an additional 4 Kbytes of ROM capacity (block A).
2. The correspondence between new and old package types is as follows.

PRQP0100JB-A: 100P6S-A

PLQP0100KB-A: 100P6Q-A

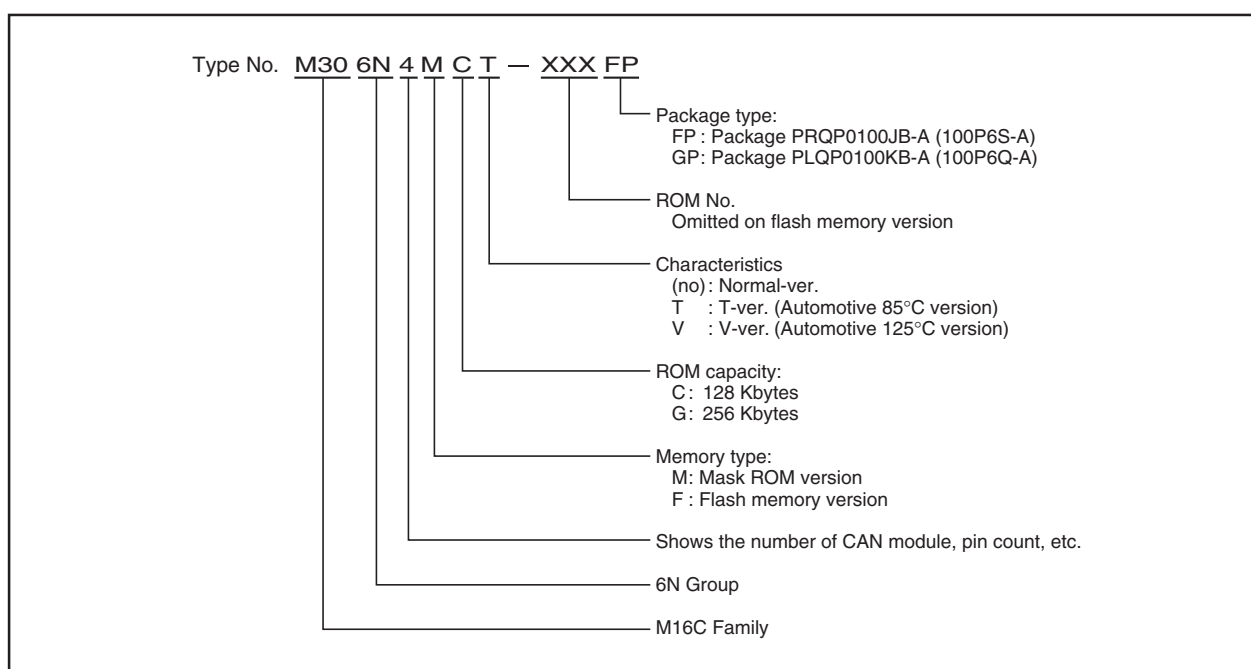


Figure 1.2 Type Number, Memory Size, and Package

Table 1.4 List of Pin Names (2)

Pin No.		Control	Port	Interrupt	Timer Pin	UART Pin	Analog	CAN Module	Bus Control Pin
FP	GP	Pin		Pin			Pin	Pin	
51	49		P4_3						A19
52	50		P4_2						A18
53	51		P4_1						A17
54	52		P4_0						A16
55	53		P3_7						A15
56	54		P3_6						A14
57	55		P3_5						A13
58	56		P3_4						A12
59	57		P3_3						A11
60	58		P3_2						A10
61	59		P3_1						A9
62	60	VCC2							
63	61		P3_0						A8(/-/D7)
64	62	VSS							
65	63		P2_7				AN2_7		A7(/D7/D6)
66	64		P2_6				AN2_6		A6(/D6/D5)
67	65		P2_5				AN2_5		A5(/D5/D4)
68	66		P2_4				AN2_4		A4(/D4/D3)
69	67		P2_3				AN2_3		A3(/D3/D2)
70	68		P2_2				AN2_2		A2(/D2/D1)
71	69		P2_1				AN2_1		A1(/D1/D0)
72	70		P2_0				AN2_0		A0(/D0/-)
73	71		P1_7	INT5					D15
74	72		P1_6	INT4					D14
75	73		P1_5	INT3					D13
76	74		P1_4						D12
77	75		P1_3						D11
78	76		P1_2						D10
79	77		P1_1						D9
80	78		P1_0						D8
81	79		P0_7				AN0_7		D7
82	80		P0_6				AN0_6		D6
83	81		P0_5				AN0_5		D5
84	82		P0_4				AN0_4		D4
85	83		P0_3				AN0_3		D3
86	84		P0_2				AN0_2		D2
87	85		P0_1				AN0_1		D1
88	86		P0_0				AN0_0		D0
89	87		P10_7	KI3			AN7		
90	88		P10_6	KI2			AN6		
91	89		P10_5	KI1			AN5		
92	90		P10_4	KI0			AN4		
93	91		P10_3				AN3		
94	92		P10_2				AN2		
95	93		P10_1				AN1		
96	94	AVSS							
97	95		P10_0				AN0		
98	96	VREF							
99	97	AVCC							
100	98		P9_7				ADTRG		

FP: PRQP0100JB-A (100P6S-A), GP: PLQP0100KB-A (100P6Q-A)

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h	CAN0 Message Box 14: Identifier /DLC		XXh
0141h			XXh
0142h			XXh
0143h			XXh
0144h			XXh
0145h			XXh
0146h	CAN0 Message Box 14: Data Field		XXh
0147h			XXh
0148h			XXh
0149h			XXh
014Ah			XXh
014Bh			XXh
014Ch			XXh
014Dh			XXh
014Eh	CAN0 Message Box 14: Time Stamp		XXh
014Fh			XXh
0150h	CAN0 Message Box 15: Identifier /DLC		XXh
0151h			XXh
0152h			XXh
0153h			XXh
0154h			XXh
0155h			XXh
0156h	CAN0 Message Box 15: Data Field		XXh
0157h			XXh
0158h			XXh
0159h			XXh
015Ah			XXh
015Bh			XXh
015Ch			XXh
015Dh			XXh
015Eh	CAN0 Message Box 15: Time Stamp		XXh
015Fh			XXh
0160h	CAN0 Global Mask Register	C0GMR	XXh
0161h			XXh
0162h			XXh
0163h			XXh
0164h			XXh
0165h			XXh
0166h	CAN0 Local Mask A Register	C0LMAR	XXh
0167h			XXh
0168h			XXh
0169h			XXh
016Ah			XXh
016Bh			XXh
016Ch	CAN0 Local Mask B Register	C0LMBR	XXh
016Dh			XXh
016Eh			XXh
016Fh			XXh
0170h			XXh
0171h			XXh
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

- Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information (11)

Address	Register	Symbol	After Reset
0280h	CAN1 Message Box 2: Identifier / DLC		XXh
0281h			XXh
0282h			XXh
0283h			XXh
0284h			XXh
0285h			XXh
0286h	CAN1 Message Box 2: Data Field		XXh
0287h			XXh
0288h			XXh
0289h			XXh
028Ah			XXh
028Bh			XXh
028Ch			XXh
028Dh			XXh
028Eh	CAN1 Message Box 2: Time Stamp		XXh
028Fh			XXh
0290h	CAN1 Message Box 3: Identifier / DLC		XXh
0291h			XXh
0292h			XXh
0293h			XXh
0294h			XXh
0295h			XXh
0296h	CAN1 Message Box 3: Data Field		XXh
0297h			XXh
0298h			XXh
0299h			XXh
029Ah			XXh
029Bh			XXh
029Ch			XXh
029Dh			XXh
029Eh	CAN1 Message Box 3: Time Stamp		XXh
029Fh			XXh
02A0h	CAN1 Message Box 4: Identifier / DLC		XXh
02A1h			XXh
02A2h			XXh
02A3h			XXh
02A4h			XXh
02A5h			XXh
02A6h	CAN1 Message Box 4: Data Field		XXh
02A7h			XXh
02A8h			XXh
02A9h			XXh
02AAh			XXh
02ABh			XXh
02ACh			XXh
02ADh			XXh
02AEh	CAN1 Message Box 4: Time Stamp		XXh
02AFh			XXh
02B0h	CAN1 Message Box 5: Identifier / DLC		XXh
02B1h			XXh
02B2h			XXh
02B3h			XXh
02B4h			XXh
02B5h			XXh
02B6h	CAN1 Message Box 5: Data Field		XXh
02B7h			XXh
02B8h			XXh
02B9h			XXh
02BAh			XXh
02BBh			XXh
02BCh			XXh
02BDh			XXh
02BEh	CAN1 Message Box 5: Time Stamp		XXh
02BFh			XXh

X: Undefined

Table 4.13 SFR Information (13)

Address	Register	Symbol	After Reset
0300h	CAN1 Message Box 10: Identifier / DLC		XXh
0301h			XXh
0302h			XXh
0303h			XXh
0304h			XXh
0305h	CAN1 Message Box 10: Data Field		XXh
0306h			XXh
0307h			XXh
0308h			XXh
0309h			XXh
030Ah			XXh
030Bh			XXh
030Ch	CAN1 Message Box 10: Time Stamp		XXh
030Dh			XXh
030Eh	CAN1 Message Box 11: Identifier / DLC		XXh
030Fh			XXh
0310h			XXh
0311h			XXh
0312h			XXh
0313h	CAN1 Message Box 11: Data Field		XXh
0314h			XXh
0315h			XXh
0316h			XXh
0317h			XXh
0318h			XXh
0319h			XXh
031Ah	CAN1 Message Box 11: Time Stamp		XXh
031Bh			XXh
031Ch	CAN1 Message Box 12: Identifier / DLC		XXh
031Dh			XXh
031Eh			XXh
031Fh			XXh
0320h			XXh
0321h	CAN1 Message Box 12: Data Field		XXh
0322h			XXh
0323h			XXh
0324h			XXh
0325h			XXh
0326h			XXh
0327h			XXh
0328h	CAN1 Message Box 12: Time Stamp		XXh
0329h			XXh
032Ah	CAN1 Message Box 13: Identifier / DLC		XXh
032Bh			XXh
032Ch			XXh
032Dh			XXh
032Eh			XXh
032Fh	CAN1 Message Box 13: Data Field		XXh
0330h			XXh
0331h			XXh
0332h			XXh
0333h			XXh
0334h			XXh
0335h			XXh
0336h	CAN1 Message Box 13: Time Stamp		XXh
0337h			XXh
0338h	CAN1 Message Box 13: Data Field		XXh
0339h			XXh
033Ah			XXh
033Bh			XXh
033Ch			XXh
033Dh	CAN1 Message Box 13: Time Stamp		XXh
033Eh			XXh
033Fh			XXh

X: Undefined

Table 4.15 SFR Information (15) ⁽²⁾

Address	Register	Symbol	After Reset
0380h	Count Start Flag	TABSR	00h
0381h	Clock Prescaler Reset Flag	CPSRF	0XXXXXXb
0382h	One-Shot Start Flag	ONSF	00h
0383h	Trigger Select Register	TRGSR	00h
0384h	Up/Down Flag	UDF	00h ⁽¹⁾
0385h			
0386h	Timer A0 Register	TA0	XXh
0387h			XXh
0388h	Timer A1 Register	TA1	XXh
0389h			XXh
038Ah	Timer A2 Register	TA2	XXh
038Bh			XXh
038Ch	Timer A3 Register	TA3	XXh
038Dh			XXh
038Eh	Timer A4 Register	TA4	XXh
038Fh			XXh
0390h	Timer B0 Register	TB0	XXh
0391h			XXh
0392h	Timer B1 Register	TB1	XXh
0393h			XXh
0394h	Timer B2 Register	TB2	XXh
0395h			XXh
0396h	Timer A0 Mode Register	TA0MR	00h
0397h	Timer A1 Mode Register	TA1MR	00h
0398h	Timer A2 Mode Register	TA2MR	00h
0399h	Timer A3 Mode Register	TA3MR	00h
039Ah	Timer A4 Mode Register	TA4MR	00h
039Bh	Timer B0 Mode Register	TB0MR	00XX0000b
039Ch	Timer B1 Mode Register	TB1MR	00XX0000b
039Dh	Timer B2 Mode Register	TB2MR	00XX0000b
039Eh	Timer B2 Special Mode Register	TB2SC	XXXXXX00b
039Fh			
03A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
03A1h	UART0 Bit Rate Register	U0BRG	XXh
03A2h	UART0 Transmit Buffer Register	U0TB	XXh
03A3h			XXh
03A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
03A5h	UART0 Transmit/Receive Control Register 1	U0C1	00XX0010b
03A6h	UART0 Receive Buffer Register	U0RB	XXh
03A7h			XXh
03A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
03A9h	UART1 Bit Rate Register	U1BRG	XXh
03AAh	UART1 Transmit Buffer Register	U1TB	XXh
03ABh			XXh
03ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
03ADh	UART1 Transmit/Receive Control Register 1	U1C1	00XX0010b
03AEh	UART1 Receive Buffer Register	U1RB	XXh
03AFh			XXh
03B0h	UART Transmit/Receive Control Register 2	UCON	X0000000b
03B1h			
03B2h			
03B3h			
03B4h			
03B5h			
03B6h			
03B7h			
03B8h	DMA0 Request Source Select Register	DM0SL	00h
03B9h			
03BAh	DMA1 Request Source Select Register	DM1SL	00h
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

NOTES:

1. Bits TA2P to TA4P in the UDF register are set to 0 after reset. However, the contents in these bits are undefined when read.
2. Blank spaces are reserved. No access is allowed.

Table 5.3 Recommended Operating Conditions (2) ⁽¹⁾

Symbol	Parameter				Standard			Unit
					Min.	Typ.	Max.	
f(XIN)	Main clock input oscillation frequency ^{(2) (3) (4)}	No wait	Mask ROM version Flash memory version	VCC = 4.2 to 5.5 V	0		16	MHz
f(XCIN)	Sub clock oscillation frequency					32.768	50	kHz
f(Ring)	On-chip oscillation frequency					1		MHz
f(PLL)	PLL clock oscillation frequency				16		20	MHz
f(BCLK)	CPU operation clock			VCC = 4.2 to 5.5 V	0		20	MHz
t _{su} (PLL)	PLL frequency synthesizer stabilization wait time						20	ms

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V at Topr = -40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency and supply voltage is shown right.
3. Execute program/erase of flash memory by VCC = 5.0 ± 0.5 V.
4. When using over 16 MHz, use PLL clock. PLL clock oscillation frequency which can be used is 16 MHz or 20 MHz.

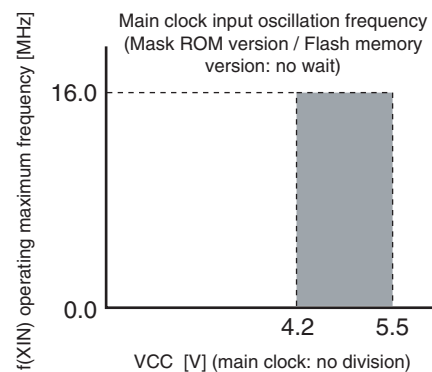


Table 5.6 A/D Conversion Characteristics ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		VREF = VCC				10	Bit
INL	Integral nonlinearity error	10 bits	VREF = VCC	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
			= 5 V	External operation amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 5 V				±2	LSB
—	Absolute accuracy	10 bits	VREF = VCC	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
			= 5 V	External operation amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 5 V				±2	LSB
DNL	Differential nonlinearity error						±1	LSB
—	Offset error						±3	LSB
—	Gain error						±3	LSB
R _{LADDER}	Resistor ladder		VREF = VCC		10		40	kΩ
t _{CONV}	10-bit conversion time, sample & hold available		VREF = VCC = 5 V, φ _{AD} = 10 MHz		3.3			μs
	8-bit conversion time, sample & hold available		VREF = VCC = 5 V, φ _{AD} = 10 MHz		2.8			μs
t _{SAMP}	Sampling time				0.3			μs
V _{REF}	Reference voltage				2.0		V _{CC}	V
V _{IA}	Analog input voltage				0		V _{REF}	V

NOTES:

1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, -40 to 85°C unless otherwise specified.
2. φ_{AD} frequency must be 10 MHz or less.
3. When sample & hold is disabled, φ_{AD} frequency must be 250kHz or more in addition to a limit of NOTE 2.
When sample & hold is enabled, φ_{AD} frequency must be 1MHz or more in addition to a limit of NOTE 2.

Table 5.7 D/A conversion Characteristics ⁽¹⁾

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
t _{su}	Setup time				3	μs
R _o	Output resistance		4	10	20	kΩ
I _{VREF}	Reference power supply input current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, -40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the DAi register (i = 0, 1) for the unused D/A converter set to 00h.
The resistor ladder of the A/D converter is not included. Also, the I_{VREF} will flow even if VREF is disconnected by the ADCON1 register.

Switching Characteristics**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.24 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 5.2		25	ns
t _h (BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (in relation to RD)		0		ns
t _h (WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip select output delay time			25	ns
t _h (BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
t _d (BCLK-ALE)	ALE signal output delay time			15	ns
t _h (BCLK-ALE)	ALE signal output hold time		–4		ns
t _d (BCLK-RD)	RD signal output delay time			25	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			25	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (in relation to BCLK) ⁽³⁾		4		ns
t _d (DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data output hold time (in relation to WR) ⁽³⁾		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

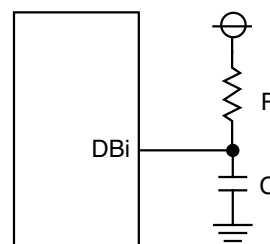
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, $C = 30 \text{ pF}$,

$R = 1 \text{ k}\Omega$, hold time of output “L” level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$



Switching Characteristics**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.25 Memory Expansion Mode and Microprocessor Mode
(for 2- to 3-wait setting, external area access and multiplexed bus selection)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 5.2		25	ns
t _h (BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (in relation to RD)		(NOTE 1)		ns
t _h (WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip select output delay time			25	ns
t _h (BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
t _h (RD-CS)	Chip select output hold time (in relation to RD)		(NOTE 1)		ns
t _h (WR-CS)	Chip select output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-RD)	RD signal output delay time			25	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			25	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (in relation to BCLK)		4		ns
t _d (DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA output delay time			40	ns
t _d (BCLK-ALE)	ALE signal output delay time (in relation to BCLK)			15	ns
t _h (BCLK-ALE)	ALE signal output hold time (in relation to BCLK)		–4		ns
t _d (AD-ALE)	ALE signal output delay time (in relation to Address)		(NOTE 3)		ns
t _h (ALE-AD)	ALE signal output hold time (in relation to Address)		(NOTE 4)		ns
t _d (AD-RD)	RD signal output delay from the end of Address		0		ns
t _d (AD-WR)	WR signal output delay from the end of Address		0		ns
t _{dZ} (RD-AD)	Address output floating start time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 25 \text{ [ns]}$$

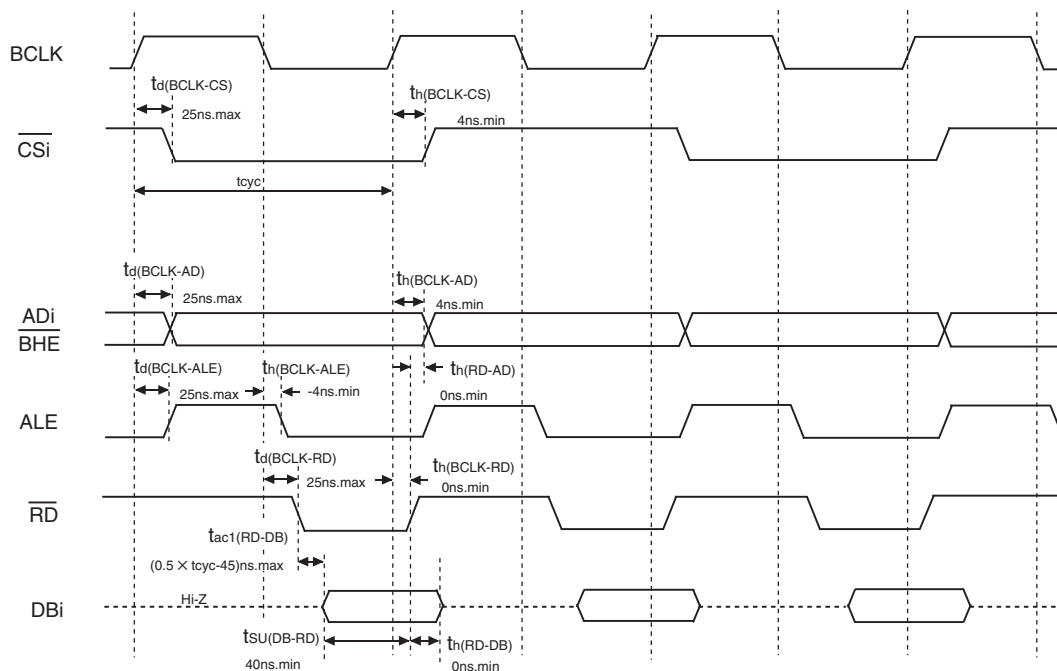
4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \text{ [ns]}$$

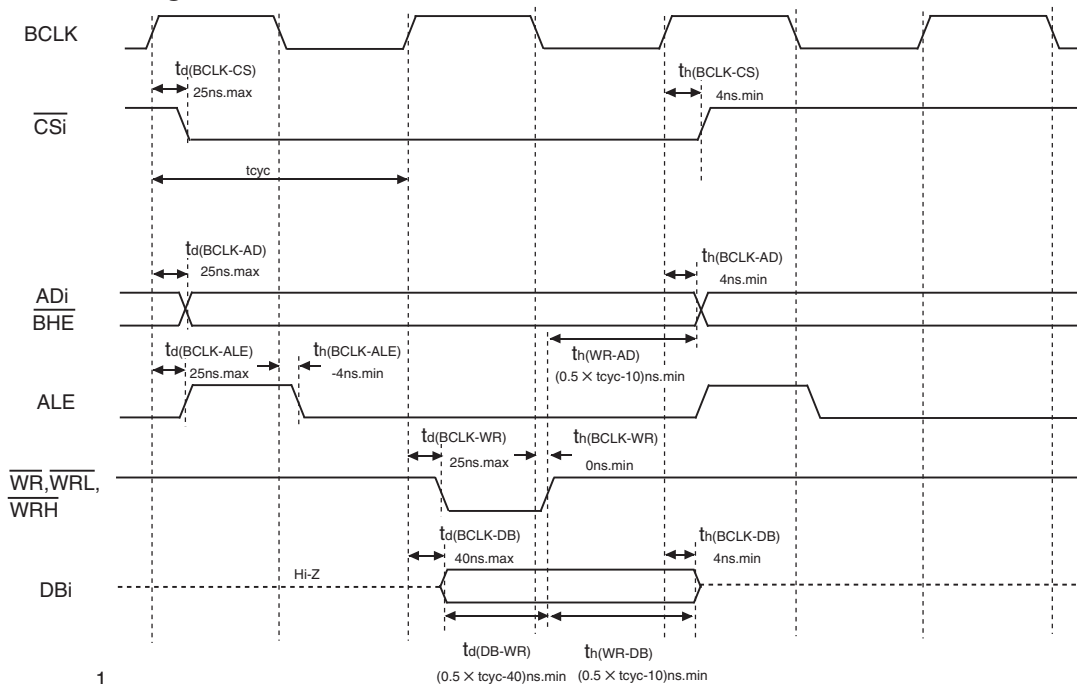
Memory Expansion Mode and Microprocessor Mode (For setting with no wait)

VCC = 5 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : $V_{IL} = 0.8 \text{ V}$, $V_{IH} = 2.0 \text{ V}$
- Output timing voltage : $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$

Figure 5.5 Timing Diagram (3)

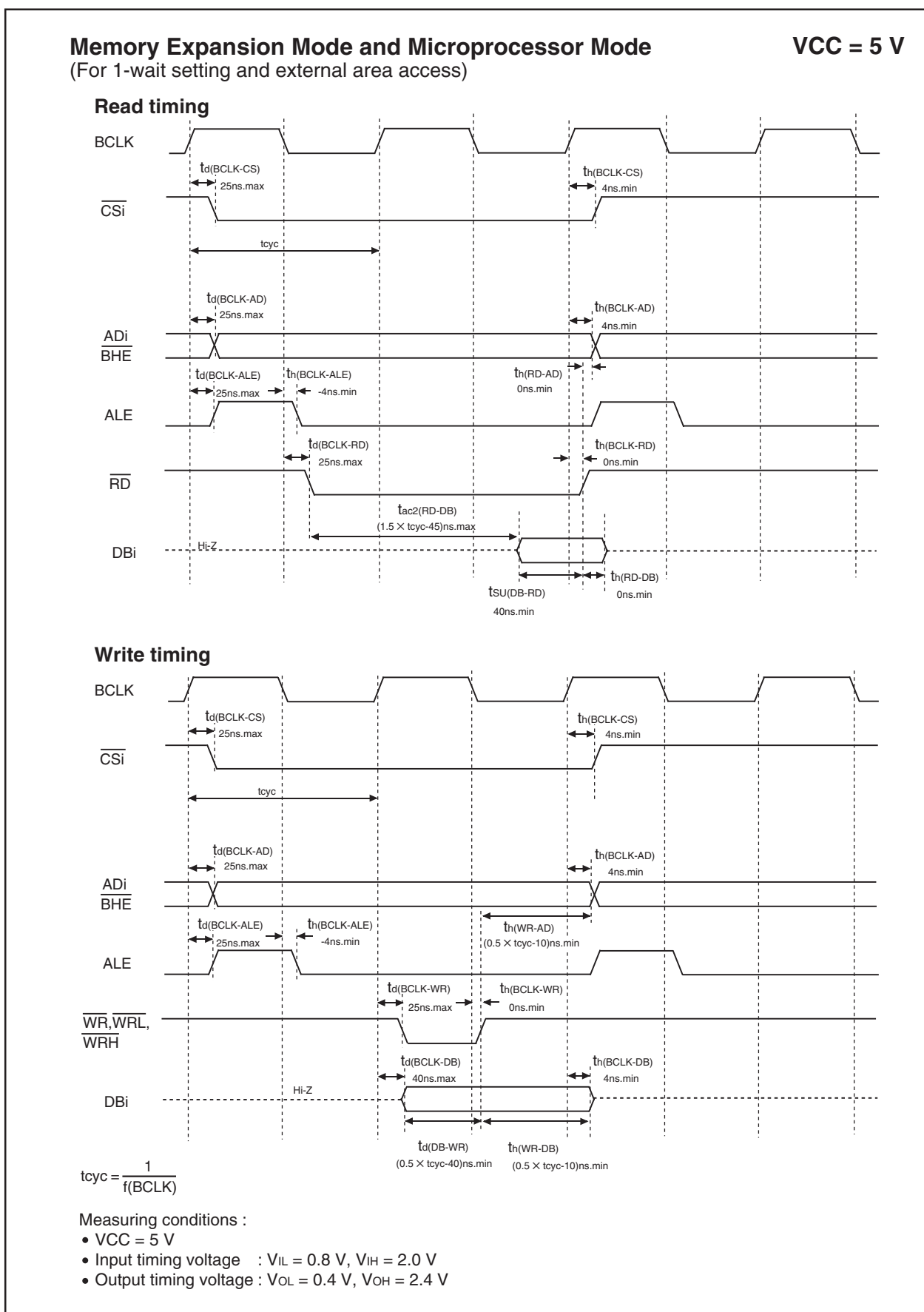
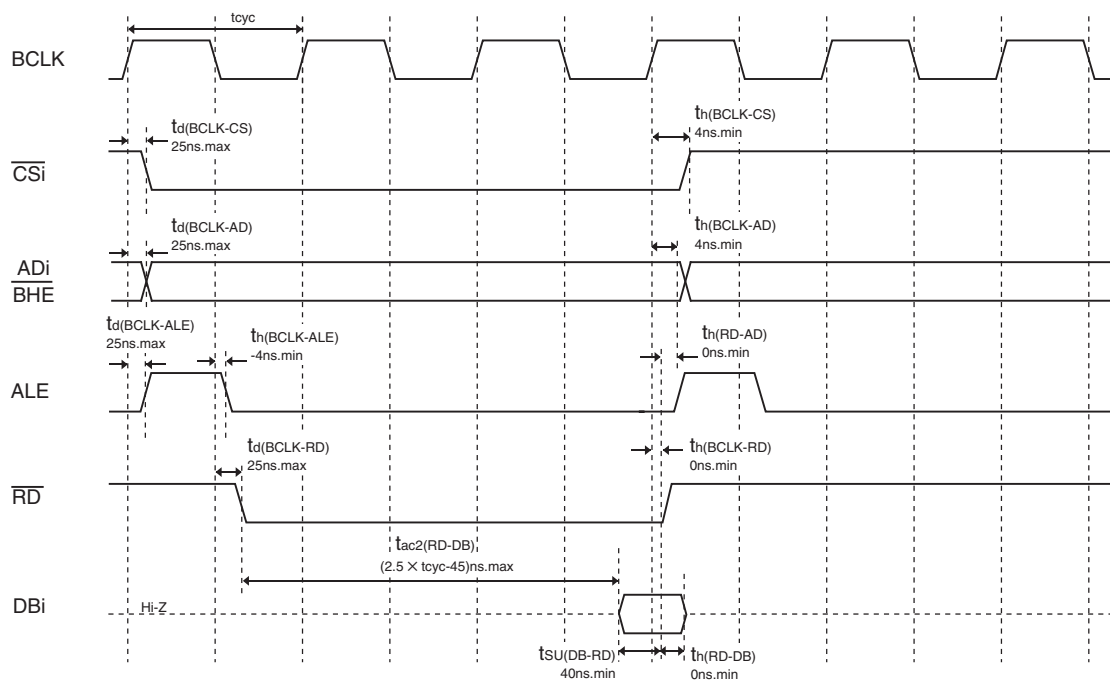


Figure 5.6 Timing Diagram (4)

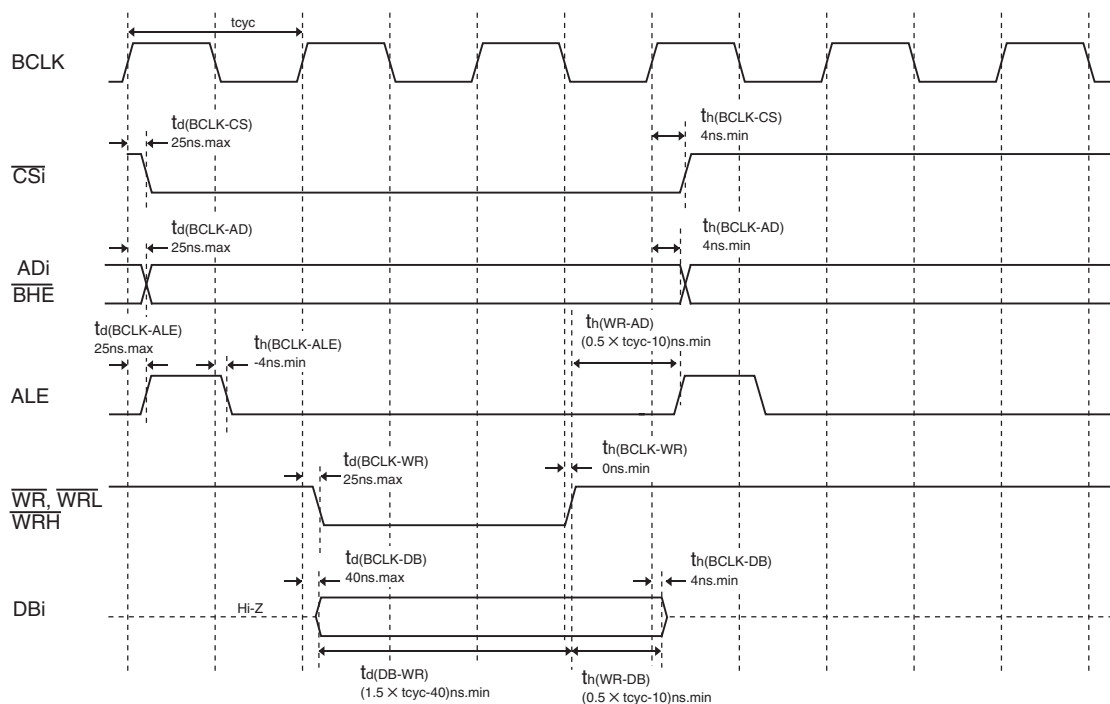
Memory Expansion Mode and Microprocessor Mode (For 2-wait setting and external area access)

VCC = 5 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage : $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

Figure 5.7 Timing Diagram (5)

Table 5.33 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I _{cc}	Power supply current (VCC = 3.0 to 5.5 V)	In single-chip mode, the output pins are open and other pins are VSS.	Mask ROM	f(BCLK) = 24 MHz, PLL operation, No division		20	36	mA
				On-chip oscillation, No division		1		mA
			Flash memory	f(BCLK) = 24 MHz, PLL operation, No division		22	38	mA
				On-chip oscillation, No division		1.8		mA
			Flash memory program	f(BCLK) = 10 MHz, VCC = 5 V		15		mA
			Flash memory erase	f(BCLK) = 10 MHz, VCC = 5 V		25		mA
			Mask ROM	f(BCLK) = 32 kHz, Low power dissipation mode, ROM ⁽²⁾		25		μA
			Flash memory	f(BCLK) = 32 kHz, Low power dissipation mode, RAM ⁽²⁾		25		μA
				f(BCLK) = 32 kHz, Low power dissipation mode, Flash memory ⁽²⁾		420		μA
			Mask ROM Flash memory	On-chip oscillation, Wait mode		50		μA
				f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity High		8.5		μA
				f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity Low		3.0		μA
				Stop mode, T _{opr} = 25°C		0.8	3.0	μA

NOTES:

1. Referenced to VCC = 3.0 to 5.5 V, VSS = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)****Table 5.42 Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 5.43 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.44 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 5.45 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG $\bar{}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	ADTRG $\bar{}$ input LOW pulse width	125		ns

Table 5.46 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.47 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	INTi input HIGH pulse width	250		ns
$t_{w(INL)}$	INTi input LOW pulse width	250		ns

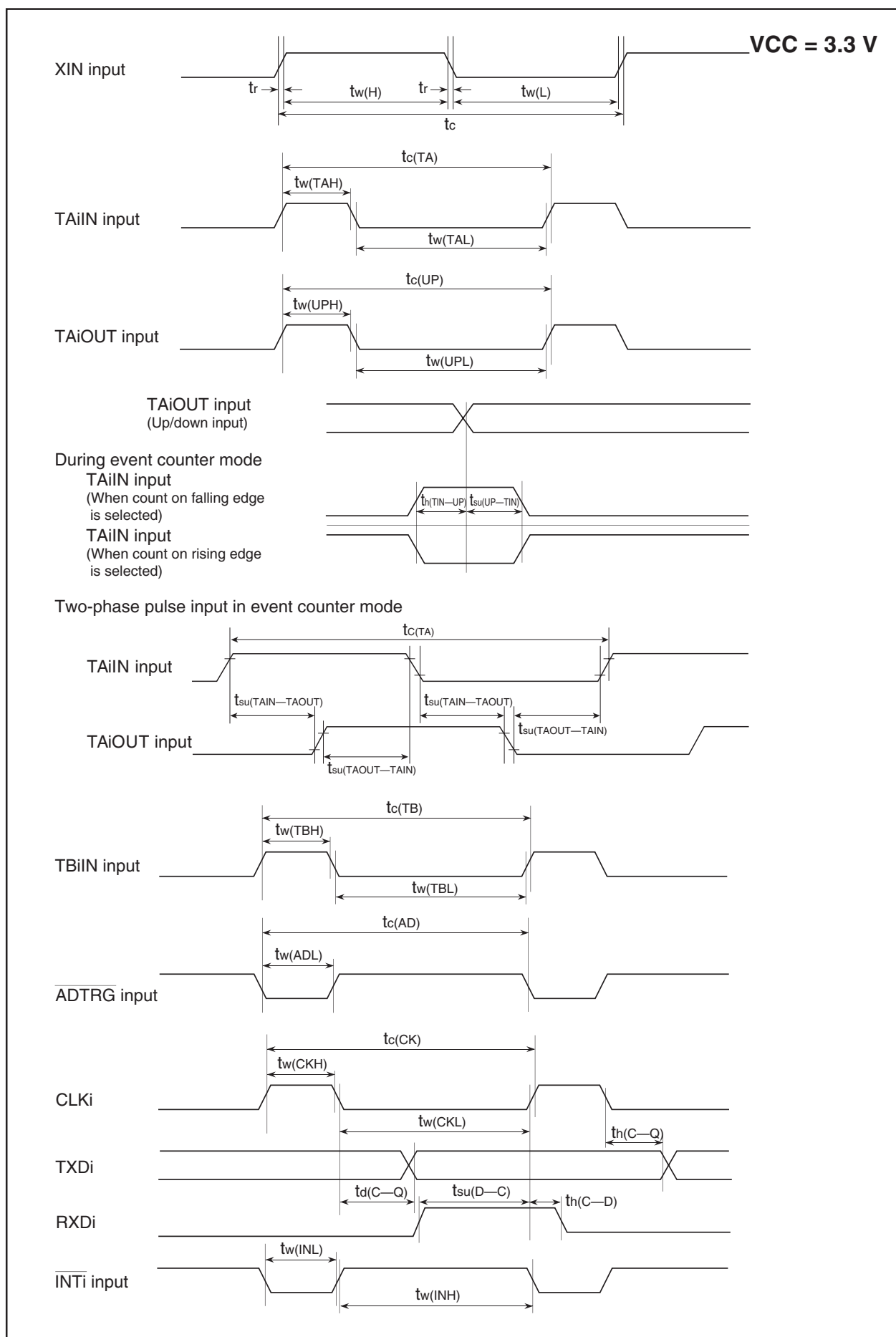


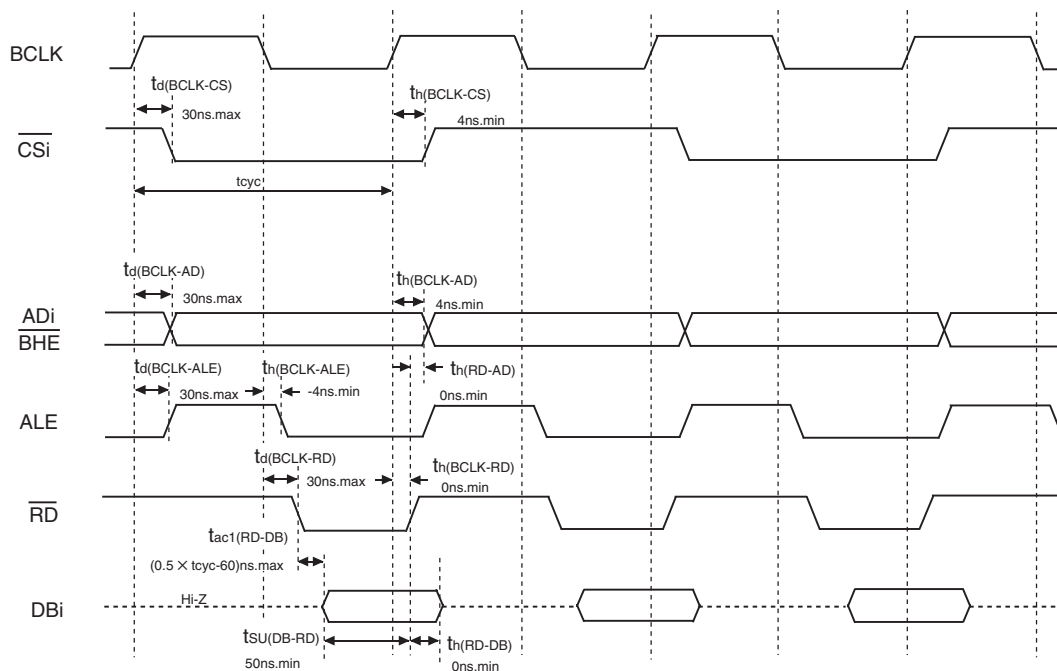
Figure 5.22 Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

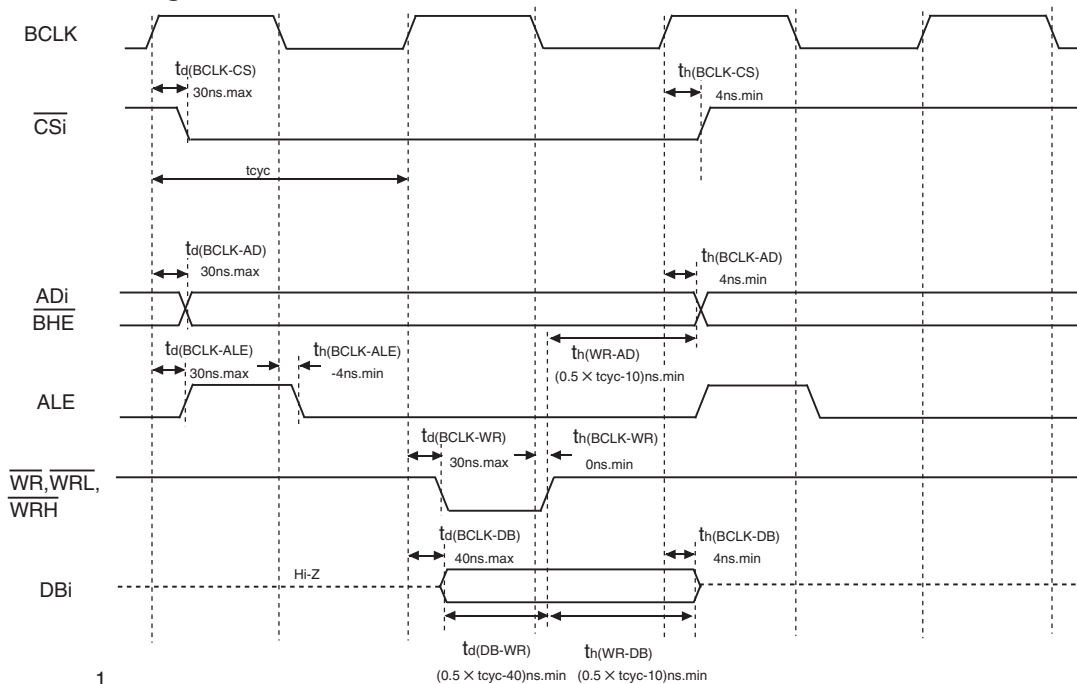
(For setting with no wait)

VCC = 3.3 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : $V_{IL} = 0.6 \text{ V}$, $V_{IH} = 2.7 \text{ V}$
- Output timing voltage : $V_{OL} = 1.65 \text{ V}$, $V_{OH} = 1.65 \text{ V}$

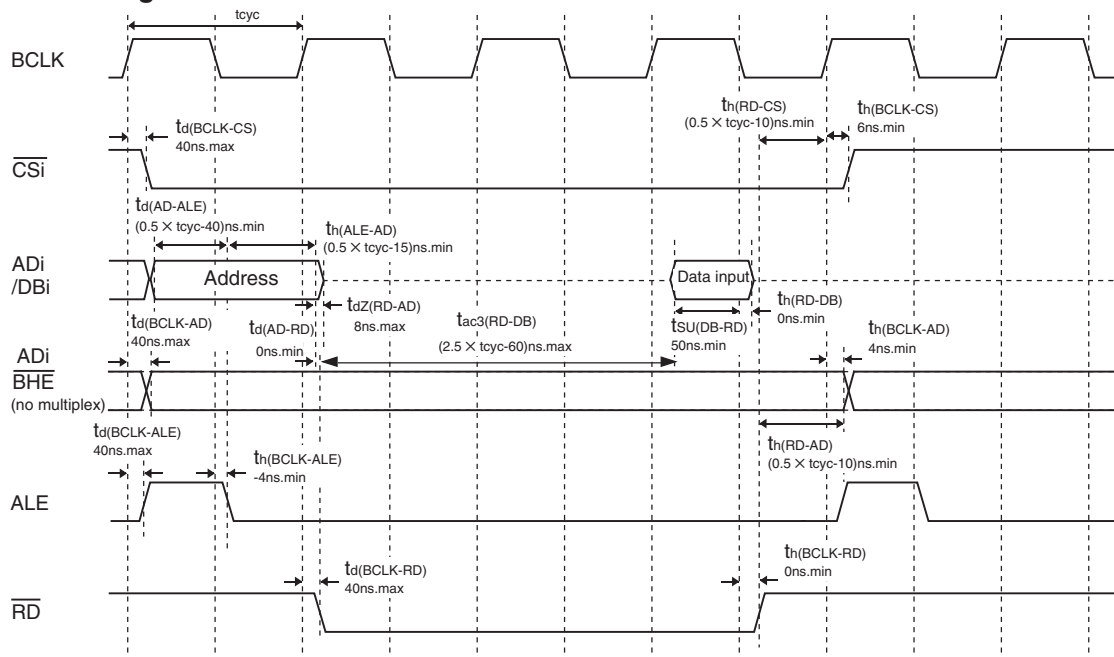
Figure 5.24 Timing Diagram (3)

Memory Expansion Mode and Microprocessor Mode

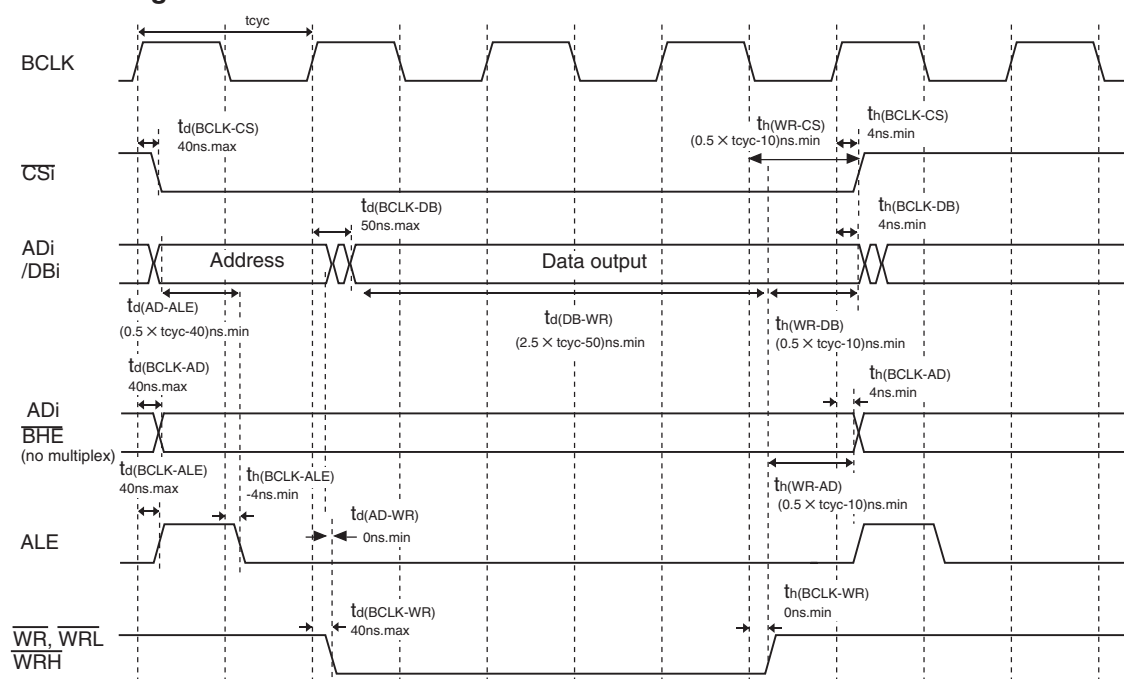
(For 3-wait setting, external area access and multiplexed bus selection)

VCC = 3.3 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : $V_{IL} = 0.6$ V, $V_{IH} = 2.7$ V
- Output timing voltage : $V_{OL} = 1.65$ V, $V_{OH} = 1.65$ V

Figure 5.29 Timing Diagram (8)

REVISION HISTORY

M16C/6N Group (M16C/6N4) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 30, 2003	–	First edition issued
2.00	Nov. 10, 2004	–	Revised edition issued * Words standardizes (on-chip oscillator) * 100P6Q-A (100-pin version) is added. * Revised parts and revised contents are as follows (except for change of a layout and an expressional change).
		1 2 4 5 6 8 12 13 19 27 28 29 31 32	1. Overview 3rd line: "and LQFP" is added. Table 1.1 Performance outline of M16C/6N Group (M16C/6N4) • Operation Mode is added. • Address Space is added. • Power Consumption is revised. • "LQFP" is added to Package. Table 1.2 Product List is revised. Figure 1.2 Type No., Memory Size, and Package: • "GP: Package 100P6Q-A" is added to Package type. Figure 1.3 Pin Configuration (Top View) (1): "ZP" is added. Figure 1.4 Pin Configuration (Top View) (2) is added. (100P6Q-A) Table 1.4 Pin Description (2): "ZP" is added to Timer A. 3. Memory • 5th to 6th lines: The description about the flash memory version (block A) is added. Figure 3.1 Memory Map • Internal ROM (data area) is added. • NOTES 3, 4 are added and NOTE 5 is revised. Table 4.1 SFR Information (1) • The value of After Reset in PM1 register is revised. • The value of After Reset in CM2 register is revised. Table 4.7 SFR Information (7) • The value of After Reset in FMR0 register is revised. Table 4.15 SFR Information (15) • The value of After Reset in U0C1 register is revised. • The value of After Reset in U1C1 register is revised. • NOTE 1 is added. Table 4.16 SFR Information (16) • The value of After Reset in DA0, DA1 registers are revised. Table 5.1 Absolute Maximum Ratings • "Flash Program Erase" in Operating Ambient Temperature is added. Table 5.3 Recommended Operating Conditions (2) • Parameters of Power Supply Ripple are added. • NOTE 4 is revised. Figure 5.1 Timing of Voltage Fluctuation is added. Table 5.4 Electrical Characteristics (1): Hysteresis • "CLK4" is revised to "CLK3", and "TA2OUT" is revised to "TA0OUT". • Max. of Standard in $\overline{\text{RESET}}$ is revised from "2.2" to "2.5". • XIN is added.