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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306n4mgt-158fpusl

Table 4.9 SFR Information (9)

Address	Register	Symbol	After Reset
0200h	CAN0 Message Control Register 0	C0MCTL0	00h
0201h	CAN0 Message Control Register 1	C0MCTL1	00h
0202h	CAN0 Message Control Register 2	C0MCTL2	00h
0203h	CAN0 Message Control Register 3	C0MCTL3	00h
0204h	CAN0 Message Control Register 4	C0MCTL4	00h
0205h	CAN0 Message Control Register 5	C0MCTL5	00h
0206h	CAN0 Message Control Register 6	C0MCTL6	00h
0207h	CAN0 Message Control Register 7	C0MCTL7	00h
0208h	CAN0 Message Control Register 8	C0MCTL8	00h
0209h	CAN0 Message Control Register 9	C0MCTL9	00h
020Ah	CAN0 Message Control Register 10	C0MCTL10	00h
020Bh	CAN0 Message Control Register 11	C0MCTL11	00h
020Ch	CAN0 Message Control Register 12	C0MCTL12	00h
020Dh	CAN0 Message Control Register 13	C0MCTL13	00h
020Eh	CAN0 Message Control Register 14	C0MCTL14	00h
020Fh	CAN0 Message Control Register 15	C0MCTL15	00h
0210h	CAN0 Control Register	C0CTLR	X0000001b
0211h			XX0X0000b
0212h	CAN0 Status Register	C0STR	00h
0213h			X0000001b
0214h	CAN0 Slot Status Register	C0SSTR	00h
0215h			00h
0216h	CAN0 Interrupt Control Register	C0ICR	00h
0217h			00h
0218h	CAN0 Extended ID Register	C0IDR	00h
0219h			00h
021Ah	CAN0 Configuration Register	C0CONR	XXh
021Bh			XXh
021Ch	CAN0 Receive Error Count Register	C0RECR	00h
021Dh	CAN0 Transmit Error Count Register	C0TECR	00h
021Eh	CAN0 Time Stamp Register	C0TSR	00h
021Fh			00h
0220h	CAN1 Message Control Register 0	C1MCTL0	00h
0221h	CAN1 Message Control Register 1	C1MCTL1	00h
0222h	CAN1 Message Control Register 2	C1MCTL2	00h
0223h	CAN1 Message Control Register 3	C1MCTL3	00h
0224h	CAN1 Message Control Register 4	C1MCTL4	00h
0225h	CAN1 Message Control Register 5	C1MCTL5	00h
0226h	CAN1 Message Control Register 6	C1MCTL6	00h
0227h	CAN1 Message Control Register 7	C1MCTL7	00h
0228h	CAN1 Message Control Register 8	C1MCTL8	00h
0229h	CAN1 Message Control Register 9	C1MCTL9	00h
022Ah	CAN1 Message Control Register 10	C1MCTL10	00h
022Bh	CAN1 Message Control Register 11	C1MCTL11	00h
022Ch	CAN1 Message Control Register 12	C1MCTL12	00h
022Dh	CAN1 Message Control Register 13	C1MCTL13	00h
022Eh	CAN1 Message Control Register 14	C1MCTL14	00h
022Fh	CAN1 Message Control Register 15	C1MCTL15	00h
0230h	CAN1 Control Register	C1CTLR	X0000001b
0231h			XX0X0000b
0232h	CAN1 Status Register	C1STR	00h
0233h			X0000001b
0234h	CAN1 Slot Status Register	C1SSTR	00h
0235h			00h
0236h	CAN1 Interrupt Control Register	C1ICR	00h
0237h			00h
0238h	CAN1 Extended ID Register	C1IDR	00h
0239h			00h
023Ah	CAN1 Configuration Register	C1CONR	XXh
023Bh			XXh
023Ch	CAN1 Receive Error Count Register	C1RECR	00h
023Dh	CAN1 Transmit Error Count Register	C1TECR	00h
023Eh	CAN1 Time Stamp Register	C1TSR	00h
023Fh			00h

X: Undefined

Table 4.11 SFR Information (11)

Address	Register	Symbol	After Reset
0280h	CAN1 Message Box 2: Identifier / DLC		XXh
0281h			XXh
0282h			XXh
0283h			XXh
0284h			XXh
0285h			XXh
0286h	CAN1 Message Box 2: Data Field		XXh
0287h			XXh
0288h			XXh
0289h			XXh
028Ah			XXh
028Bh			XXh
028Ch			XXh
028Dh			XXh
028Eh	CAN1 Message Box 2: Time Stamp		XXh
028Fh			XXh
0290h	CAN1 Message Box 3: Identifier / DLC		XXh
0291h			XXh
0292h			XXh
0293h			XXh
0294h			XXh
0295h			XXh
0296h	CAN1 Message Box 3: Data Field		XXh
0297h			XXh
0298h			XXh
0299h			XXh
029Ah			XXh
029Bh			XXh
029Ch			XXh
029Dh			XXh
029Eh	CAN1 Message Box 3: Time Stamp		XXh
029Fh			XXh
02A0h	CAN1 Message Box 4: Identifier / DLC		XXh
02A1h			XXh
02A2h			XXh
02A3h			XXh
02A4h			XXh
02A5h			XXh
02A6h	CAN1 Message Box 4: Data Field		XXh
02A7h			XXh
02A8h			XXh
02A9h			XXh
02AAh			XXh
02ABh			XXh
02ACh			XXh
02ADh			XXh
02AEh	CAN1 Message Box 4: Time Stamp		XXh
02AFh			XXh
02B0h	CAN1 Message Box 5: Identifier / DLC		XXh
02B1h			XXh
02B2h			XXh
02B3h			XXh
02B4h			XXh
02B5h			XXh
02B6h	CAN1 Message Box 5: Data Field		XXh
02B7h			XXh
02B8h			XXh
02B9h			XXh
02BAh			XXh
02BBh			XXh
02BCh			XXh
02BDh			XXh
02BEh	CAN1 Message Box 5: Time Stamp		XXh
02BFh			XXh

X: Undefined

Table 4.16 SFR Information (16) ⁽²⁾

Address	Register	Symbol	After Reset
03C0h	A/D Register 0	AD0	XXh
03C1h			XXh
03C2h			XXh
03C3h	A/D Register 1	AD1	XXh
03C4h			XXh
03C5h	A/D Register 2	AD2	XXh
03C6h			XXh
03C7h	A/D Register 3	AD3	XXh
03C8h			XXh
03C9h	A/D Register 4	AD4	XXh
03CAh			XXh
03CBh	A/D Register 5	AD5	XXh
03CCh			XXh
03CDh	A/D Register 6	AD6	XXh
03CEh			XXh
03CFh	A/D Register 7	AD7	XXh
03D0h			XXh
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	00h
03D5h			
03D6h	A/D Control Register 0	ADCON0	00000XXXb
03D7h	A/D Control Register 1	ADCON1	00h
03D8h	D/A Register 0	DA0	00h
03D9h			
03DAh	D/A Register 1	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh	Pull-up Control Register 0	PUR0	00h
03FDh	Pull-up Control Register 1	PUR1	00000000b ⁽¹⁾ 00000010b
03FEh	Pull-up Control Register 2	PUR2	00h
03FFh	Port Control Register	PCR	00h

X: Undefined

NOTES:

1. At hardware reset, the register is as follows:

- 00000000b where "L" is input to the CNVSS pin
- 00000010b where "H" is input to the CNVSS pin

At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:

- 00000000b where bits PM01 to PM00 in the PM0 register are 00b (single-chip mode)
- 00000010b where bits PM01 to PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode)

2. Blank spaces are reserved. No access is allowed.

Table 5.4 Electrical Characteristics (1) ⁽¹⁾

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	I _{OH} = -5 mA	V _{CC} -2.0		V _{CC}	V
V _{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	I _{OH} = -200 μA	V _{CC} -0.3		V _{CC}	V
V _{OH}	HIGH output voltage	XOUT	HIGHPOWER	I _{OH} = -1 mA	3.0	V _{CC}	V
			LOWPOWER	I _{OH} = -0.5 mA	3.0	V _{CC}	V
	HIGH output voltage	XCOUT	HIGHPOWER	With no load applied	2.5		V
			LOWPOWER	With no load applied	1.6		V
V _{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OL} = 5 mA			2.0	V
V _{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OL} = 200 μA			0.45	V
V _{OL}	LOW output voltage	XOUT	HIGHPOWER	I _{OL} = 1 mA		2.0	V
			LOWPOWER	I _{OL} = 0.5 mA		2.0	V
	LOW output voltage	XCOUT	HIGHPOWER	With no load applied	0		V
			LOWPOWER	With no load applied	0		V
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK3, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SIN3		0.2		1.0	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		2.5	V
I _{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I = 5 V			5.0	μA
I _{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I = 0 V			-5.0	μA
R _{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	V _I = 0 V	30	50	170	kΩ
R _{IXIN}	Feedback resistance	XIN			1.5		MΩ
R _{IXCIN}	Feedback resistance	XCIN			15		MΩ
V _{RAM}	RAM retention voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V, VSS = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 20 MHz unless otherwise specified.

Table 5.5 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I _{cc}	Power supply current (VCC = 4.2 to 5.5 V)	In single-chip mode, the output pins are open and other pins are VSS.	Mask ROM	f(BCLK) = 20 MHz, PLL operation, No division		18	32	mA
				On-chip oscillation, No division		1		mA
			Flash memory	f(BCLK) = 20 MHz, PLL operation, No division		20	34	mA
				On-chip oscillation, No division		1.8		mA
			Flash memory program	f(BCLK) = 10 MHz, VCC = 5 V		15		mA
			Flash memory erase	f(BCLK) = 10 MHz, VCC = 5 V		25		mA
			Mask ROM	f(BCLK) = 32 kHz, Low power dissipation mode, ROM ⁽²⁾		25		μA
			Flash memory	f(BCLK) = 32 kHz, Low power dissipation mode, RAM ⁽²⁾		25		μA
				f(BCLK) = 32 kHz, Low power dissipation mode, Flash memory ⁽²⁾		420		μA
			Mask ROM Flash memory	On-chip oscillation, Wait mode		50		μA
				f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity High		8.5		μA
				f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity Low		3.0		μA
				Stop mode, T _{opr} = 25°C		0.8	3.0	μA

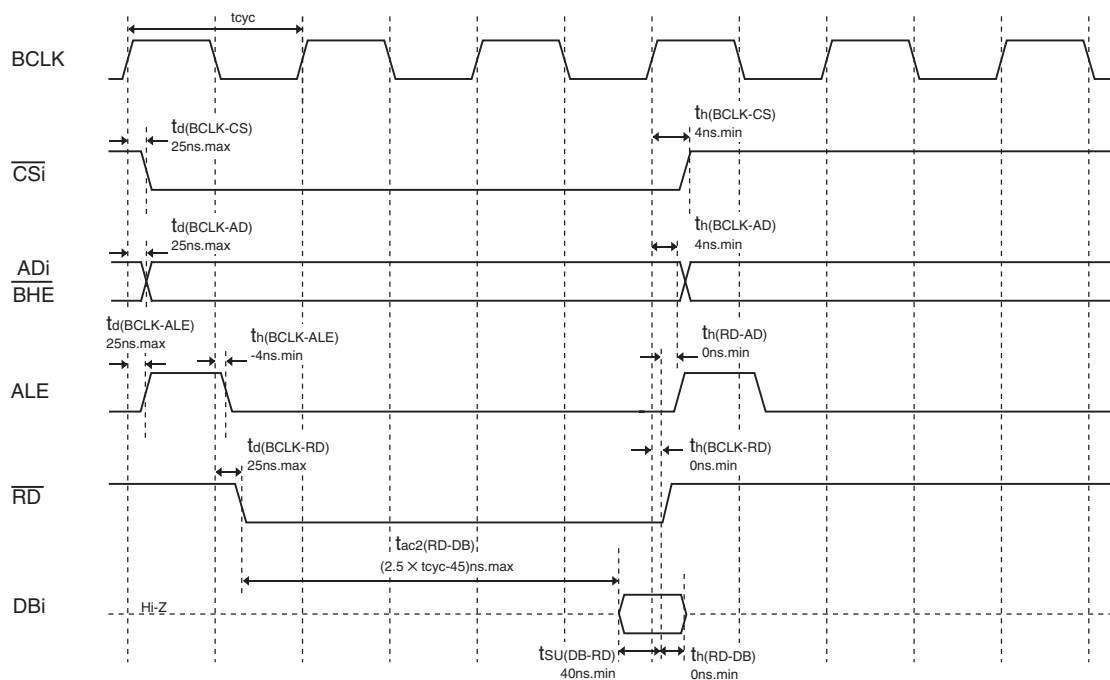
NOTES:

1. Referenced to VCC = 4.2 to 5.5 V, VSS = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 20 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

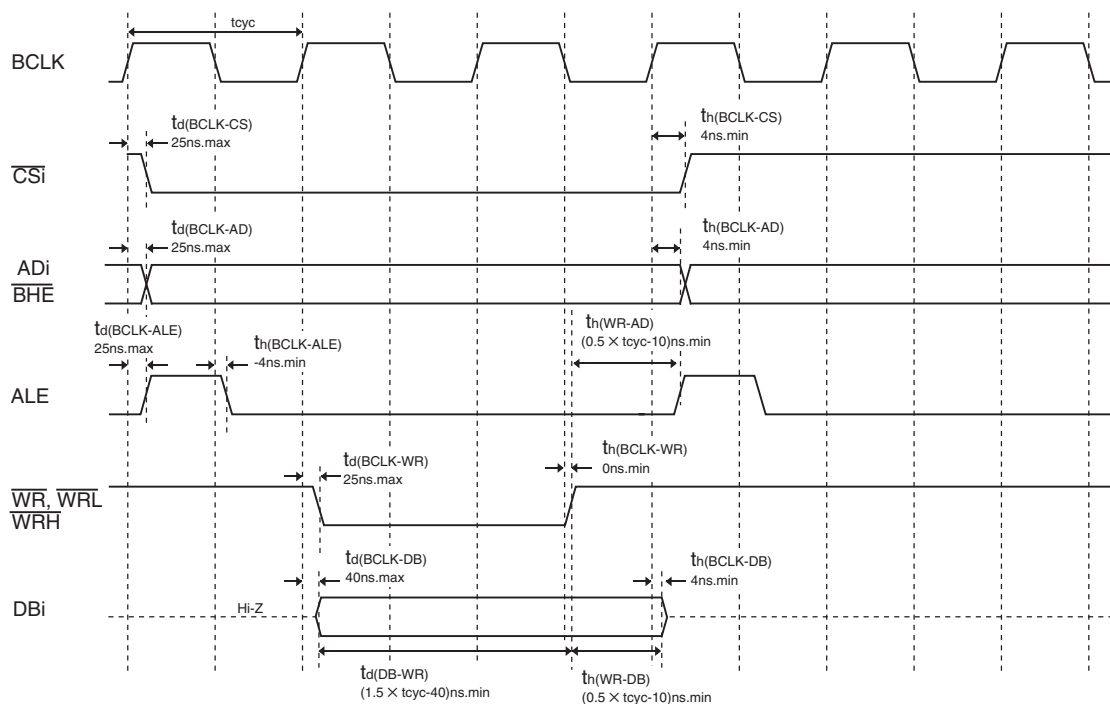
Memory Expansion Mode and Microprocessor Mode (For 2-wait setting and external area access)

VCC = 5 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions :

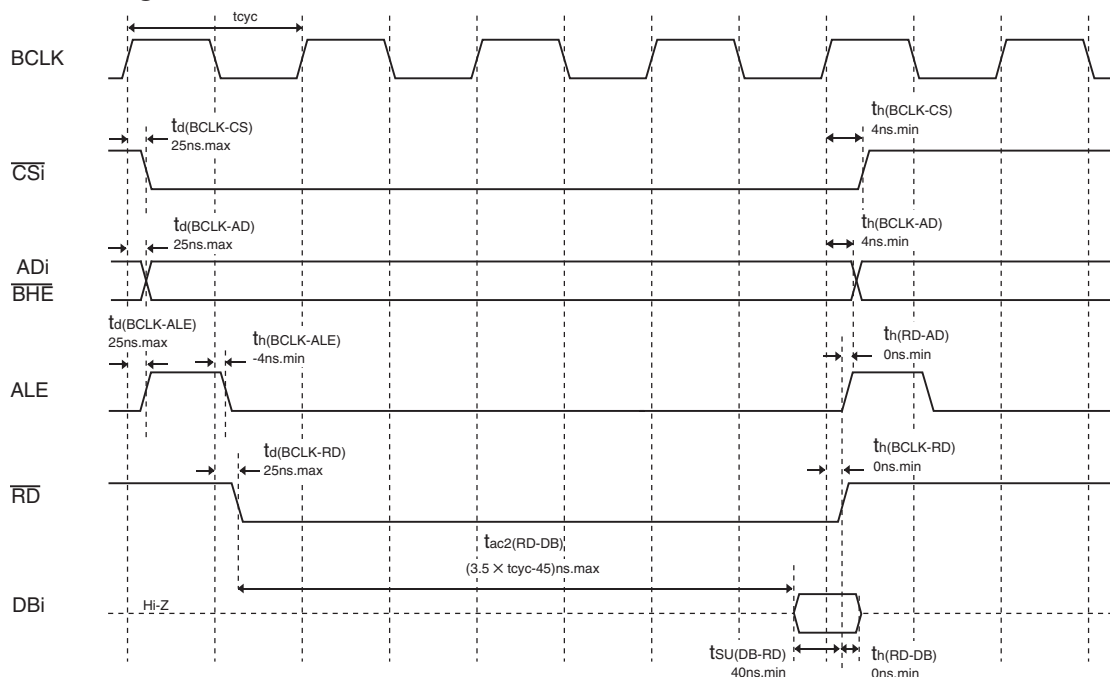
- VCC = 5 V
- Input timing voltage : $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage : $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

Figure 5.7 Timing Diagram (5)

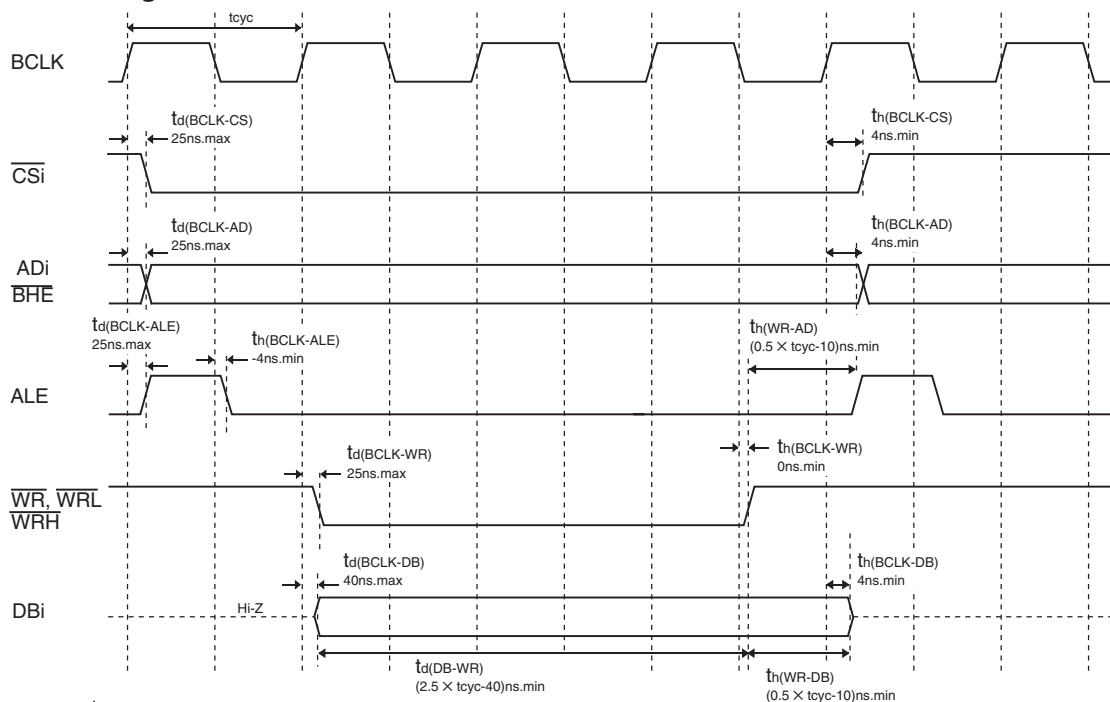
Memory Expansion Mode and Microprocessor Mode (For 3-wait setting and external area access)

VCC = 5 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

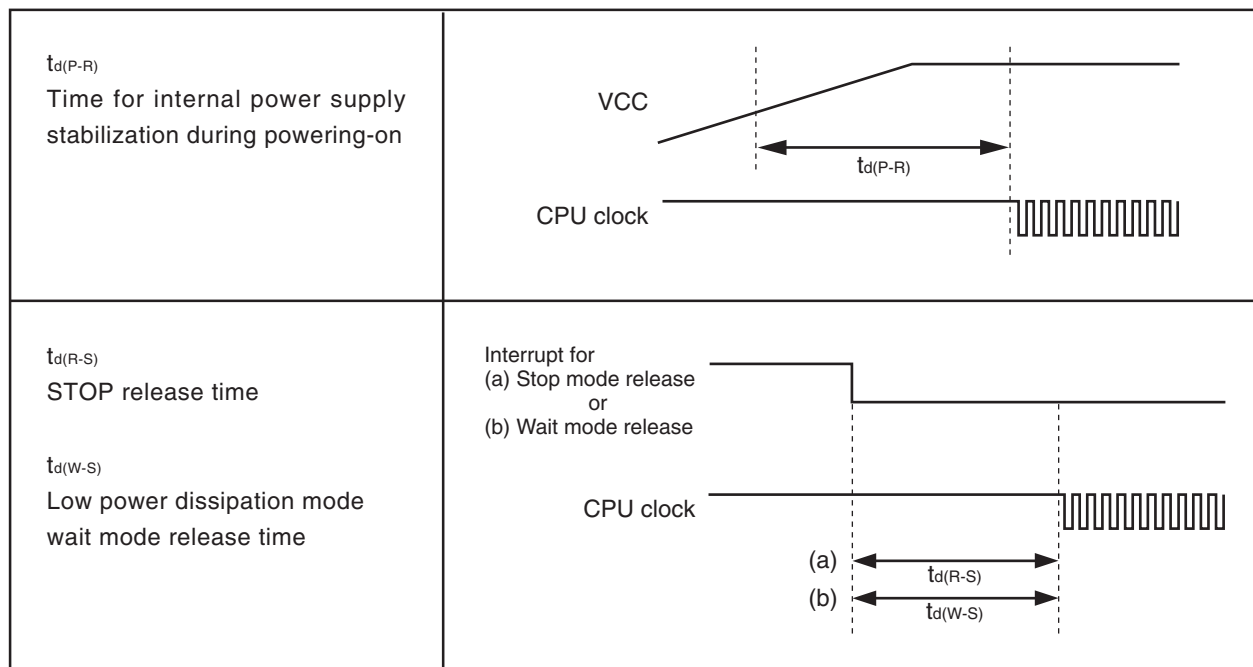
Measuring conditions :

- VCC = 5 V
- Input timing voltage : $V_{IL} = 0.8 V$, $V_{IH} = 2.0 V$
- Output timing voltage : $V_{OL} = 0.4 V$, $V_{OH} = 2.4 V$

Figure 5.8 Timing Diagram (6)

Table 5.31 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	$V_{CC} = 3.0 \text{ to } 5.5 \text{ V}$			2	ms
$t_{d(R-S)}$	STOP release time				150	μs
$t_{d(W-S)}$	Low power dissipation mode wait mode release time				150	μs

**Figure 5.11 Power Supply Circuit Timing Diagram**

Timing Requirements**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)****Table 5.34 External Clock Input (XIN Input)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c	External clock input cycle time	62.5		ns
t _{w(H)}	External clock input HIGH pulse width	25		ns
t _{w(L)}	External clock input LOW pulse width	25		ns
t _r	External clock rise time		15	ns
t _f	External clock fall time		15	ns

Table 5.35 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{ac1} (RD-DB)	Data input access time (for setting with no wait)		(NOTE 1)	ns
t _{ac2} (RD-DB)	Data input access time (for setting with wait)		(NOTE 2)	ns
t _{ac3} (RD-DB)	Data input access time (when accessing multiplexed bus area)		(NOTE 3)	ns
t _{su} (DB-RD)	Data input setup time	40		ns
t _{su} (RDY-BCLK)	RDY input setup time	30		ns
t _{su} (HOLD-BCLK)	HOLD input setup time	40		ns
t _h (RD-DB)	Data input hold time	0		ns
t _h (BCLK-RDY)	RDY input hold time	0		ns
t _h (BCLK-HOLD)	HOLD input hold time	0		ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 1-wait setting, "3" for 2-wait setting and "4" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(\text{BCLK})} - 45 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

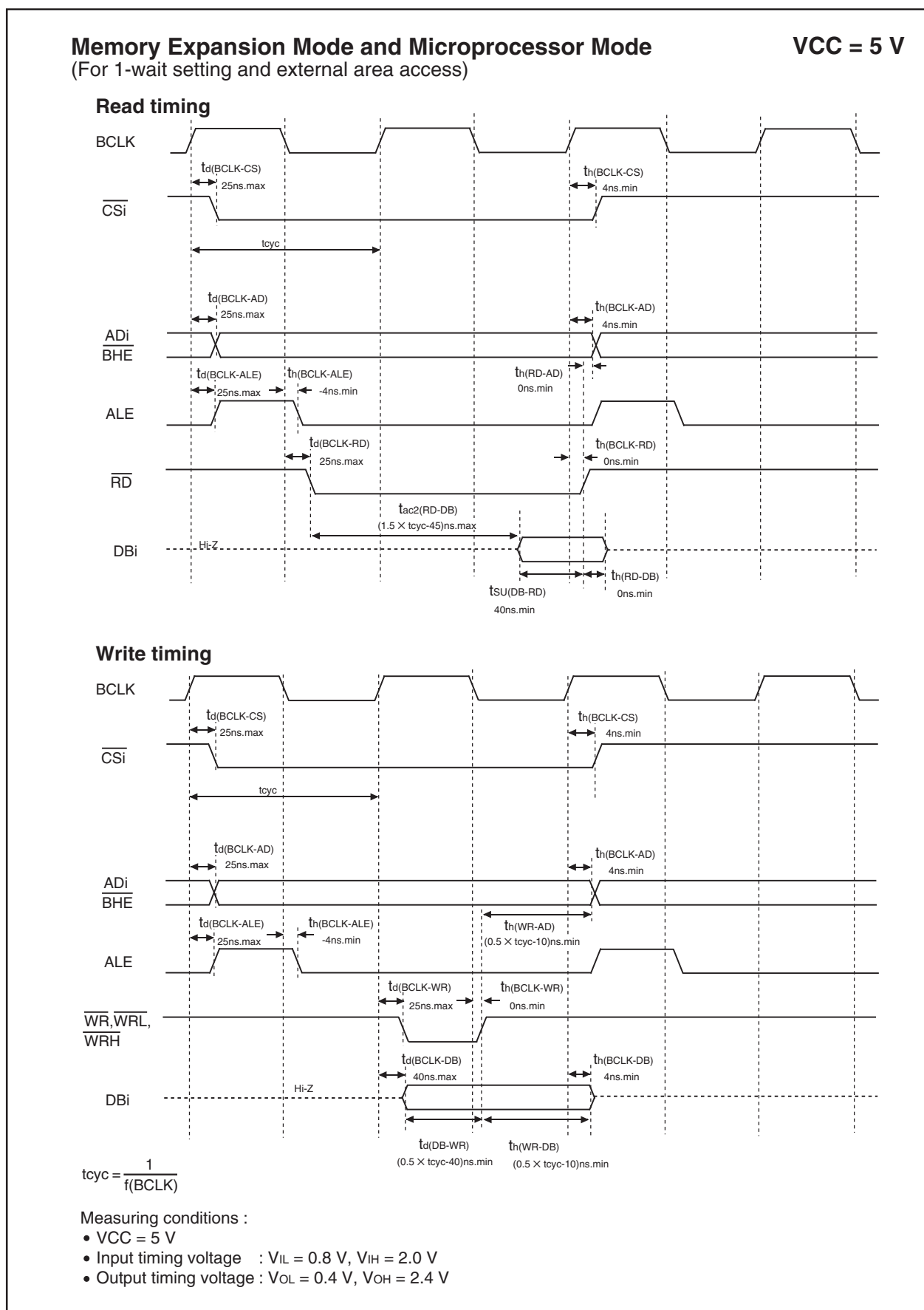
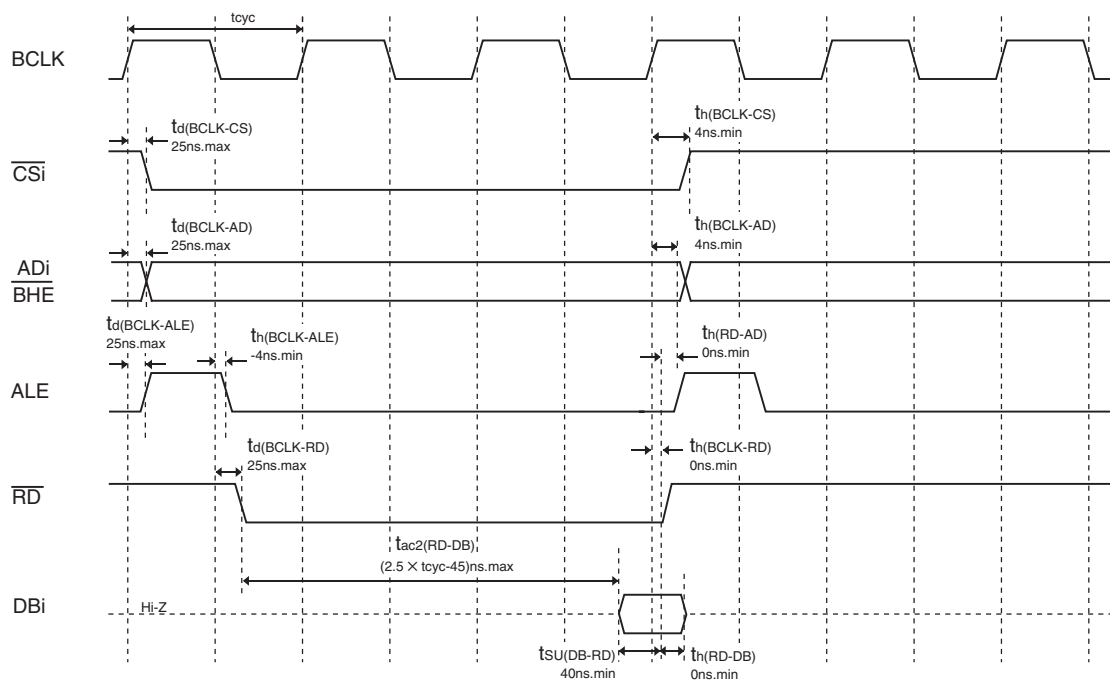


Figure 5.16 Timing Diagram (4)

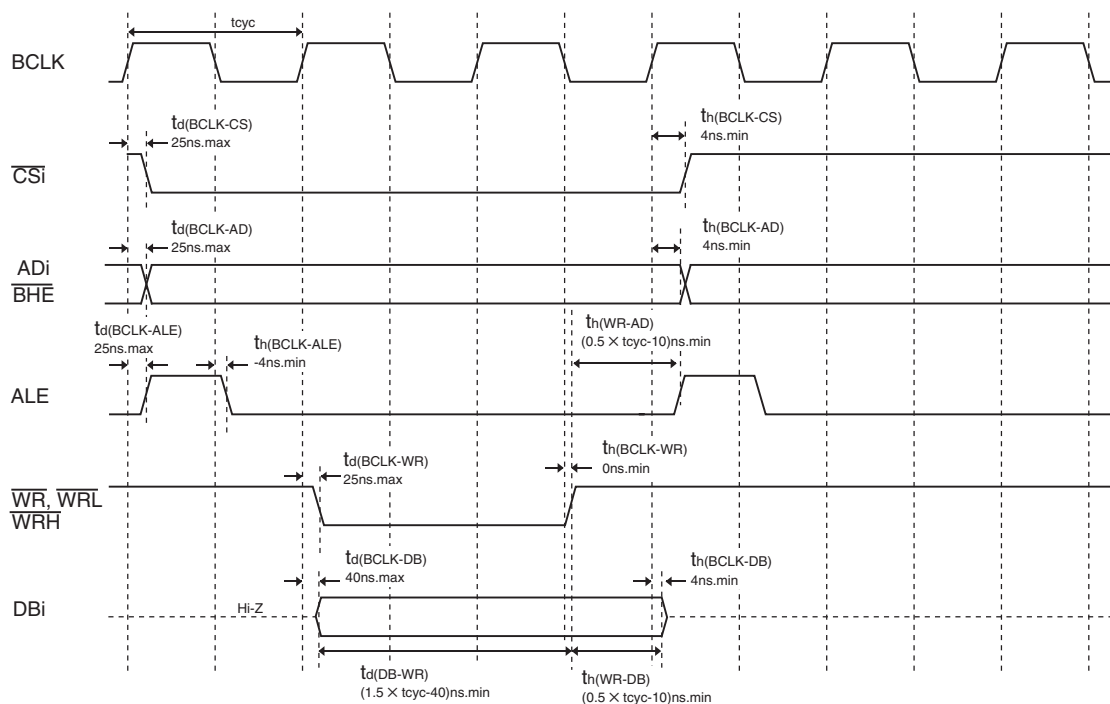
Memory Expansion Mode and Microprocessor Mode (For 2-wait setting and external area access)

VCC = 5 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

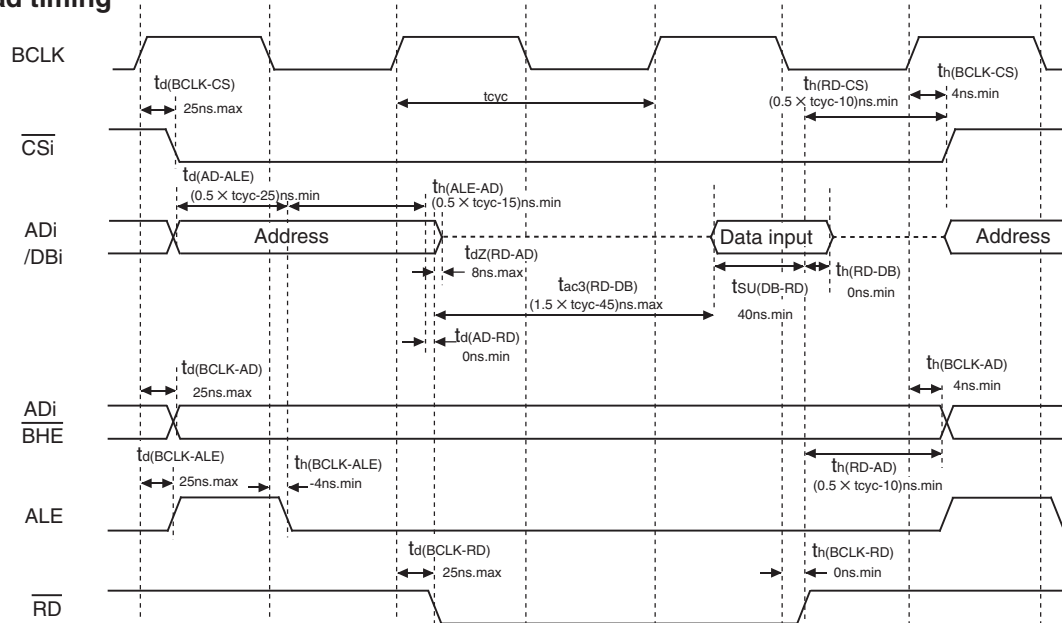
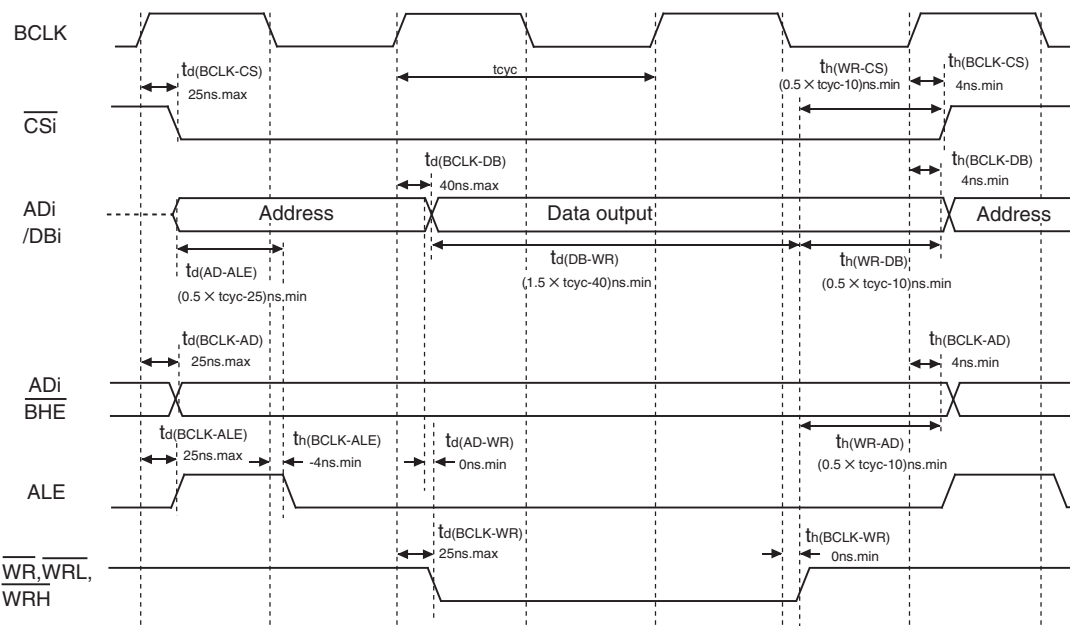
Measuring conditions :

- VCC = 5 V
- Input timing voltage : $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage : $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

Figure 5.17 Timing Diagram (5)

Memory Expansion Mode and Microprocessor Mode**VCC = 5 V**

(For 1- or 2-wait setting, external area access and multiplexed bus selection)

Read timing**Write timing**

$$t_{\text{cyc}} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : $V_{\text{IL}} = 0.8 \text{ V}$, $V_{\text{IH}} = 2.0 \text{ V}$
- Output timing voltage : $V_{\text{OL}} = 0.4 \text{ V}$, $V_{\text{OH}} = 2.4 \text{ V}$

Figure 5.19 Timing Diagram (7)

Timing Requirements**VCC = 3.3 V****(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)****Table 5.54 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiIN input cycle time	150		ns
t _{w(TAH)}	TAiIN input HIGH pulse width	60		ns
t _{w(TAL)}	TAiIN input LOW pulse width	60		ns

Table 5.55 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiIN input cycle time	600		ns
t _{w(TAH)}	TAiIN input HIGH pulse width	300		ns
t _{w(TAL)}	TAiIN input LOW pulse width	300		ns

Table 5.56 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiIN input cycle time	300		ns
t _{w(TAH)}	TAiIN input HIGH pulse width	150		ns
t _{w(TAL)}	TAiIN input LOW pulse width	150		ns

Table 5.57 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{w(TAH)}	TAiIN input HIGH pulse width	150		ns
t _{w(TAL)}	TAiIN input LOW pulse width	150		ns

Table 5.58 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(UP)}	TAiOUT input cycle time	3000		ns
t _{w(UPH)}	TAiOUT input HIGH pulse width	1500		ns
t _{w(UPL)}	TAiOUT input LOW pulse width	1500		ns
t _{su(UP-TIN)}	TAiOUT input setup time	600		ns
t _{h(TIN-UP)}	TAiOUT input hold time	600		ns

Table 5.59 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiIN input cycle time	2		μs
t _{su(TAIN-TAOUT)}	TAiOUT input setup time	500		ns
t _{su(TAOUT-TAIN)}	TAiIN input setup time	500		ns

Switching Characteristics**VCC = 3.3 V****(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.66 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_d(\text{BCLK-AD})$	Address output delay time	Figure 5.21		30	ns
$t_h(\text{BCLK-AD})$	Address output hold time (in relation to BCLK)		4		ns
$t_h(\text{RD-AD})$	Address output hold time (in relation to RD)		0		ns
$t_h(\text{WR-AD})$	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_d(\text{BCLK-CS})$	Chip select output delay time			30	ns
$t_h(\text{BCLK-CS})$	Chip select output hold time (in relation to BCLK)		4		ns
$t_d(\text{BCLK-ALE})$	ALE signal output delay time			25	ns
$t_h(\text{BCLK-ALE})$	ALE signal output hold time		–4		ns
$t_d(\text{BCLK-RD})$	RD signal output delay time			30	ns
$t_h(\text{BCLK-RD})$	RD signal output hold time		0		ns
$t_d(\text{BCLK-WR})$	WR signal output delay time			30	ns
$t_h(\text{BCLK-WR})$	WR signal output hold time		0		ns
$t_d(\text{BCLK-DB})$	Data output delay time (in relation to BCLK)			40	ns
$t_h(\text{BCLK-DB})$	Data output hold time (in relation to BCLK) ⁽³⁾		4		ns
$t_d(\text{DB-WR})$	Data output delay time (in relation to WR)		(NOTE 2)		ns
$t_h(\text{WR-DB})$	Data output hold time (in relation to WR) ⁽³⁾		(NOTE 1)		ns
$t_d(\text{BCLK-HLDA})$	HLDA output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad f(\text{BCLK}) \text{ is 12.5 MHz or less.}$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

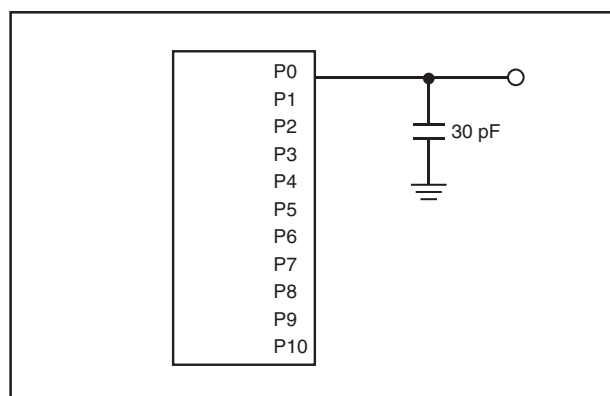
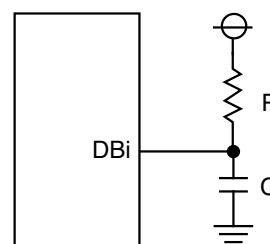
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, $C = 30 \text{ pF}$,

$R = 1 \text{ k}\Omega$, hold time of output “L” level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$

**Figure 5.21 Port P0 to P10 Measurement Circuit**

Switching Characteristics**VCC = 3.3 V****(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.67 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 5.21		30	ns
t _h (BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (in relation to RD)		0		ns
t _h (WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip select output delay time			30	ns
t _h (BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
t _d (BCLK-ALE)	ALE signal output delay time			25	ns
t _h (BCLK-ALE)	ALE signal output hold time		–4		ns
t _d (BCLK-RD)	RD signal output delay time			30	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			30	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (in relation to BCLK) ⁽³⁾		4		ns
t _d (DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data output hold time (in relation to WR) ⁽³⁾		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

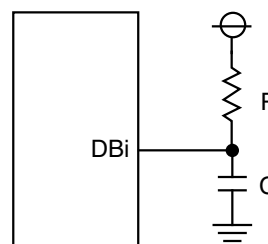
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2 V_{CC}$, $C = 30 \text{ pF}$,

$R = 1 \text{ k}\Omega$, hold time of output “L” level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$



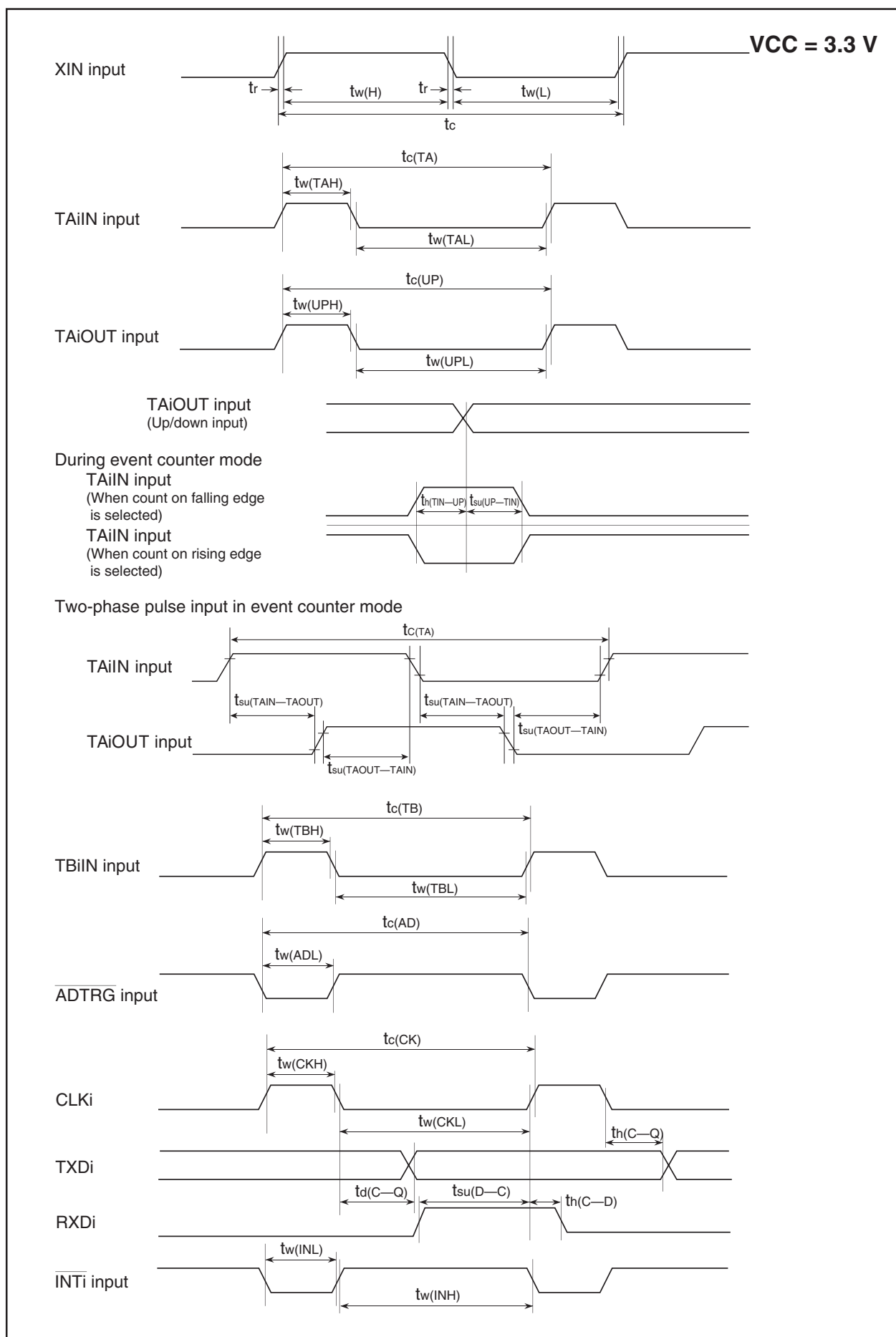
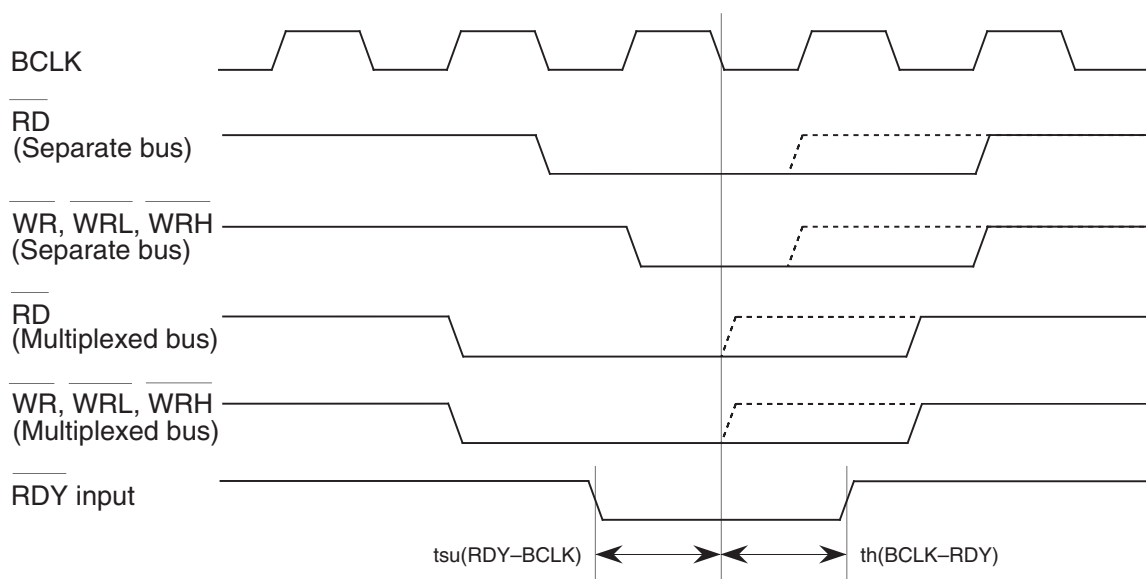


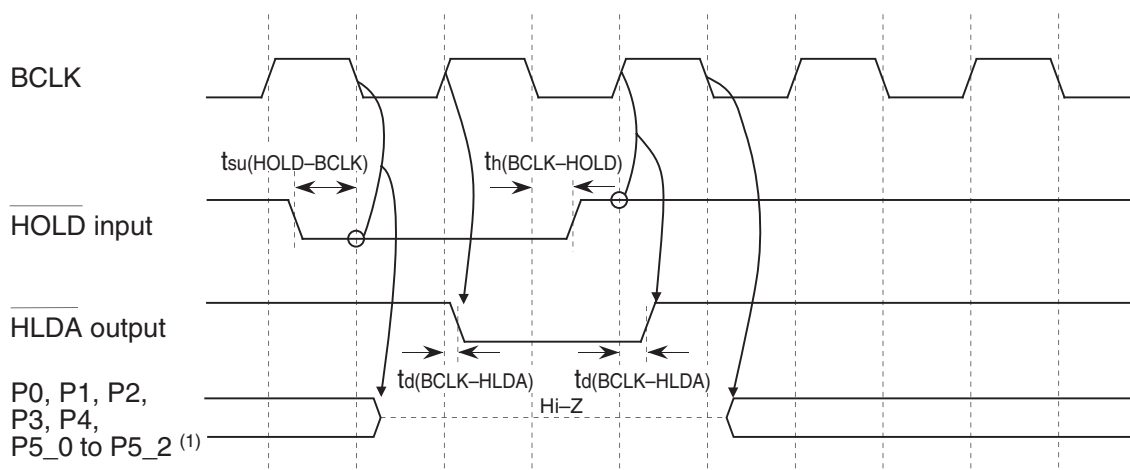
Figure 5.22 Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode**VCC = 3.3 V**

(Effective for setting with wait)



(Common to setting with wait and setting without wait)

**NOTE:**

1. The above pins are set to high-impedance regardless of the input level of the BYTE pin, the PM06 bit in the PM0 register, and the PM11 bit in the PM1 register.

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : Determined with $V_{IL} = 0.6 \text{ V}$, $V_{IH} = 2.7 \text{ V}$
- Output timing voltage: Determined with $V_{OL} = 1.65 \text{ V}$, $V_{OH} = 1.65 \text{ V}$

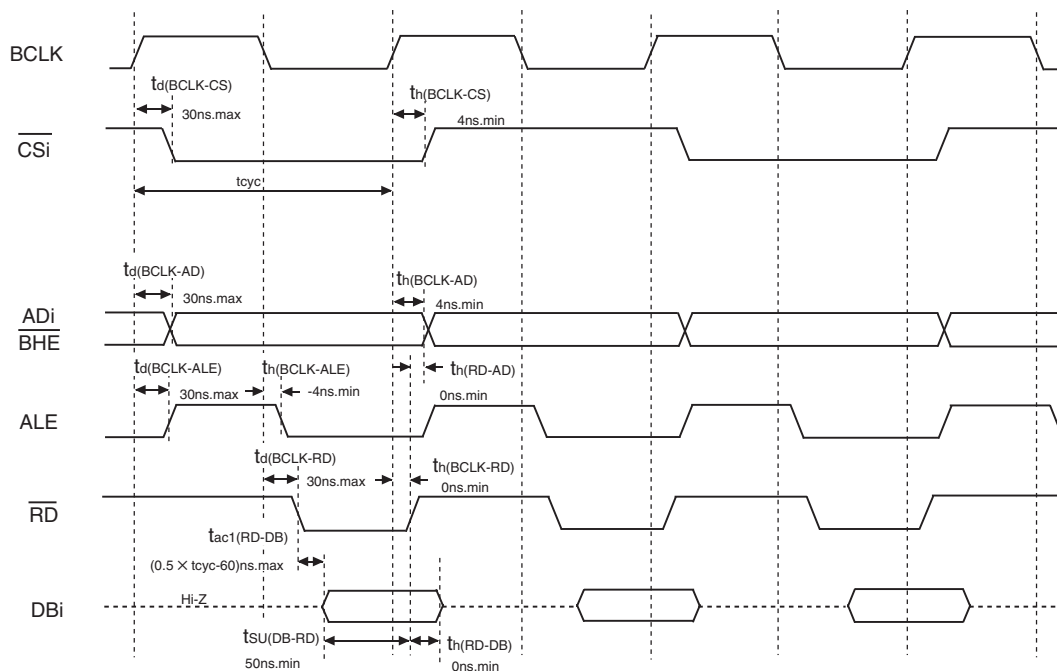
Figure 5.23 Timing Diagram (2)

Memory Expansion Mode and Microprocessor Mode

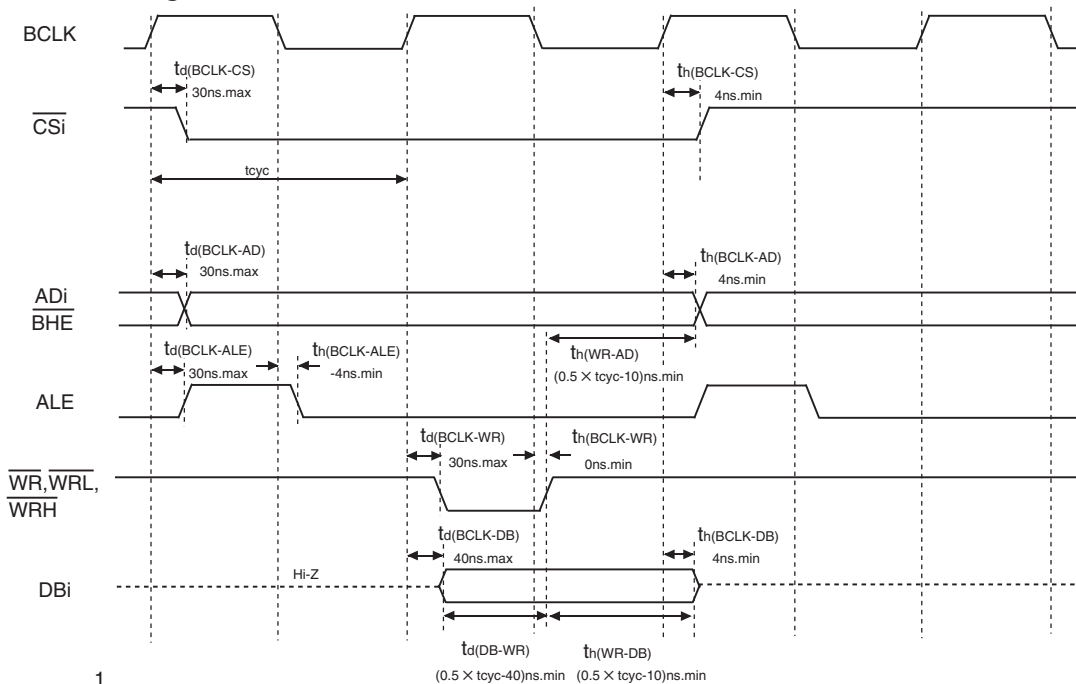
(For setting with no wait)

VCC = 3.3 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions :

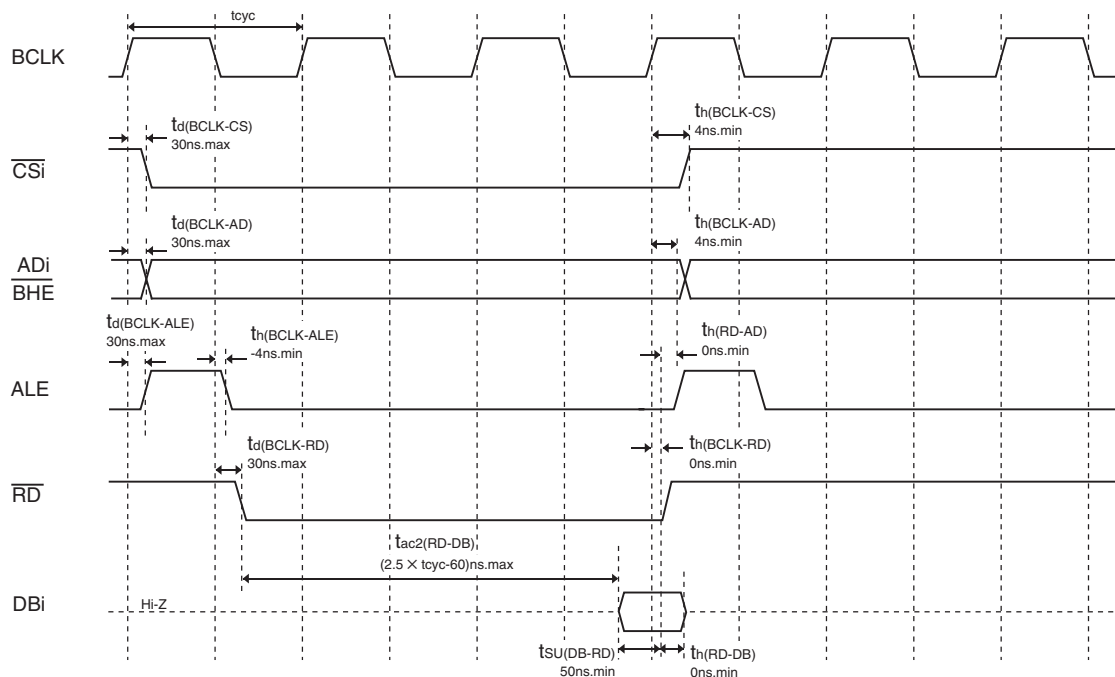
- VCC = 3.3 V
- Input timing voltage : $V_{IL} = 0.6 \text{ V}$, $V_{IH} = 2.7 \text{ V}$
- Output timing voltage : $V_{OL} = 1.65 \text{ V}$, $V_{OH} = 1.65 \text{ V}$

Figure 5.24 Timing Diagram (3)

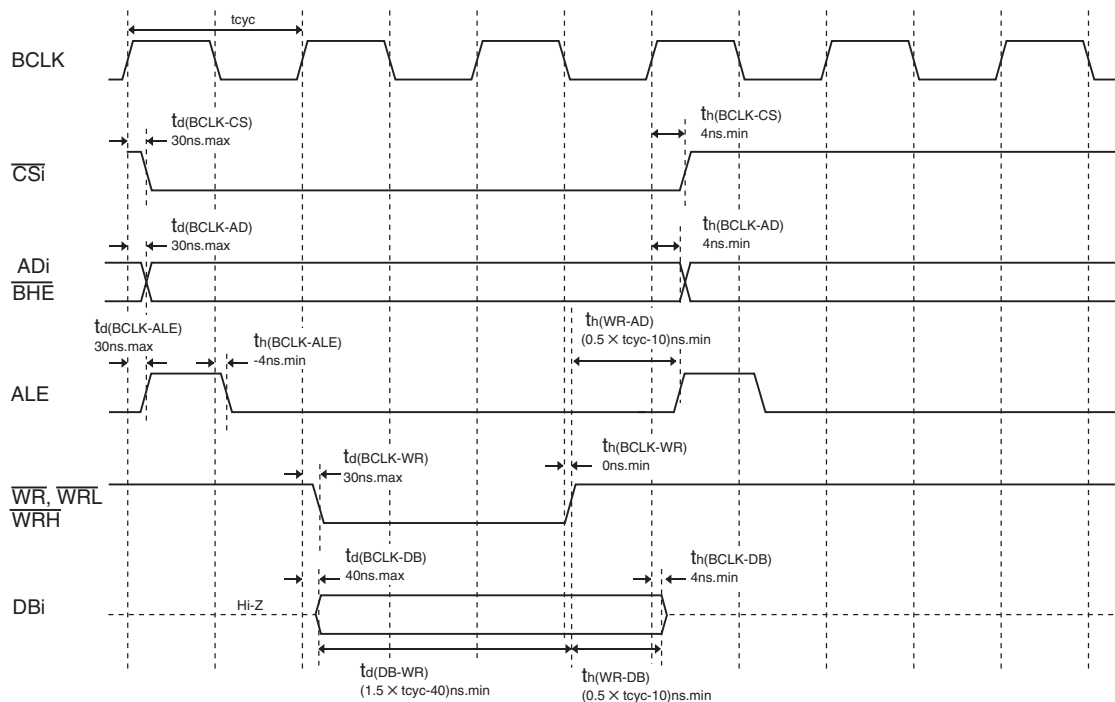
Memory Expansion Mode and Microprocessor Mode (For 2-wait setting and external area access)

VCC = 3.3 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : $V_{IL} = 0.6$ V, $V_{IH} = 2.7$ V
- Output timing voltage : $V_{OL} = 1.65$ V, $V_{OH} = 1.65$ V

Figure 5.26 Timing Diagram (5)

REVISION HISTORY

M16C/6N Group (M16C/6N4) Data Sheet

Rev.	Date	Description	
		Page	Summary
2.00	Nov. 10, 2004	34	Table 5.6 A/D Conversion Characteristics: "Tolerance Level Impedance" is added.
		35	Table 5.8 Power Supply Circuit Timing Characteristics: " $t_{d(M-L)}$ " is deleted. Figure 5.2 Power Supply Circuit Timing Diagram is added.
		36	Table 5.10 Memory Expansion Mode and Microprocessor Mode: " $t_{d(BCLK-HLDA)}$ " is deleted.
		38	Table 5.21 Serial I/O: Min. of standard in $t_{su(D-C)}$ is revised from "30" to "70".
		39	Table 5.23 Memory Expansion Mode and Microprocessor Mode (for setting with no wait) • Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15". • $t_{d(BCLK-HLDA)}$ is added.
		40	Table 5.24 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access) • Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15". • $t_{d(BCLK-HLDA)}$ is added.
		41	Table 5.25 Memory Expansion Mode and Microprocessor Mode (for 2- to 3-wait setting, external area access and multiplexed bus selection) • $t_{d(BCLK-HLDA)}$ is added. • Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15".
		42	Figure 5.4 Timing Diagram (1): "XIN input" is added.
		44, 45	Figures 5.6 and 5.7 Timing Diagram (3) (4): "DB" in Read timing is revised to "DBi".
		46, 47	Figures 5.8 and 5.9 Timing Diagram (5) (6): "DB" in Write timing is revised to "DBi".
		49	Figure 5.11 Timing Diagram (8) • "ADi/DB" in Read/Write timing is revised to "ADi/DBi".
		50	Appendix 1. Package Dimensions: 100P6Q-A is added.
2.10	Jun. 24, 2005	—	Revised edition issued * The contents of product are revised. (Normal-ver. is added.) * Revised parts and revised contents are as follows (except for expressional change).
		2	Table 1.1 Performance outline of M16C/6N Group (M16C/6N4) • Performance outline of Normal-ver. is added.
		4	Table 1.2 Product List is revised. (Normal-ver. is added.) Figure 1.2 Type No., Memory Size, and Package: • "(no): Normal-ver." is added to Characteristics.
		19	Figure 4.7 SFR Information (7): NOTE 1 is revised.
		32	Table 5.4 Electrical Characteristics (1) • Measuring Condition of V_{OL} is revised from " $L_{OL} = -200\mu A$ " to " $L_{OL} = 200\mu A$ ".
		33	Table 5.5 Electrical Characteristics (2): Mask ROM (5th item) • " $f(XCIN)$ " is changed to " $f(BCLK)$ ".
		34	Table 5.6 A/D Conversion Characteristics: "Tolerance Level Impedance" is deleted.
2.40	Aug. 25, 2006	—	Revised edition issued * Electric Characteristics of Normal-ver. is added. * Revised parts and revised contents are as follows (except for expressional change).
		1	1.1 Applications: Comment of Normal-ver. is added.
		4	Table 1.2 Product Information • Status of development is revised and NOTES 1 and 2 are added.