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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306n4mgt-165fpusq

1.5 Pin Assignments

Figures 1.3 and 1.4 show the Pin Assignment (Top View). Tables 1.3 and 1.4 list the List of Pin Names.

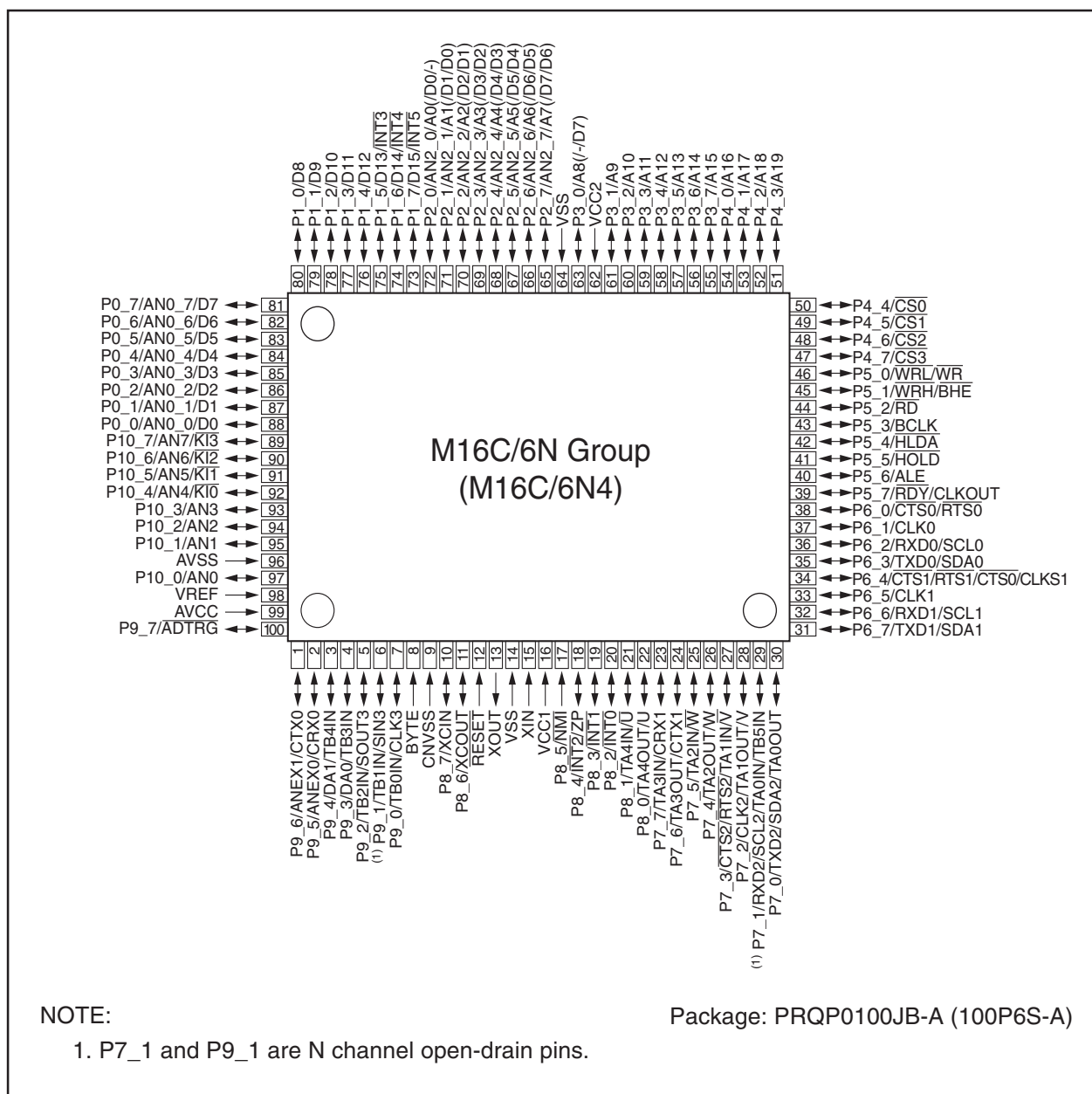


Figure 1.3 Pin Assignments (Top View) (1)

Table 4.4 SFR Information (4)

Address	Register	Symbol	After Reset
00C0h	CAN0 Message Box 6: Identifier / DLC		XXh
00C1h			XXh
00C2h			XXh
00C3h			XXh
00C4h			XXh
00C5h			XXh
00C6h	CAN0 Message Box 6: Data Field		XXh
00C7h			XXh
00C8h			XXh
00C9h			XXh
00CAh			XXh
00CBh			XXh
00CCh	CAN0 Message Box 6: Time Stamp		XXh
00CDh			XXh
00CEh	CAN0 Message Box 7: Identifier / DLC		XXh
00CFh			XXh
00D0h			XXh
00D1h			XXh
00D2h			XXh
00D3h			XXh
00D4h	CAN0 Message Box 7: Data Field		XXh
00D5h			XXh
00D6h			XXh
00D7h			XXh
00D8h			XXh
00D9h			XXh
00DAh	CAN0 Message Box 7: Time Stamp		XXh
00DBh			XXh
00DBh			XXh
00DCh			XXh
00DDh			XXh
00DEh			XXh
00DFh	CAN0 Message Box 8: Identifier / DLC		XXh
00E0h			XXh
00E1h			XXh
00E2h			XXh
00E3h			XXh
00E4h			XXh
00E5h	CAN0 Message Box 8: Data Field		XXh
00E6h			XXh
00E7h			XXh
00E8h			XXh
00E9h			XXh
00EAh			XXh
00EBh	CAN0 Message Box 8: Time Stamp		XXh
00EBh			XXh
00ECh			XXh
00EDh			XXh
00EEh			XXh
00EFh			XXh
00F0h	CAN0 Message Box 9: Identifier / DLC		XXh
00F1h			XXh
00F2h			XXh
00F3h			XXh
00F4h			XXh
00F5h			XXh
00F6h	CAN0 Message Box 9: Data Field		XXh
00F7h			XXh
00F8h			XXh
00F9h			XXh
00FAh			XXh
00FBh			XXh
00FCh	CAN0 Message Box 9: Time Stamp		XXh
00FDh			XXh
00FEh			XXh
00FFh			XXh

X: Undefined

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h	CAN0 Message Box 14: Identifier /DLC		XXh
0141h			XXh
0142h			XXh
0143h			XXh
0144h			XXh
0145h			XXh
0146h	CAN0 Message Box 14: Data Field		XXh
0147h			XXh
0148h			XXh
0149h			XXh
014Ah			XXh
014Bh			XXh
014Ch			XXh
014Dh			XXh
014Eh	CAN0 Message Box 14: Time Stamp		XXh
014Fh			XXh
0150h	CAN0 Message Box 15: Identifier /DLC		XXh
0151h			XXh
0152h			XXh
0153h			XXh
0154h			XXh
0155h			XXh
0156h	CAN0 Message Box 15: Data Field		XXh
0157h			XXh
0158h			XXh
0159h			XXh
015Ah			XXh
015Bh			XXh
015Ch			XXh
015Dh			XXh
015Eh	CAN0 Message Box 15: Time Stamp		XXh
015Fh			XXh
0160h	CAN0 Global Mask Register	C0GMR	XXh
0161h			XXh
0162h			XXh
0163h			XXh
0164h			XXh
0165h			XXh
0166h	CAN0 Local Mask A Register	C0LMAR	XXh
0167h			XXh
0168h			XXh
0169h			XXh
016Ah			XXh
016Bh			XXh
016Ch	CAN0 Local Mask B Register	C0LMBR	XXh
016Dh			XXh
016Eh			XXh
016Fh			XXh
0170h			XXh
0171h			XXh
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

- Blank spaces are reserved. No access is allowed.

Table 4.8 SFR Information (8) ⁽¹⁾

Address	Register	Symbol	After Reset
01C0h	Timer B3, B4, B5 Count Start Flag	TBSR	000XXXXXb
01C1h	Timer A1-1 Register	TA11	XXh
01C2h			XXh
01C3h			XXh
01C4h	Timer A2-1 Register	TA21	XXh
01C5h			XXh
01C6h			XXh
01C7h	Timer A4-1 Register	TA41	XXh
01C8h			XXh
01C9h			XXh
01CAh	Three-Phase PWM Control Register 0	INVC0	00h
01CBh	Three-Phase PWM Control Register 1	INVC1	00h
01CAh	Three-Phase Output Buffer Register 0	IDB0	00111111b
01CBh	Three-Phase Output Buffer Register 1	IDB1	00111111b
01CCh	Dead Time Timer	DTT	XXh
01CDh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
01CEh			
01CFh			
01D0h	Timer B3 Register	TB3	XXh
01D1h			XXh
01D2h			XXh
01D3h	Timer B4 Register	TB4	XXh
01D4h			XXh
01D5h			XXh
01D6h	Timer B5 Register	TB5	XXh
01D7h			XXh
01D8h			XXh
01D9h			
01DAh			
01DBh	Timer B3 Mode Register	TB3MR	00XX0000b
01DCh	Timer B4 Mode Register	TB4MR	00XX0000b
01DDh	Timer B5 Mode Register	TB5MR	00XX0000b
01DEh	Interrupt Source Select Register 0	IFSR0	00XX0000b
01DFh	Interrupt Source Select Register 1	IFSR1	00h
01E0h	SI/O3 Transmit/Receive Register	S3TRR	XXh
01E1h			
01E2h	SI/O3 Control Register	S3C	01000000b
01E3h	SI/O3 Bit Rate Register	S3BRG	XXh
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh	UART0 Special Mode Register 4	U0SMR4	00h
01EDh	UART0 Special Mode Register 3	U0SMR3	000X0X0Xb
01EEh	UART0 Special Mode Register 2	U0SMR2	X0000000b
01EFh	UART0 Special Mode Register 1	U0SMR1	X0000000b
01F0h	UART1 Special Mode Register 4	U1SMR4	00h
01F1h	UART1 Special Mode Register 3	U1SMR3	000X0X0Xb
01F2h	UART1 Special Mode Register 2	U1SMR2	X0000000b
01F3h	UART1 Special Mode Register 1	U1SMR1	X0000000b
01F4h	UART2 Special Mode Register 4	U2SMR4	00h
01F5h	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
01F6h	UART2 Special Mode Register 2	U2SMR2	X0000000b
01F7h	UART2 Special Mode Register 1	U2SMR1	X0000000b
01F8h	UART2 Transmit/Receive Mode Register	U2MR	00h
01F9h	UART2 Bit Rate Register	U2BRG	XXh
01FAh	UART2 Transmit Buffer Register	U2TB	XXh
01FBh			XXh
01FCh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
01FDh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
01FEh	UART2 Receive Buffer Register	U2RB	XXh
01FFh			XXh

X: Undefined

NOTE:

1. Blank spaces are reserved. No access is allowed.

Table 4.13 SFR Information (13)

Address	Register	Symbol	After Reset
0300h	CAN1 Message Box 10: Identifier / DLC		XXh
0301h			XXh
0302h			XXh
0303h			XXh
0304h			XXh
0305h	CAN1 Message Box 10: Data Field		XXh
0306h			XXh
0307h			XXh
0308h			XXh
0309h			XXh
030Ah			XXh
030Bh			XXh
030Ch	CAN1 Message Box 10: Time Stamp		XXh
030Dh			XXh
030Eh	CAN1 Message Box 11: Identifier / DLC		XXh
030Fh			XXh
0310h			XXh
0311h			XXh
0312h			XXh
0313h	CAN1 Message Box 11: Data Field		XXh
0314h			XXh
0315h			XXh
0316h			XXh
0317h			XXh
0318h			XXh
0319h			XXh
031Ah	CAN1 Message Box 11: Time Stamp		XXh
031Bh			XXh
031Ch	CAN1 Message Box 12: Identifier / DLC		XXh
031Dh			XXh
031Eh			XXh
031Fh			XXh
0320h			XXh
0321h	CAN1 Message Box 12: Data Field		XXh
0322h			XXh
0323h			XXh
0324h			XXh
0325h			XXh
0326h			XXh
0327h			XXh
0328h	CAN1 Message Box 12: Time Stamp		XXh
0329h			XXh
032Ah	CAN1 Message Box 13: Identifier / DLC		XXh
032Bh			XXh
032Ch			XXh
032Dh			XXh
032Eh			XXh
032Fh	CAN1 Message Box 13: Data Field		XXh
0330h			XXh
0331h			XXh
0332h			XXh
0333h			XXh
0334h			XXh
0335h			XXh
0336h	CAN1 Message Box 13: Time Stamp		XXh
0337h			XXh
0338h	CAN1 Message Box 13: Data Field		XXh
0339h			XXh
033Ah			XXh
033Bh			XXh
033Ch			XXh
033Dh	CAN1 Message Box 13: Time Stamp		XXh
033Eh			XXh
033Fh			XXh

X: Undefined

Table 4.16 SFR Information (16) ⁽²⁾

Address	Register	Symbol	After Reset
03C0h	A/D Register 0	AD0	XXh
03C1h			XXh
03C2h			XXh
03C3h	A/D Register 1	AD1	XXh
03C4h			XXh
03C5h	A/D Register 2	AD2	XXh
03C6h			XXh
03C7h	A/D Register 3	AD3	XXh
03C8h			XXh
03C9h			XXh
03CAh	A/D Register 4	AD4	XXh
03CBh			XXh
03CCh	A/D Register 5	AD5	XXh
03CDh			XXh
03CEh	A/D Register 6	AD6	XXh
03CFh			XXh
03D0h			XXh
03D1h	A/D Register 7	AD7	XXh
03D2h			XXh
03D3h			XXh
03D4h	A/D Control Register 2	ADCON2	00h
03D5h	A/D Control Register 0	ADCON0	00000XXXb
03D6h			00h
03D7h	A/D Control Register 1	ADCON1	00h
03D8h	D/A Register 0	DA0	00h
03D9h	D/A Register 1	DA1	00h
03DAh			00h
03DBh			00h
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P10 Direction Register	PD10	00h
03F6h			
03F7h			
03F8h			
03F9h			
03FAh			
03FBh	Pull-up Control Register 0	PUR0	00h
03FCh			
03FDh			
03FEh	Pull-up Control Register 1	PUR1	00000000b ⁽¹⁾
03FFh	Pull-up Control Register 2	PUR2	0000010b
	Port Control Register	PCR	00h

X: Undefined

NOTES:

1. At hardware reset, the register is as follows:

- 00000000b where "L" is input to the CNVSS pin
- 00000010b where "H" is input to the CNVSS pin

At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:

- 00000000b where bits PM01 to PM00 in the PM0 register are 00b (single-chip mode)
- 00000010b where bits PM01 to PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode)

2. Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Electrical Characteristics (T/V-ver.)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC}	Supply voltage (VCC1 = VCC2)		VCC = AVCC	−0.3 to 6.5	V
AV _{CC}	Analog supply voltage		VCC = AVCC	−0.3 to 6.5	V
V _I	Input voltage	RESET, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, VREF, XIN		−0.3 to VCC+0.3	V
		P7_1, P9_1		−0.3 to 6.5	V
V _O	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, XOUT		−0.3 to VCC+0.3	V
		P7_1, P9_1		−0.3 to 6.5	V
P _d	Power dissipation		T _{opr} = 25°C	700	mW
T _{opr}	Operating ambient temperature	During MCU operation		T version: −40 to 85 V version: −40 to 125 (option)	°C
		During flash memory program and erase operation		0 to 60	
T _{stg}	Storage temperature			−65 to 150	°C

option: All options are on request basis.

Table 5.6 A/D Conversion Characteristics ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		VREF = VCC				10	Bit
INL	Integral nonlinearity error	10 bits	VREF = VCC	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
			= 5 V	External operation amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 5 V				±2	LSB
—	Absolute accuracy	10 bits	VREF = VCC	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
			= 5 V	External operation amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 5 V				±2	LSB
DNL	Differential nonlinearity error						±1	LSB
—	Offset error						±3	LSB
—	Gain error						±3	LSB
R _{LADDER}	Resistor ladder		VREF = VCC		10		40	kΩ
t _{CONV}	10-bit conversion time, sample & hold available		VREF = VCC = 5 V, φAD = 10 MHz		3.3			μs
	8-bit conversion time, sample & hold available		VREF = VCC = 5 V, φAD = 10 MHz		2.8			μs
t _{SAMP}	Sampling time				0.3			μs
V _{REF}	Reference voltage				2.0		V _{CC}	V
V _{IA}	Analog input voltage				0		V _{REF}	V

NOTES:

1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, -40 to 85°C unless otherwise specified.
2. φAD frequency must be 10 MHz or less.
3. When sample & hold is disabled, φAD frequency must be 250kHz or more in addition to a limit of NOTE 2.
When sample & hold is enabled, φAD frequency must be 1MHz or more in addition to a limit of NOTE 2.

Table 5.7 D/A conversion Characteristics ⁽¹⁾

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
t _{su}	Setup time				3	μs
R _o	Output resistance		4	10	20	kΩ
I _{VREF}	Reference power supply input current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to VCC = AVCC = VREF = 4.2 to 5.5 V, VSS = AVSS = 0 V, -40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the DAi register (i = 0, 1) for the unused D/A converter set to 00h.
The resistor ladder of the A/D converter is not included. Also, the I_{VREF} will flow even if VREF is disconnected by the ADCON1 register.

Switching Characteristics**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.25 Memory Expansion Mode and Microprocessor Mode
(for 2- to 3-wait setting, external area access and multiplexed bus selection)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 5.2		25	ns
t _h (BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (in relation to RD)		(NOTE 1)		ns
t _h (WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip select output delay time			25	ns
t _h (BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
t _h (RD-CS)	Chip select output hold time (in relation to RD)		(NOTE 1)		ns
t _h (WR-CS)	Chip select output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-RD)	RD signal output delay time			25	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			25	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (in relation to BCLK)		4		ns
t _d (DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA output delay time			40	ns
t _d (BCLK-ALE)	ALE signal output delay time (in relation to BCLK)			15	ns
t _h (BCLK-ALE)	ALE signal output hold time (in relation to BCLK)		–4		ns
t _d (AD-ALE)	ALE signal output delay time (in relation to Address)		(NOTE 3)		ns
t _h (ALE-AD)	ALE signal output hold time (in relation to Address)		(NOTE 4)		ns
t _d (AD-RD)	RD signal output delay from the end of Address		0		ns
t _d (AD-WR)	WR signal output delay from the end of Address		0		ns
t _{dZ} (RD-AD)	Address output floating start time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]} \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 25 \text{ [ns]}$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 15 \text{ [ns]}$$

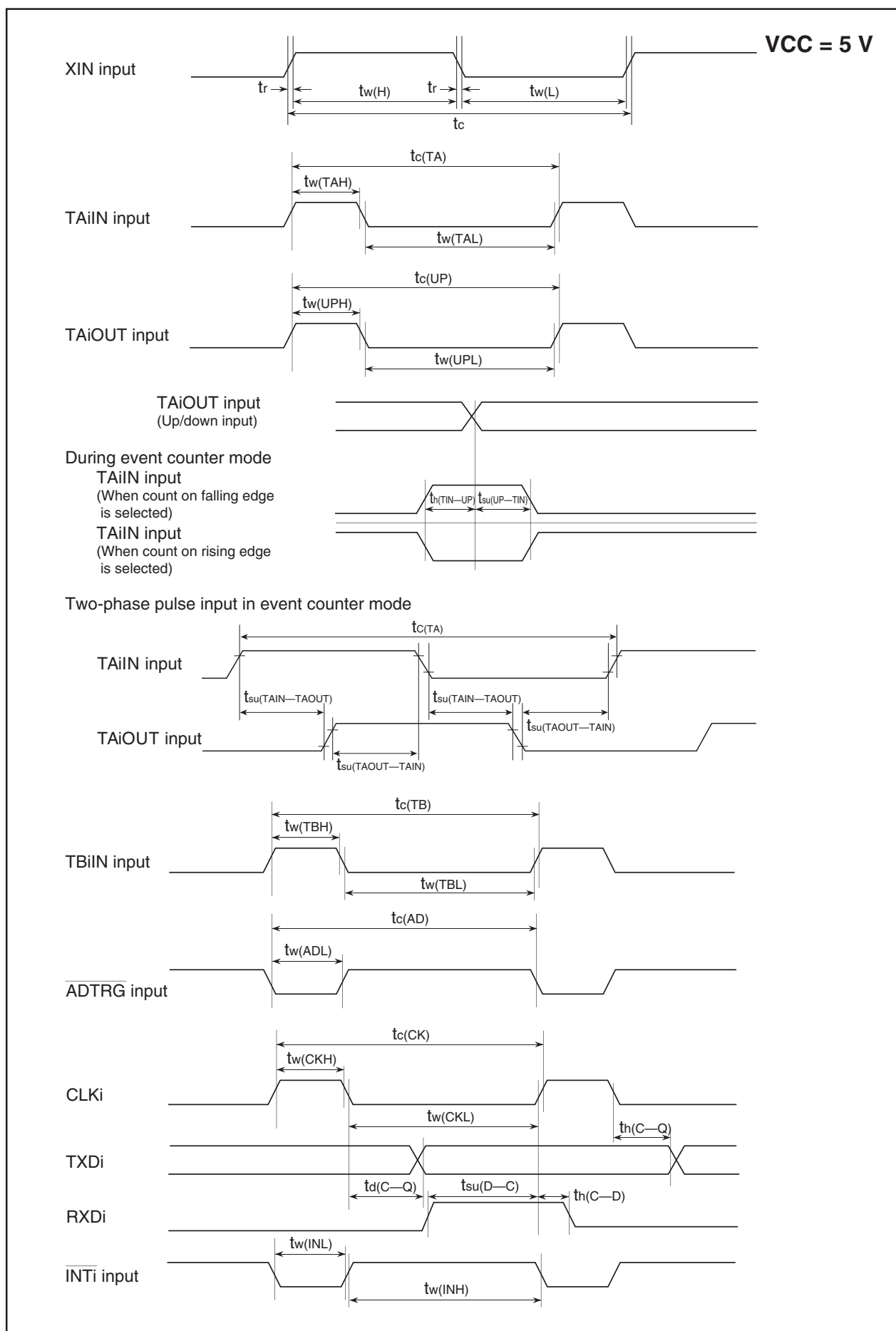


Figure 5.3 Timing Diagram (1)

Table 5.27 Recommended Operating Conditions (1) ⁽¹⁾

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage (V _{CC1} = V _{CC2})		3.0	5.0	5.5	V
AV _{CC}	Analog supply voltage			V _{CC}		V
V _{SS}	Supply voltage			0		V
AV _{SS}	Analog supply voltage			0		V
V _{IH}	HIGH input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	0.8 V _{CC}		V _{CC}	V
		P7_1, P9_1	0.8 V _{CC}		6.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode)	0.8 V _{CC}		V _{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes)	0.5 V _{CC}		V _{CC}	V
V _{IL}	LOW input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	0		0.2 V _{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (During single-chip mode)	0		0.2 V _{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (Data input during memory expansion and microprocessor modes)	0		0.16 V _{CC}	V
I _{OH(peak)}	HIGH peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7			−10.0	mA
I _{OH(avg)}	HIGH average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7			−5.0	mA
I _{OL(peak)}	LOW peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
I _{OL(avg)}	LOW average output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA

NOTES:

1. Referenced to V_{CC} = 3.0 to 5.5 V at T_{opr} = −40 to 85°C unless otherwise specified.
2. Average output current values during 100 ms period.
3. The total I_{OL(peak)} for ports P0, P1, P2, P8_6, P8_7, P9, and P10 must be 80 mA max.
The total I_{OL(peak)} for ports P3, P4, P5, P6, P7, and P8_0 to P8_4 must be 80 mA max.
The total I_{OH(peak)} for ports P0, P1, and P2 must be −40 mA max.
The total I_{OH(peak)} for ports P3, P4, and P5 must be −40 mA max.
The total I_{OH(peak)} for ports P6, P7, and P8_0 to P8_4 must be −40 mA max.
The total I_{OH(peak)} for ports P8_6, P8_7, P9, and P10 must be −40 mA max.

Table 5.31 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	$V_{CC} = 3.0 \text{ to } 5.5 \text{ V}$			2	ms
$t_{d(R-S)}$	STOP release time				150	μs
$t_{d(W-S)}$	Low power dissipation mode wait mode release time				150	μs

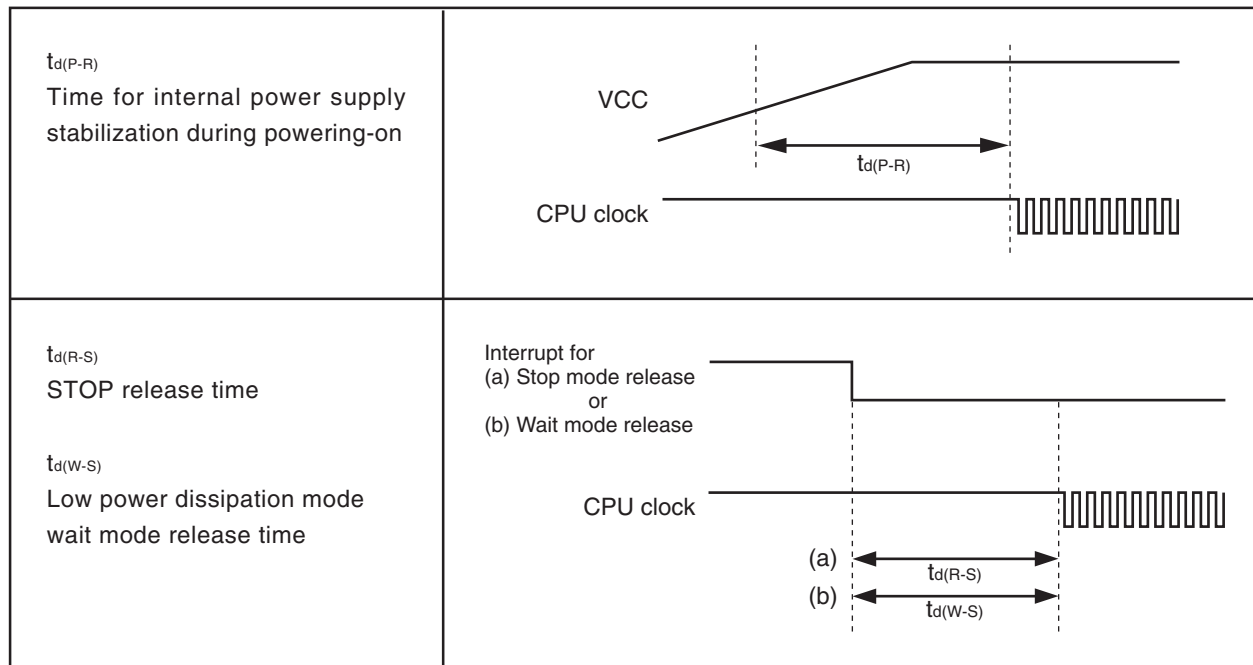
**Figure 5.11 Power Supply Circuit Timing Diagram**

Table 5.32 Electrical Characteristics (1) ⁽¹⁾

VCC = 5 V

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	I _{OH} = -5 mA	V _{CC} -2.0		V _{CC}	V
V _{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	I _{OH} = -200 μA	V _{CC} -0.3		V _{CC}	V
V _{OH}	HIGH output voltage	XOUT	HIGHPOWER	I _{OH} = -1 mA	3.0	V _{CC}	V
			LOWPOWER	I _{OH} = -0.5 mA	3.0	V _{CC}	V
	HIGH output voltage	XCOUT	HIGHPOWER	With no load applied	2.5		V
			LOWPOWER	With no load applied	1.6		V
V _{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OL} = 5 mA			2.0	V
V _{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OL} = 200 μA			0.45	V
V _{OL}	LOW output voltage	XOUT	HIGHPOWER	I _{OL} = 1 mA		2.0	V
			LOWPOWER	I _{OL} = 0.5 mA		2.0	V
	LOW output voltage	XCOUT	HIGHPOWER	With no load applied	0		V
			LOWPOWER	With no load applied	0		V
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK3, TA0OUT to TA4OUT, $\overline{\text{KI}}$ 0 to $\overline{\text{KI}}$ 3, RXD0 to RXD2, SIN3		0.2		1.0	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		2.5	V
I _{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I = 5 V			5.0	μA
I _{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I = 0 V			-5.0	μA
R _{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	V _I = 0 V	30	50	170	kΩ
R _{FXIN}	Feedback resistance	XIN			1.5		MΩ
R _{FXCIN}	Feedback resistance	XCIN			15		MΩ
V _{RAM}	RAM retention voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC = 4.2 to 5.5 V, VSS = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.

Table 5.33 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I _{cc}	Power supply current (VCC = 3.0 to 5.5 V)	In single-chip mode, the output pins are open and other pins are VSS.	Mask ROM	f(BCLK) = 24 MHz, PLL operation, No division		20	36	mA
				On-chip oscillation, No division		1		mA
			Flash memory	f(BCLK) = 24 MHz, PLL operation, No division		22	38	mA
				On-chip oscillation, No division		1.8		mA
			Flash memory program	f(BCLK) = 10 MHz, VCC = 5 V		15		mA
			Flash memory erase	f(BCLK) = 10 MHz, VCC = 5 V		25		mA
			Mask ROM	f(BCLK) = 32 kHz, Low power dissipation mode, ROM ⁽²⁾		25		μA
			Flash memory	f(BCLK) = 32 kHz, Low power dissipation mode, RAM ⁽²⁾		25		μA
				f(BCLK) = 32 kHz, Low power dissipation mode, Flash memory ⁽²⁾		420		μA
			Mask ROM Flash memory	On-chip oscillation, Wait mode		50		μA
				f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity High		8.5		μA
				f(BCLK) = 32 kHz, Wait mode ⁽³⁾ , Oscillation capacity Low		3.0		μA
				Stop mode, T _{opr} = 25°C		0.8	3.0	μA

NOTES:

1. Referenced to VCC = 3.0 to 5.5 V, VSS = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

Switching Characteristics**VCC = 5 V****(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)****Table 5.49 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)**

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
t _d (BCLK-AD)	Address output delay time	Figure 5.12		25	ns
t _h (BCLK-AD)	Address output hold time (in relation to BCLK)		4		ns
t _h (RD-AD)	Address output hold time (in relation to RD)		0		ns
t _h (WR-AD)	Address output hold time (in relation to WR)		(NOTE 1)		ns
t _d (BCLK-CS)	Chip select output delay time			25	ns
t _h (BCLK-CS)	Chip select output hold time (in relation to BCLK)		4		ns
t _d (BCLK-ALE)	ALE signal output delay time			15	ns
t _h (BCLK-ALE)	ALE signal output hold time		–4		ns
t _d (BCLK-RD)	RD signal output delay time			25	ns
t _h (BCLK-RD)	RD signal output hold time		0		ns
t _d (BCLK-WR)	WR signal output delay time			25	ns
t _h (BCLK-WR)	WR signal output hold time		0		ns
t _d (BCLK-DB)	Data output delay time (in relation to BCLK)			40	ns
t _h (BCLK-DB)	Data output hold time (in relation to BCLK) ⁽³⁾		4		ns
t _d (DB-WR)	Data output delay time (in relation to WR)		(NOTE 2)		ns
t _h (WR-DB)	Data output hold time (in relation to WR) ⁽³⁾		(NOTE 1)		ns
t _d (BCLK-HLDA)	HLDA output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(\text{BCLK})} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(\text{BCLK})} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

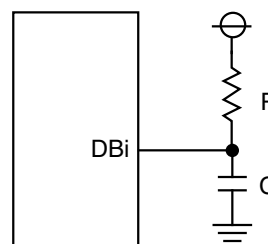
$$t = -CR \times \ln(1 - V_{OL} / V_{CC})$$

by a circuit of the right figure.

For example, when V_{OL} = 0.2 V_{CC}, C = 30 pF,

R = 1 kΩ, hold time of output “L” level is

$$t = -30 \text{ pF} \times 1 \text{ k}\Omega \times \ln(1 - 0.2 V_{CC} / V_{CC}) = 6.7 \text{ ns.}$$



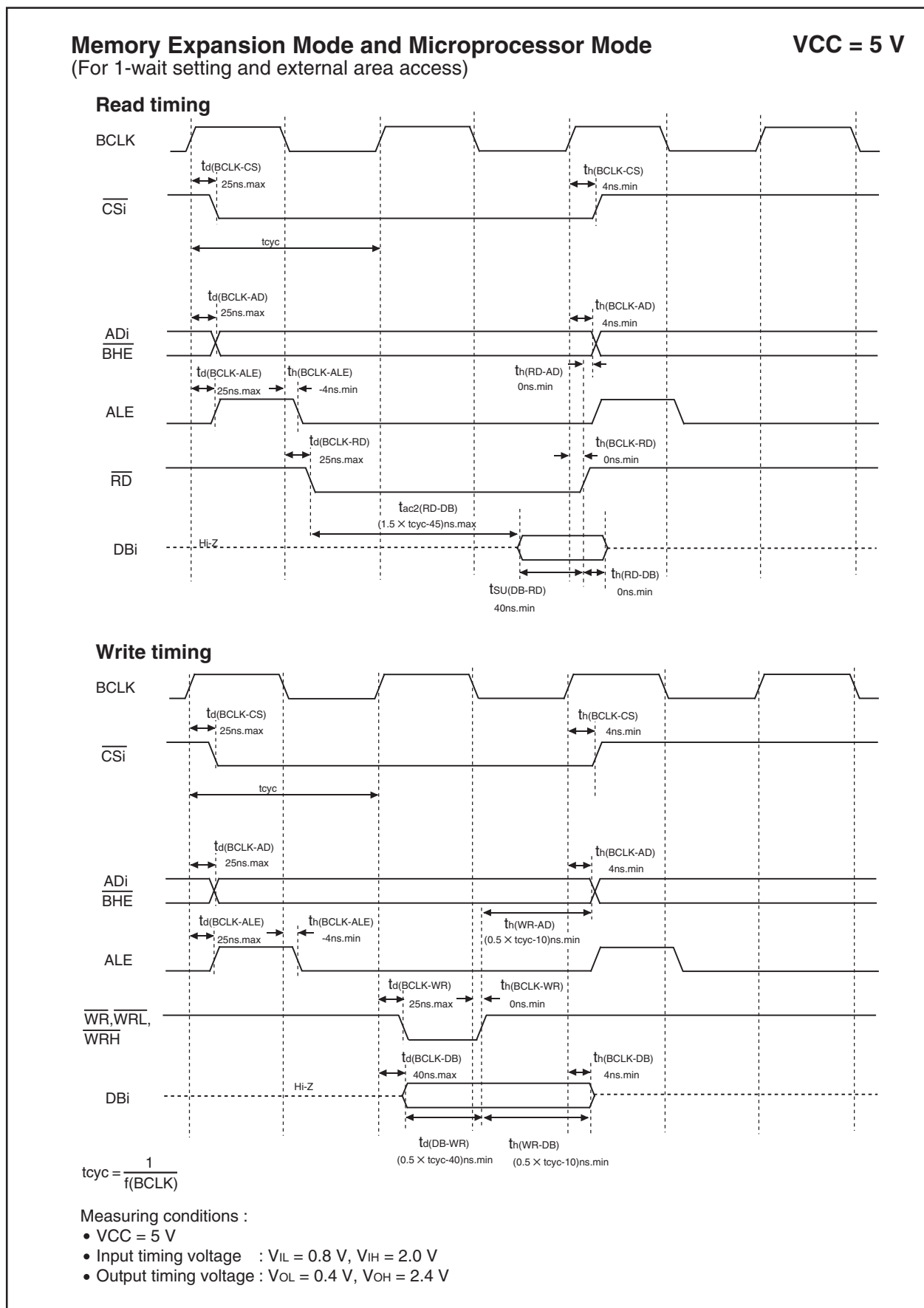


Figure 5.16 Timing Diagram (4)

Table 5.51 Electrical Characteristics ⁽¹⁾**VCC = 3.3 V**

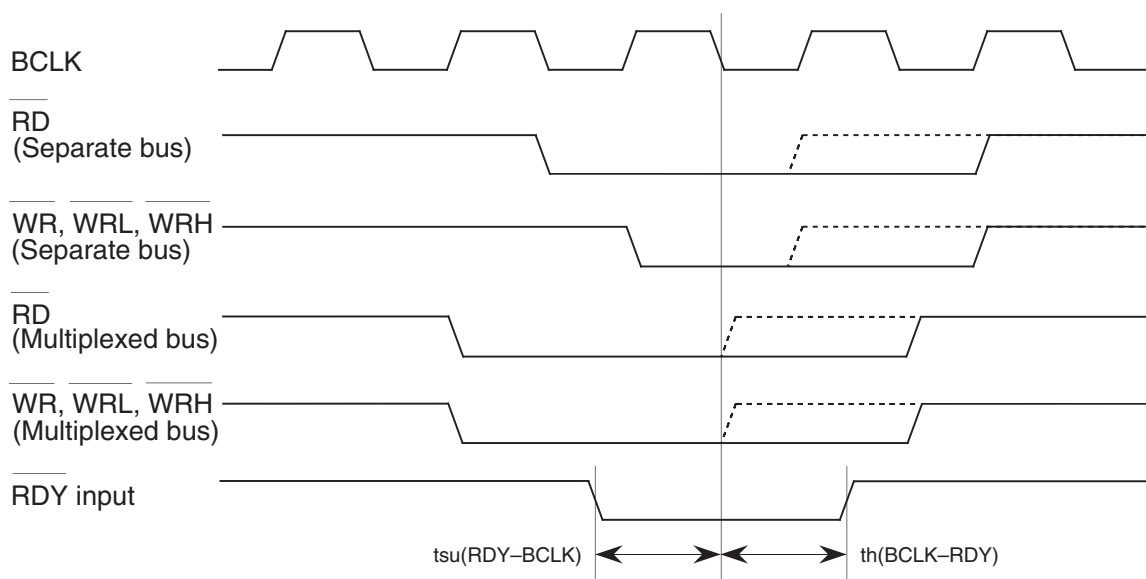
Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	I _{OH} = -1 mA	V _{CC} -0.5		V _{CC}	V
V _{OH}	HIGH output voltage	XOUT	HIGHPOWER	I _{OH} = -0.1 mA	V _{CC} -0.5	V _{CC}	V
			LOWPOWER	I _{OH} = -50 μA	V _{CC} -0.5	V _{CC}	
	HIGH output voltage	XCOUT	HIGHPOWER	With no load applied	2.5		V
			LOWPOWER	With no load applied	1.6		
V _{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	I _{OL} = 1 mA			0.5	V
V _{OL}	LOW output voltage	XOUT	HIGHPOWER	I _{OL} = 0.1 mA		0.5	V
			LOWPOWER	I _{OL} = 50 μA		0.5	
	LOW output voltage	XCOUT	HIGHPOWER	With no load applied	0		V
			LOWPOWER	With no load applied	0		
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS2, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK3, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD2, SIN3		0.2		0.8	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		1.8	V
I _{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I = 3.3 V			4.0	μA
I _{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, BYTE	V _I = 0 V			-4.0	μA
R _{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7	V _I = 0 V	50	100	500	kΩ
R _{IXIN}	Feedback resistance	XIN			3.0		MΩ
R _{IXCIN}	Feedback resistance	XCIN			25		MΩ
V _{RAM}	RAM retention voltage		At stop mode	2.0			V

NOTES:

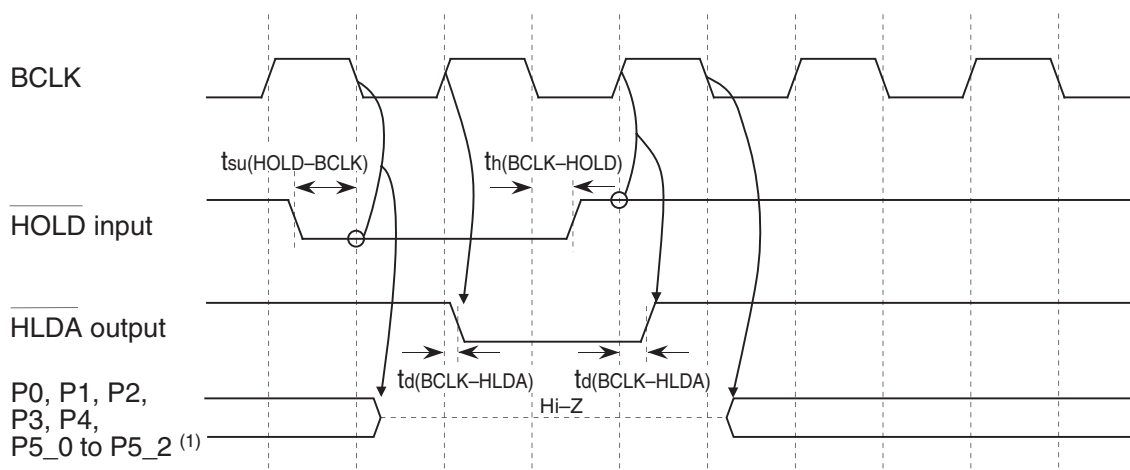
1. Referenced to VCC = 3.0 to 3.6 V, VSS = 0 V at T_{opr} = -40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.

Memory Expansion Mode and Microprocessor Mode**VCC = 3.3 V**

(Effective for setting with wait)



(Common to setting with wait and setting without wait)

**NOTE:**

1. The above pins are set to high-impedance regardless of the input level of the BYTE pin, the PM06 bit in the PM0 register, and the PM11 bit in the PM1 register.

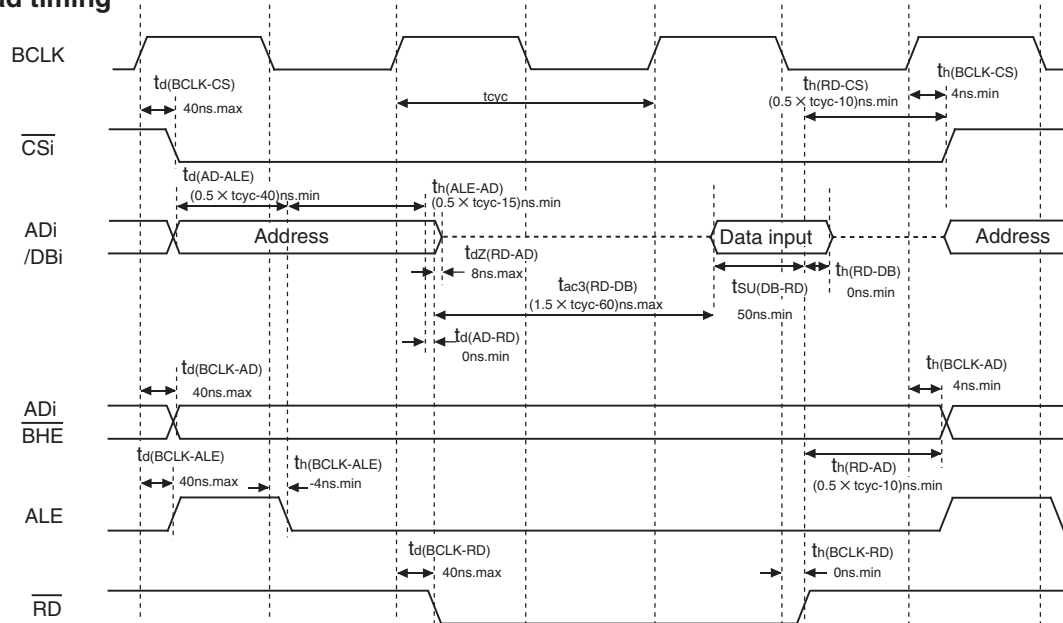
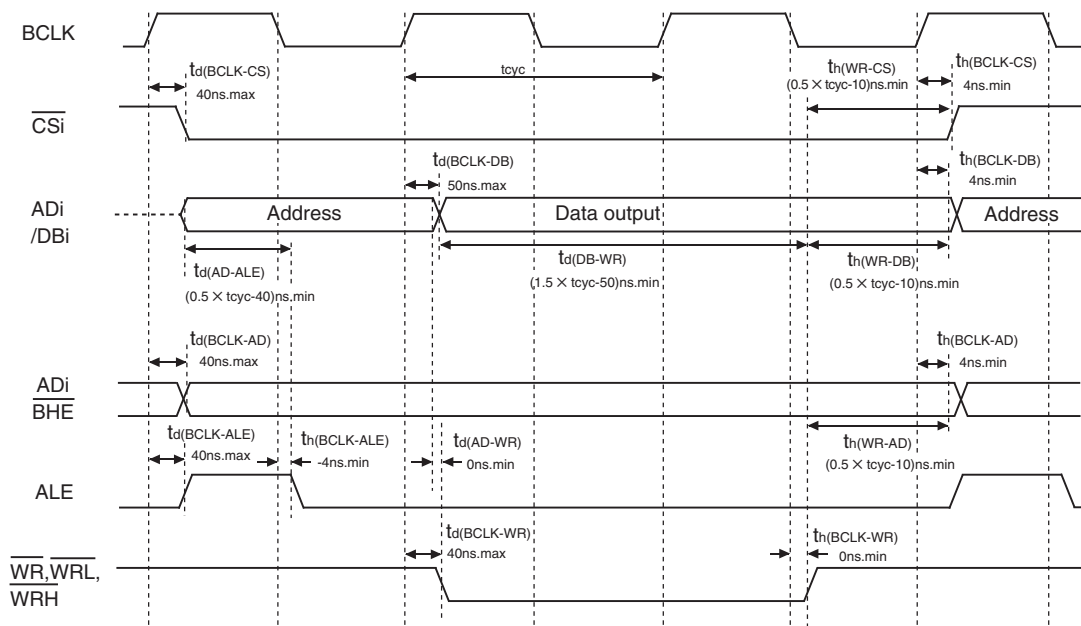
Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : Determined with $V_{IL} = 0.6 \text{ V}$, $V_{IH} = 2.7 \text{ V}$
- Output timing voltage: Determined with $V_{OL} = 1.65 \text{ V}$, $V_{OH} = 1.65 \text{ V}$

Figure 5.23 Timing Diagram (2)

Memory Expansion Mode and Microprocessor Mode**VCC = 3.3 V**

(For 2-wait setting, external area access and multiplexed bus selection)

Read timing**Write timing**

$$t_{cy} = \frac{1}{f(\text{BCLK})}$$

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : $V_{IL} = 0.6 \text{ V}$, $V_{IH} = 2.7 \text{ V}$
- Output timing voltage : $V_{OL} = 1.65 \text{ V}$, $V_{OH} = 1.65 \text{ V}$

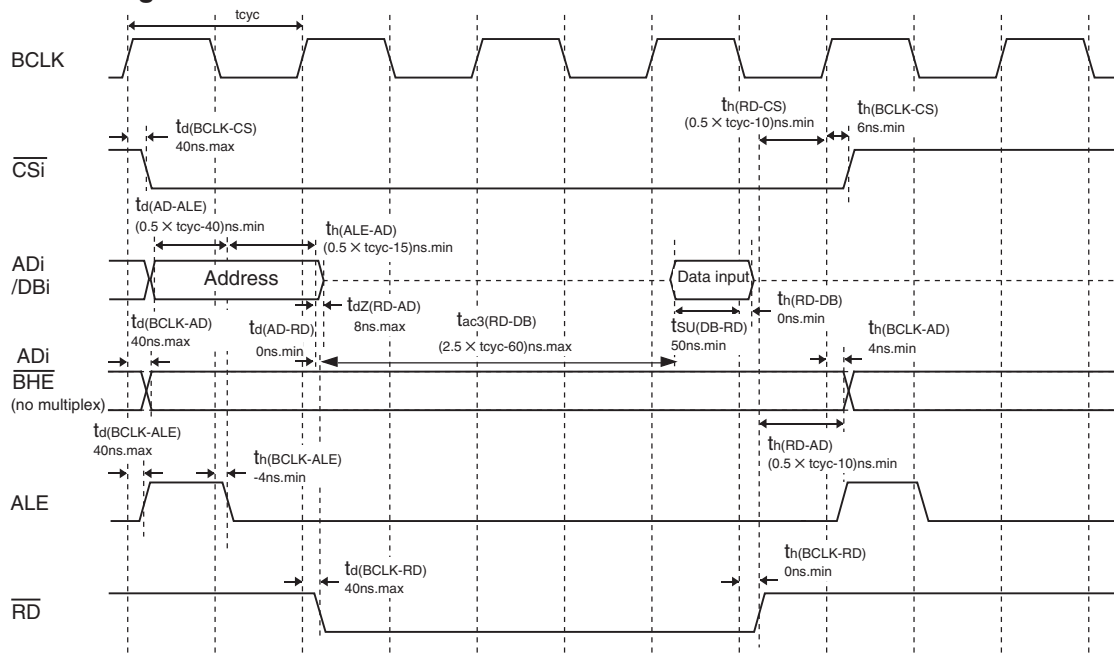
Figure 5.28 Timing Diagram (7)

Memory Expansion Mode and Microprocessor Mode

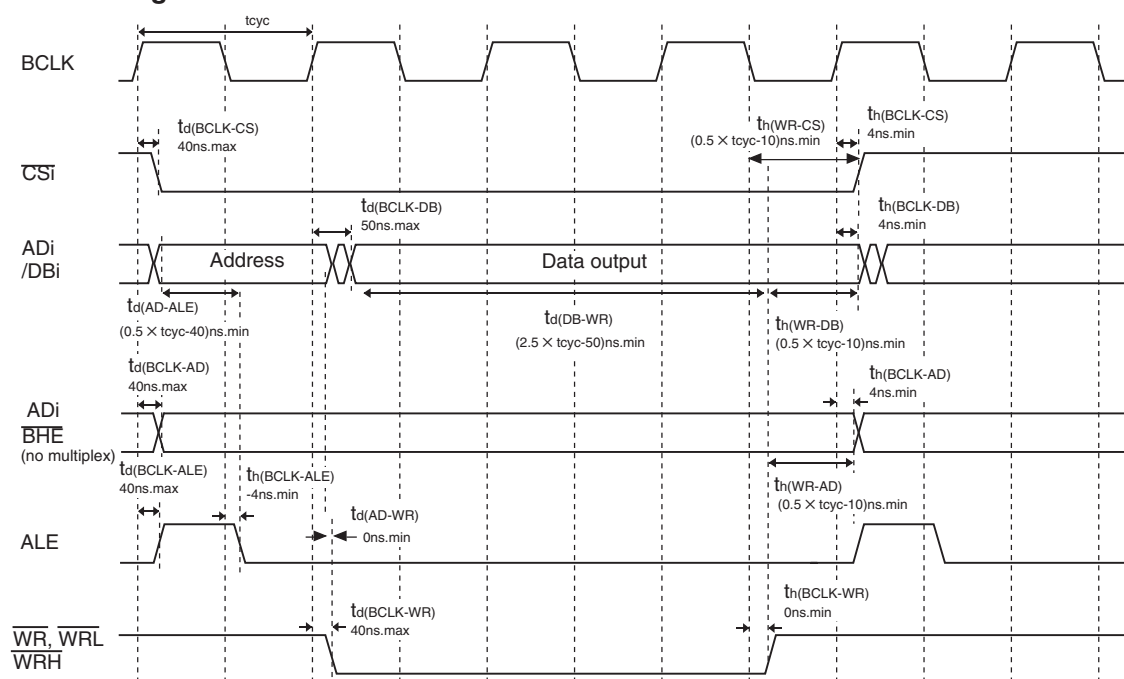
(For 3-wait setting, external area access and multiplexed bus selection)

VCC = 3.3 V

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : $V_{IL} = 0.6$ V, $V_{IH} = 2.7$ V
- Output timing voltage : $V_{OL} = 1.65$ V, $V_{OH} = 1.65$ V

Figure 5.29 Timing Diagram (8)