Renesas Electronics America Inc - M306N4MGT-173FPUFQ Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m306n4mgt-173fpufq

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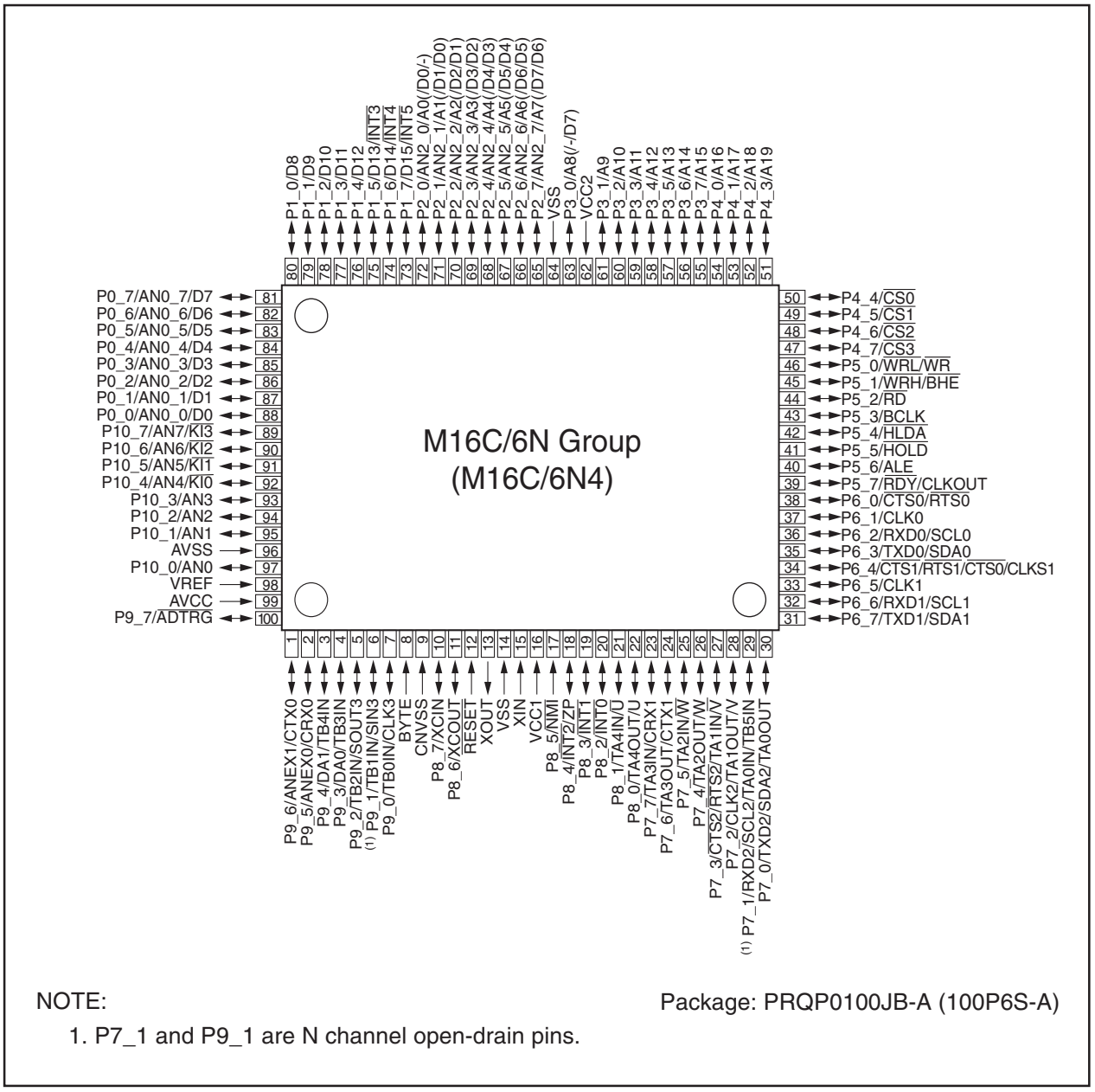
1.5 Pin Assignments

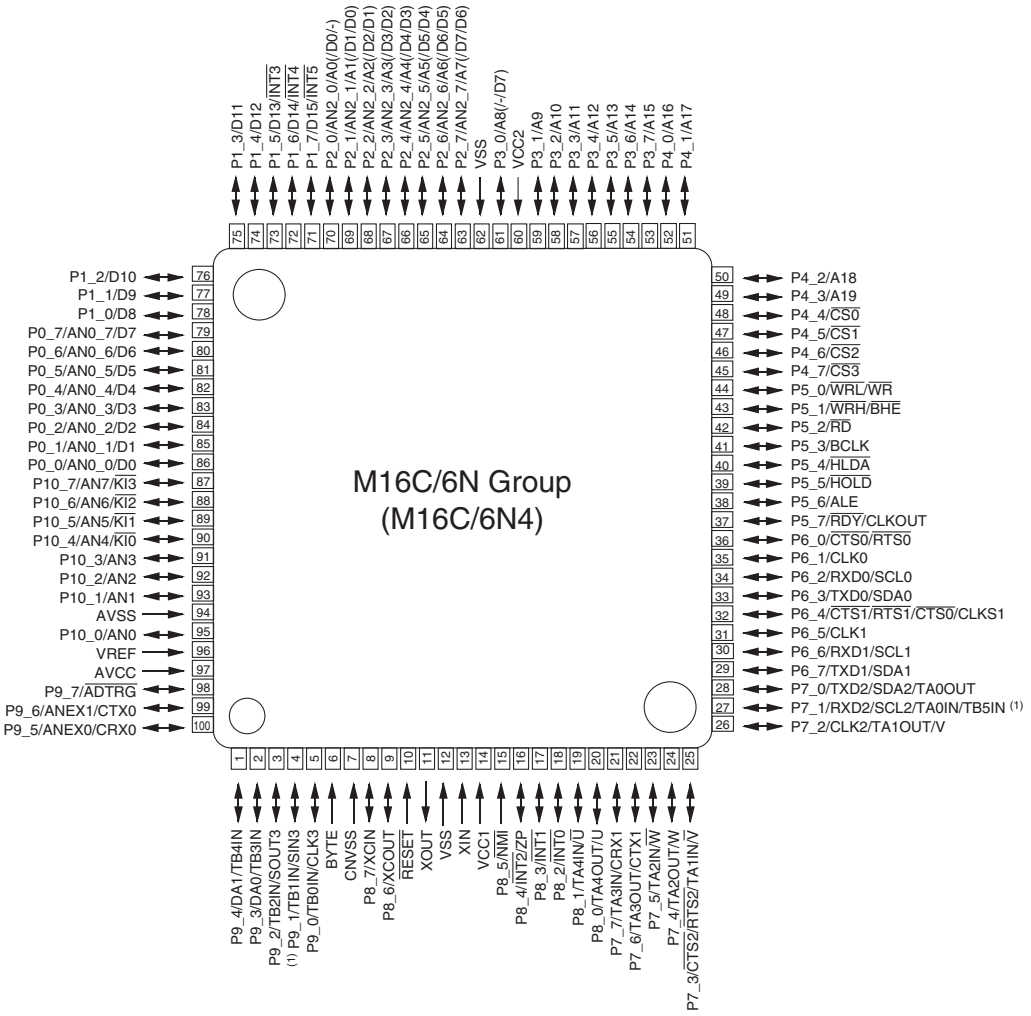
Figures 1.3 and 1.4 show the Pin Assignment (Top View). Tables 1.3 and 1.4 list the List of Pin Names.



NOTE:
1. P7_1 and P9_1 are N channel open-drain pins.

Package: PRQP0100JB-A (100P6S-A)

Figure 1.3 Pin Assignments (Top View) (1)



NOTE: Package: PLQP0100KB-A (100P6Q-A)

1. P7_1 and P9_1 are N channel open-drain pins.

Figure 1.4 Pin Assignments (Top View) (2)

Table 1.6 Pin Functions (2)

Signal Name	Pin Name	I/O Type	Description
Main clock input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (1).
Main clock output	XOUT	O	To use the external clock, input the clock from XIN and leave XOUT open.
Sub clock input	XCIN	I	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (1).
Sub clock output	XCOUT	O	To use the external clock, input the clock from XCIN and leave XCOUT open.
BCLK output	BCLK	O	Outputs the BCLK signal.
Clock output	CLKOUT	O	The clock of the same cycle as fC, f8, or f32 is output.
INT interrupt input	INT0 to INT5	I	Input pins for the INT interrupt.
NMI interrupt input	NMI	I	Input pin for the NMI interrupt.
Key input interrupt input	KI0 to KI3	I	Input pins for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	These are timer A0 to timer A4 I/O pins.
	TA0IN to TA4IN	I	These are timer A0 to timer A4 input pins.
	ZP	I	Input pin for the Z-phase.
Timer B	TB0IN to TB5IN	I	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, U, V, V, W, W	O	These are Three-phase motor control output pins.
Serial interface	CTS0 to CTS2	I	These are transmit control input pins.
	RTS0 to RTS2	O	These are receive control output pins.
	CLK0 to CLK3	I/O	These are transfer clock I/O pins.
	RXD0 to RXD2	I	These are serial data input pins.
	SIN3	I	These are serial data input pins.
	TXD0 to TXD2	O	These are serial data output pins.
	SOUT3	O	These are serial data output pins.
	CLKS1	O	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	These are serial data I/O pins.
	SCL0 to SCL2	I/O	These are transfer clock I/O pins. (however, SCL2 for the N-channel open drain output.)
Reference voltage input	VREF	I	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7 AN0_0 to AN0_7 AN2_0 to AN2_7	I	Analog input pins for the A/D converter.
	ADTRG	I	This is an A/D trigger input pin.
	ANEX0	I/O	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	These are the output pins for the D/A converter.
CAN module	CRX0, CRX1	I	These are the input pins for the CAN module.
	CTX0, CTX1	O	These are the output pins for the CAN module.

I: Input O: Output I/O: Input/Output

NOTE:
1. Ask the oscillator maker the oscillation characteristic.

3. Memory

Figure 3.1 shows a Memory Map. The address space extends the 1 Mbyte from address 00000h to FFFFFh. The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 128-Kbyte internal ROM is allocated to the addresses from E0000h to FFFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

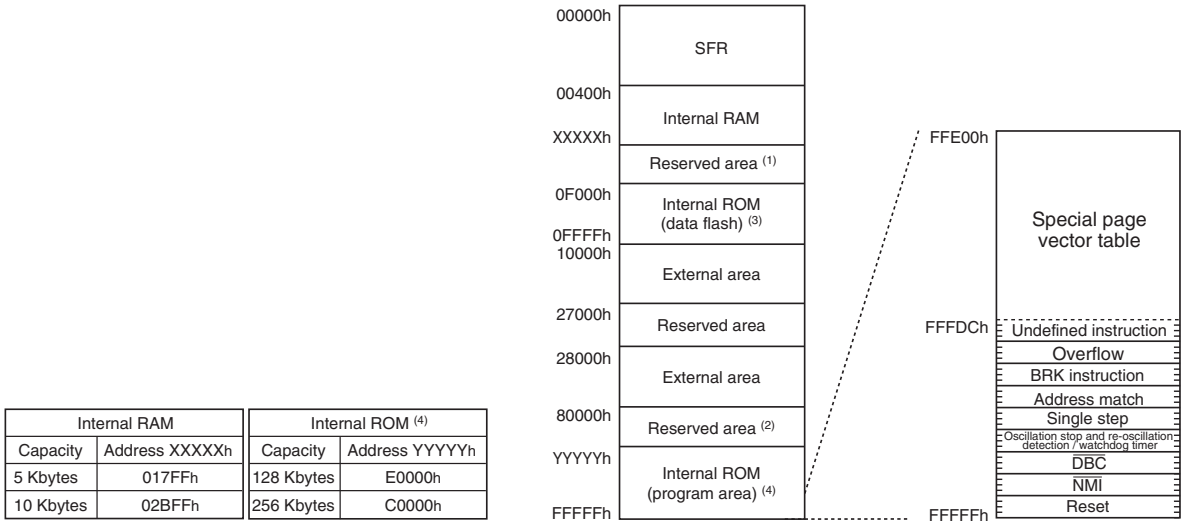
The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 5-Kbyte internal RAM is allocated to the addresses from 00400h to 017FFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The Special Function Registers (SFRs) are allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be accessed by user.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to **M16C/60, M16C/20, M16C/Tiny Series Software Manual**.

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.



Internal RAM		Internal ROM (4)	
Capacity	Address XXXXXh	Capacity	Address YYYYYh
5 Kbytes	017FFh	128 Kbytes	E0000h
10 Kbytes	02BFFh	256 Kbytes	C0000h

NOTES:
1. During memory expansion mode or microprocessor mode, cannot be used.
2. In memory expansion mode, cannot be used.
3. As for the flash memory version, 4-Kbyte space (block A) exists.
4. When using the masked ROM version, write nothing to internal ROM area.
5. Shown here is a memory map for the case where the PM10 bit in the PM1 register is 1 (block A enabled, addresses 10000h to 26FFFh for $\overline{CS2}$ area) and the PM13 bit in the PM1 register is 1 (internal RAM area is expanded over 192 Kbytes).

Figure 3.1 Memory Map

Table 4.4 SFR Information (4)

Address	Register	Symbol	After Reset
00C0h	CAN0 Message Box 6: Identifier / DLC		XXh
00C1h			XXh
00C2h			XXh
00C3h			XXh
00C4h			XXh
00C5h			XXh
00C6h	CAN0 Message Box 6: Data Field		XXh
00C7h			XXh
00C8h			XXh
00C9h			XXh
00CAh			XXh
00CBh			XXh
00CCh			XXh
00CDh			XXh
00CEh	CAN0 Message Box 6: Time Stamp		XXh
00CFh			XXh
00D0h	CAN0 Message Box 7: Identifier / DLC		XXh
00D1h			XXh
00D2h			XXh
00D3h			XXh
00D4h			XXh
00D5h			XXh
00D6h	CAN0 Message Box 7: Data Field		XXh
00D7h			XXh
00D8h			XXh
00D9h			XXh
00DAh			XXh
00DBh			XXh
00DCh			XXh
00DDh			XXh
00DEh	CAN0 Message Box 7: Time Stamp		XXh
00DFh			XXh
00E0h	CAN0 Message Box 8: Identifier / DLC		XXh
00E1h			XXh
00E2h			XXh
00E3h			XXh
00E4h			XXh
00E5h			XXh
00E6h	CAN0 Message Box 8: Data Field		XXh
00E7h			XXh
00E8h			XXh
00E9h			XXh
00EAh			XXh
00EBh			XXh
00ECh			XXh
00EDh			XXh
00EEh	CAN0 Message Box 8: Time Stamp		XXh
00EFh			XXh
00F0h	CAN0 Message Box 9: Identifier / DLC		XXh
00F1h			XXh
00F2h			XXh
00F3h			XXh
00F4h			XXh
00F5h			XXh
00F6h	CAN0 Message Box 9: Data Field		XXh
00F7h			XXh
00F8h			XXh
00F9h			XXh
00FAh			XXh
00FBh			XXh
00FCh			XXh
00FDh			XXh
00FEh	CAN0 Message Box 9: Time Stamp		XXh
00FFh			XXh

X: Undefined

Table 4.9 SFR Information (9)

Address	Register	Symbol	After Reset
0200h	CAN0 Message Control Register 0	C0MCTL0	00h
0201h	CAN0 Message Control Register 1	C0MCTL1	00h
0202h	CAN0 Message Control Register 2	C0MCTL2	00h
0203h	CAN0 Message Control Register 3	C0MCTL3	00h
0204h	CAN0 Message Control Register 4	C0MCTL4	00h
0205h	CAN0 Message Control Register 5	C0MCTL5	00h
0206h	CAN0 Message Control Register 6	C0MCTL6	00h
0207h	CAN0 Message Control Register 7	C0MCTL7	00h
0208h	CAN0 Message Control Register 8	C0MCTL8	00h
0209h	CAN0 Message Control Register 9	C0MCTL9	00h
020Ah	CAN0 Message Control Register 10	C0MCTL10	00h
020Bh	CAN0 Message Control Register 11	C0MCTL11	00h
020Ch	CAN0 Message Control Register 12	C0MCTL12	00h
020Dh	CAN0 Message Control Register 13	C0MCTL13	00h
020Eh	CAN0 Message Control Register 14	C0MCTL14	00h
020Fh	CAN0 Message Control Register 15	C0MCTL15	00h
0210h	CAN0 Control Register	C0CTLR	X0000001b
0211h			XX0X0000b
0212h	CAN0 Status Register	C0STR	00h
0213h			X0000001b
0214h	CAN0 Slot Status Register	C0SSTR	00h
0215h			00h
0216h	CAN0 Interrupt Control Register	C0ICR	00h
0217h			00h
0218h	CAN0 Extended ID Register	C0IDR	00h
0219h			00h
021Ah	CAN0 Configuration Register	C0CONR	XXh
021Bh			XXh
021Ch	CAN0 Receive Error Count Register	C0RECR	00h
021Dh	CAN0 Transmit Error Count Register	C0TECR	00h
021Eh	CAN0 Time Stamp Register	C0TSR	00h
021Fh			00h
0220h	CAN1 Message Control Register 0	C1MCTL0	00h
0221h	CAN1 Message Control Register 1	C1MCTL1	00h
0222h	CAN1 Message Control Register 2	C1MCTL2	00h
0223h	CAN1 Message Control Register 3	C1MCTL3	00h
0224h	CAN1 Message Control Register 4	C1MCTL4	00h
0225h	CAN1 Message Control Register 5	C1MCTL5	00h
0226h	CAN1 Message Control Register 6	C1MCTL6	00h
0227h	CAN1 Message Control Register 7	C1MCTL7	00h
0228h	CAN1 Message Control Register 8	C1MCTL8	00h
0229h	CAN1 Message Control Register 9	C1MCTL9	00h
022Ah	CAN1 Message Control Register 10	C1MCTL10	00h
022Bh	CAN1 Message Control Register 11	C1MCTL11	00h
022Ch	CAN1 Message Control Register 12	C1MCTL12	00h
022Dh	CAN1 Message Control Register 13	C1MCTL13	00h
022Eh	CAN1 Message Control Register 14	C1MCTL14	00h
022Fh	CAN1 Message Control Register 15	C1MCTL15	00h
0230h	CAN1 Control Register	C1CTLR	X0000001b
0231h			XX0X0000b
0232h	CAN1 Status Register	C1STR	00h
0233h			X0000001b
0234h	CAN1 Slot Status Register	C1SSTR	00h
0235h			00h
0236h	CAN1 Interrupt Control Register	C1ICR	00h
0237h			00h
0238h	CAN1 Extended ID Register	C1IDR	00h
0239h			00h
023Ah	CAN1 Configuration Register	C1CONR	XXh
023Bh			XXh
023Ch	CAN1 Receive Error Count Register	C1RECR	00h
023Dh	CAN1 Transmit Error Count Register	C1TECR	00h
023Eh	CAN1 Time Stamp Register	C1TSR	00h
023Fh			00h

X: Undefined

Table 4.12 SFR Information (12)

Address	Register	Symbol	After Reset
02C0h	CAN1 Message Box 6: Identifier / DLC		XXh
02C1h			XXh
02C2h			XXh
02C3h			XXh
02C4h			XXh
02C5h			XXh
02C6h	CAN1 Message Box 6: Data Field		XXh
02C7h			XXh
02C8h			XXh
02C9h			XXh
02CAh			XXh
02CBh			XXh
02CCh			XXh
02CDh			XXh
02CEh	CAN1 Message Box 6: Time Stamp		XXh
02CFh			XXh
02D0h	CAN1 Message Box 7: Identifier / DLC		XXh
02D1h			XXh
02D2h			XXh
02D3h			XXh
02D4h			XXh
02D5h			XXh
02D6h	CAN1 Message Box 7: Data Field		XXh
02D7h			XXh
02D8h			XXh
02D9h			XXh
02DAh			XXh
02DBh			XXh
02DCh			XXh
02DDh			XXh
02DEh	CAN1 Message Box 7: Time Stamp		XXh
02DFh			XXh
02E0h	CAN1 Message Box 8: Identifier / DLC		XXh
02E1h			XXh
02E2h			XXh
02E3h			XXh
02E4h			XXh
02E5h			XXh
02E6h	CAN1 Message Box 8: Data Field		XXh
02E7h			XXh
02E8h			XXh
02E9h			XXh
02EAh			XXh
02EBh			XXh
02ECh			XXh
02EDh			XXh
02EEh	CAN1 Message Box 8: Time Stamp		XXh
02EFh			XXh
02F0h	CAN1 Message Box 9: Identifier / DLC		XXh
02F1h			XXh
02F2h			XXh
02F3h			XXh
02F4h			XXh
02F5h			XXh
02F6h	CAN1 Message Box 9: Data Field		XXh
02F7h			XXh
02F8h			XXh
02F9h			XXh
02FAh			XXh
02FBh			XXh
02FCh			XXh
02FDh			XXh
02FEh	CAN1 Message Box 9: Time Stamp		XXh
02FFh			XXh

X: Undefined

5. Electrical Characteristics

5.1 Electrical Characteristics (T/V-ver.)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}	Supply voltage (VCC1 = VCC2)		VCC = AVCC	–0.3 to 6.5	V
AV_{CC}	Analog supply voltage		VCC = AVCC	–0.3 to 6.5	V
V_I	Input voltage	$\overline{RESET}$, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, VREF, XIN		–0.3 to VCC+0.3	V
		P7_1, P9_1		–0.3 to 6.5	V
V_O	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, XOUT		–0.3 to VCC+0.3	V
		P7_1, P9_1		–0.3 to 6.5	V
P_d	Power dissipation		Topr = 25°C	700	mW
T_{opr}	Operating ambient temperature	During MCU operation		T version: –40 to 85 V version: –40 to 125 (option)	°C
		During flash memory program and erase operation		0 to 60	
T_{stg}	Storage temperature			–65 to 150	°C

option: All options are on request basis.

Switching Characteristics

VCC = 5 V

(Referenced to VCC = 5 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.25 Memory Expansion Mode and Microprocessor Mode (for 2- to 3-wait setting, external area access and multiplexed bus selection)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.2		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(NOTE 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(NOTE 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(NOTE 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (in relation to Address)		(NOTE 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of Address		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25 \text{ [ns]}$$

4. Calculated according to the BCLK frequency as follows:

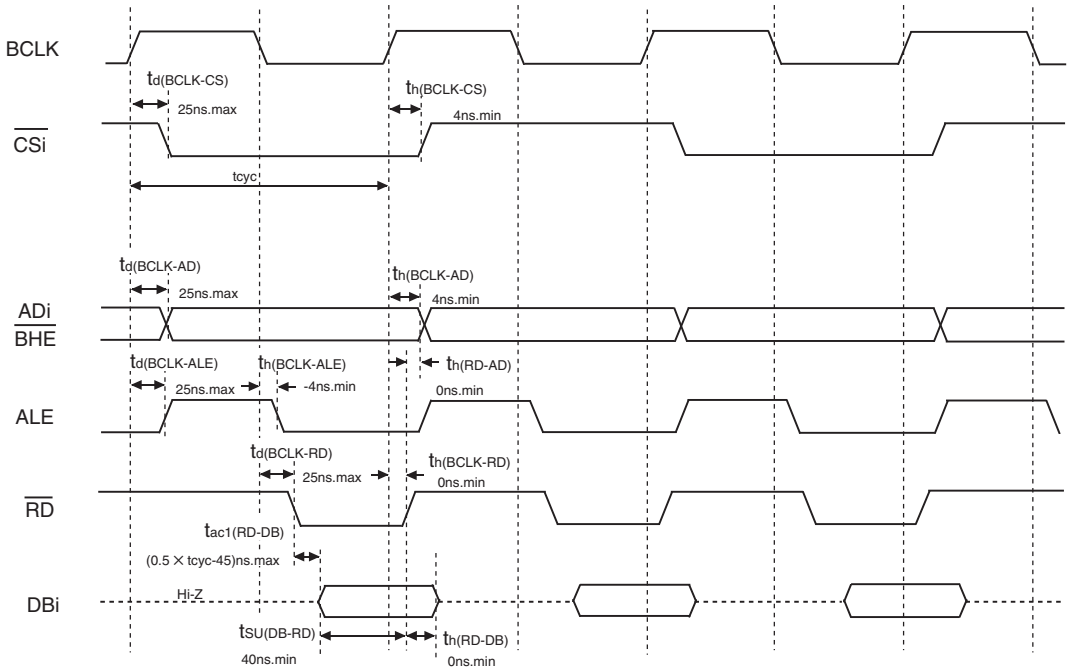
$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 \text{ [ns]}$$

Memory Expansion Mode and Microprocessor Mode

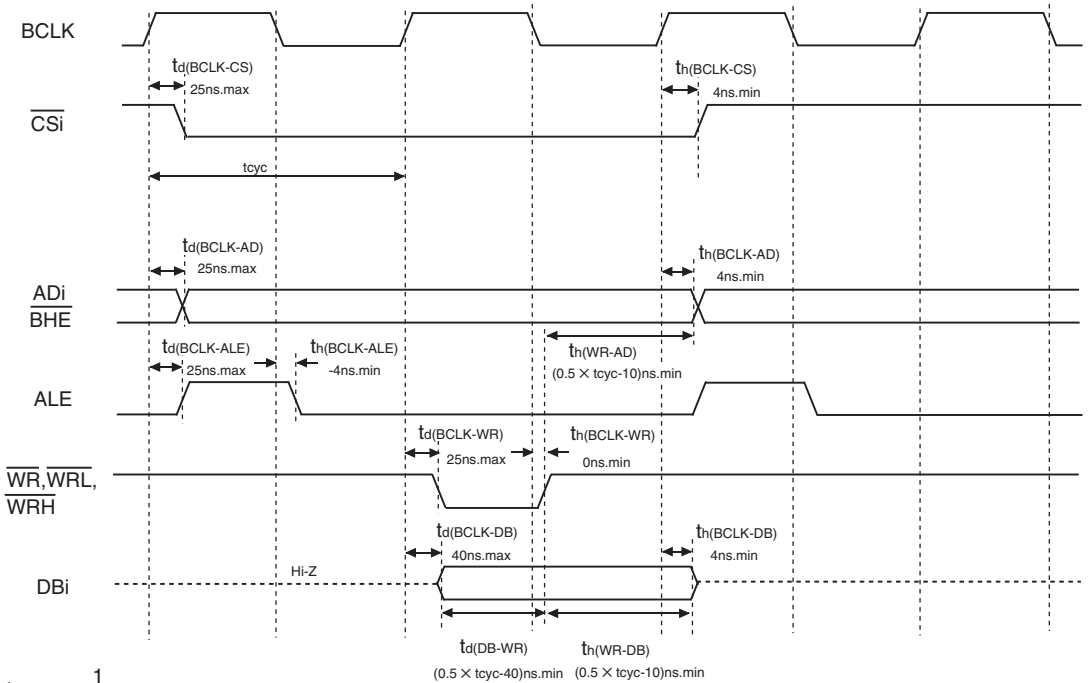
VCC = 5 V

(For setting with no wait)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.5 Timing Diagram (3)

Table 5.32 Electrical Characteristics (1) [1] **VCC = 5 V**

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7		I_{OH} = –5 mA	V_{CC}-2.0		V_{CC}	V
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7		I_{OH} = –200 µA	V_{CC}-0.3		V_{CC}	V
V_{OH}	HIGH output voltage	XOUT	HIGHPOWER	I_{OH} = –1 mA	3.0		V_{CC}	V
			LOWPOWER	I_{OH} = –0.5 mA	3.0		V_{CC}	
	HIGH output voltage	XCOUT	HIGHPOWER	With no load applied		2.5		V
			LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 5 mA			2.0	V
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 200 µA			0.45	V
V_{OL}	LOW output voltage	XOUT	HIGHPOWER	I_{OL} = 1 mA			2.0	V
			LOWPOWER	I_{OL} = 0.5 mA			2.0	
	LOW output voltage	XCOUT	HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK3, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SIN3			0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		2.5	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 5 V			5.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I = 0 V			–5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7		V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistance	XIN				1.5		MΩ
R_{fXCIN}	Feedback resistance	XCIN				15		MΩ
V_{RAM}	RAM retention voltage			At stop mode	2.0			V

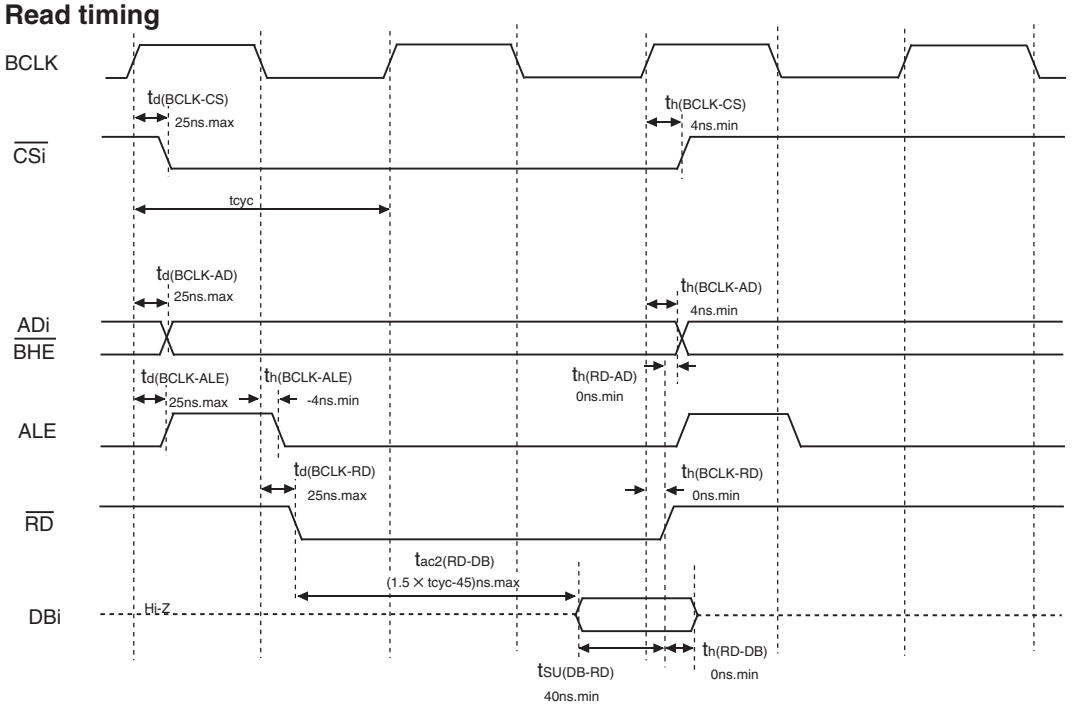
NOTES:
1. Referenced to VCC = 4.2 to 5.5 V, VSS = 0 V at Topr = –40 to 85°C, f(BCLK) = 24 MHz unless otherwise specified.

Memory Expansion Mode and Microprocessor Mode

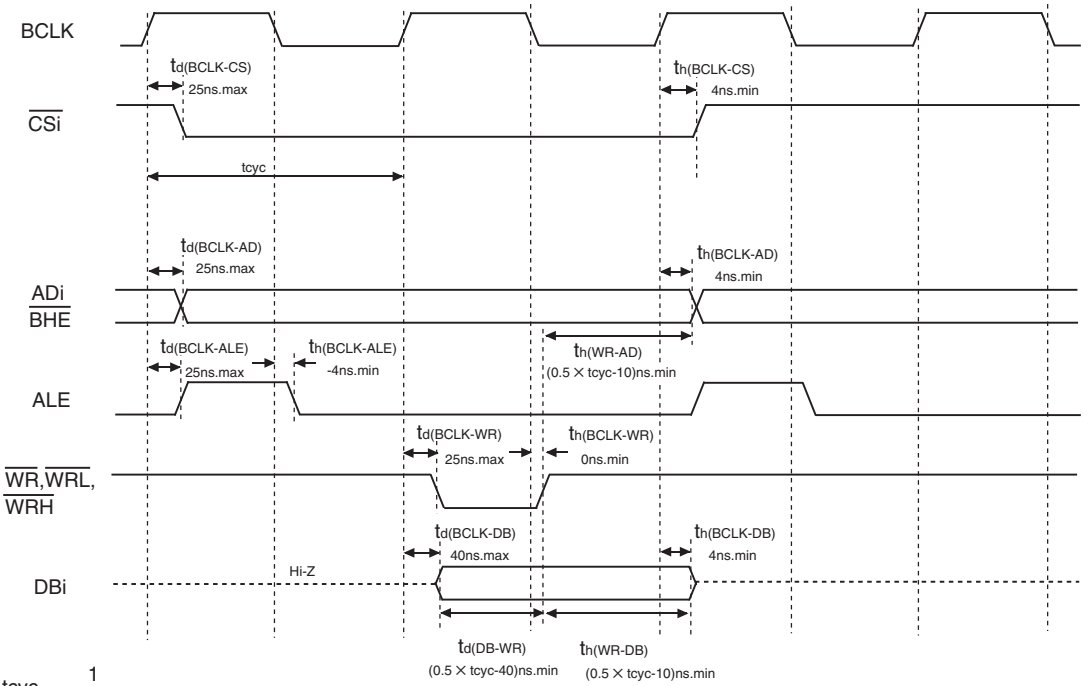
VCC = 5 V

(For 1-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions :

- VCC = 5 V
- Input timing voltage : V_{IL} = 0.8 V, V_{IH} = 2.0 V
- Output timing voltage : V_{OL} = 0.4 V, V_{OH} = 2.4 V

Figure 5.16 Timing Diagram (4)

Timing Requirements

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85°C unless otherwise specified)

Table 5.54 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	60		ns

Table 5.55 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	300		ns

Table 5.56 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 5.57 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 5.58 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	600		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	600		ns

Table 5.59 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

Switching Characteristics

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.67 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.21		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

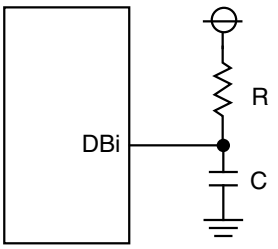
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting. When n = 1, f(BCLK) is 12.5 MHz or less.

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln (1 - V_{OL} / V_{CC})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2\ V_{CC}$, C = 30 pF, R =1 kΩ, hold time of output “L” level is
$t = -30\ pF \times 1\ k\Omega \times \ln (1 - 0.2\ V_{CC} / V_{CC}) = 6.7$ ns.



Switching Characteristics

VCC = 3.3 V

(Referenced to VCC = 3.3 V, VSS = 0 V, at Topr = –40 to 85 °C unless otherwise specified)

Table 5.68 Memory Expansion Mode and Microprocessor Mode (for 2- to 3-wait setting, external area access and multiplexed bus selection)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 5.21		50	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(NOTE 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			50	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(NOTE 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			40	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			40	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			50	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(NOTE 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(NOTE 1)		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time			40	ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(NOTE 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (in relation to Address)		(NOTE 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of Address		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \text{ [ns]}$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f(BCLK)} - 50 \text{ [ns]}$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \text{ [ns]}$$

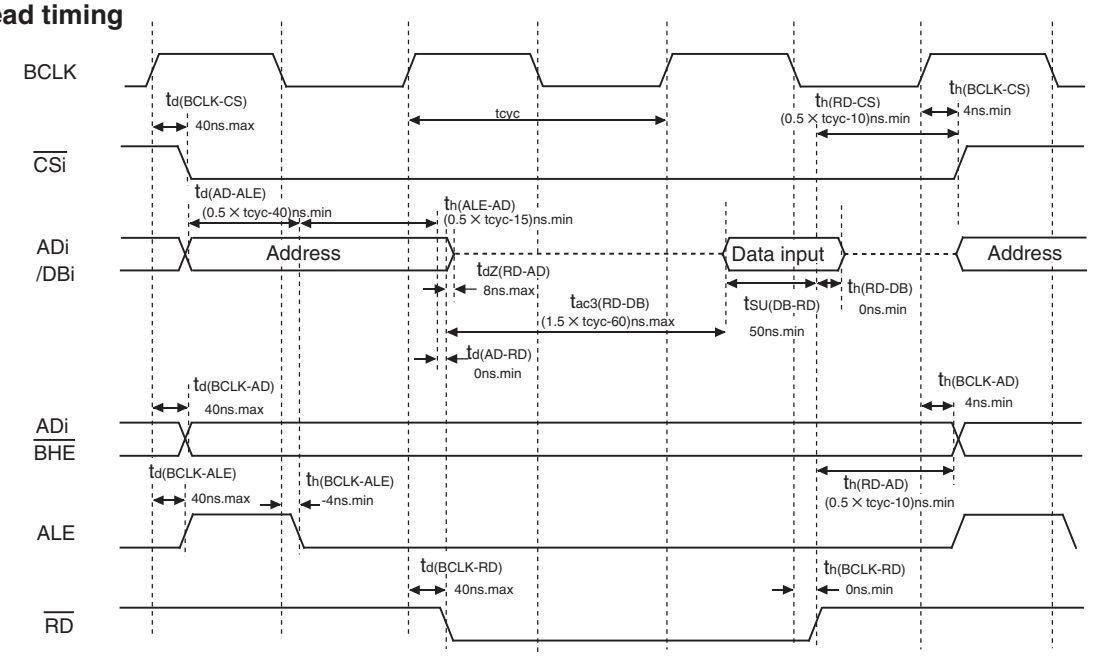
4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 \text{ [ns]}$$

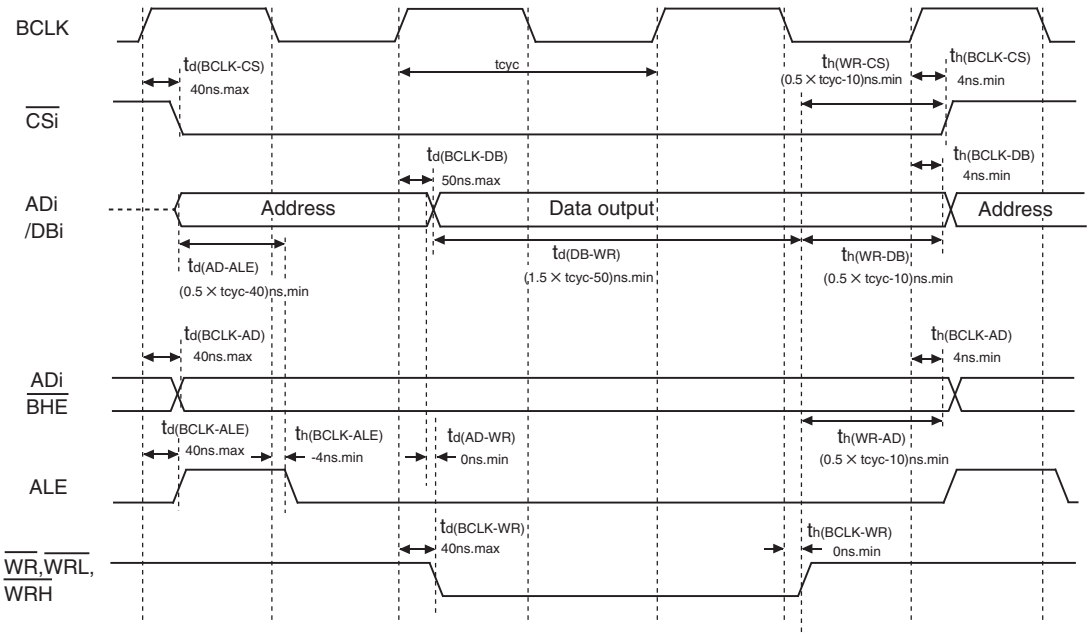
Memory Expansion Mode and Microprocessor Mode — VCC = 3.3 V

(For 2-wait setting, external area access and multiplexed bus selection)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

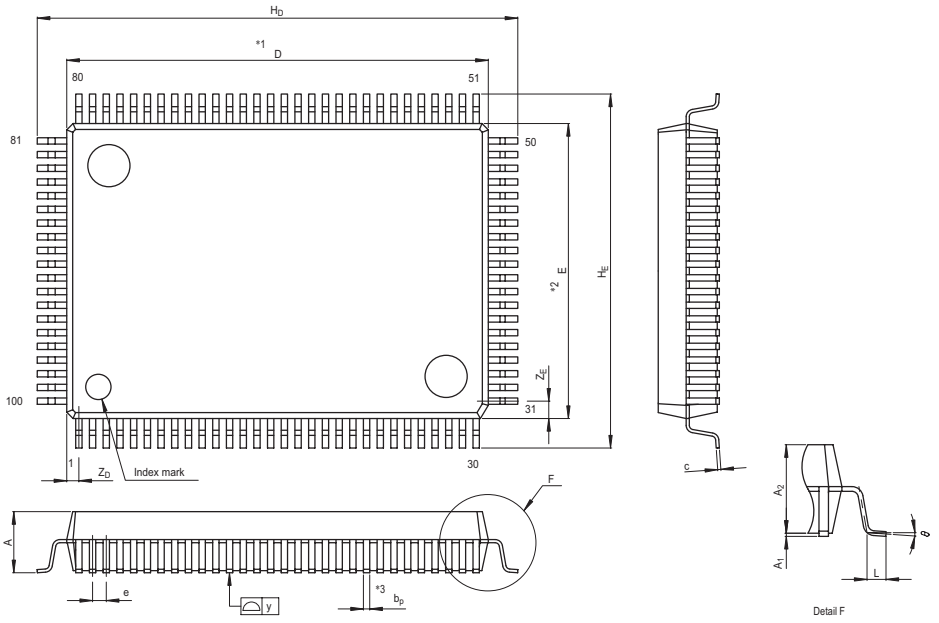
Measuring conditions :

- VCC = 3.3 V
- Input timing voltage : V_{IL} = 0.6 V, V_{IH} = 2.7 V
- Output timing voltage : V_{OL} = 1.65 V, V_{OH} = 1.65 V

Figure 5.28 Timing Diagram (7)

Appendix 1. Package Dimensions

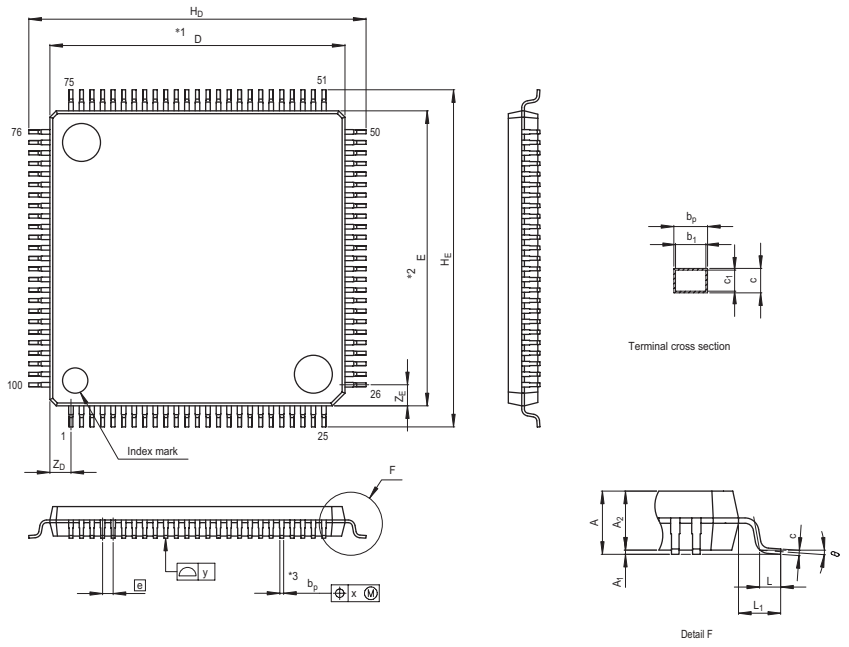
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	M16C/6N Group (M16C/6N4) Data Sheet

Rev.	Date	Description	
		Page	Summary
2.00	Nov. 10, 2004	34	Table 5.6 A/D Conversion Characteristics: "Tolerance Level Impedance" is added.
		35	Table 5.8 Power Supply Circuit Timing Characteristics: "$t_{d(M-L)}$" is deleted.
			Figure 5.2 Power Supply Circuit Timing Diagram is added.
		36	Table 5.10 Memory Expansion Mode and Microprocessor Mode: "$t_{d(BCLK-HLDA)}$" is deleted.
		38	Table 5.21 Serial I/O: Min. of standard in $t_{su(D-C)}$ is revised from "30" to "70".
		39	Table 5.23 Memory Expansion Mode and Microprocessor Mode (for setting with no wait)
			• Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15".
			• $t_{d(BCLK-HLDA)}$ is added.
		40	Table 5.24 Memory Expansion Mode and Microprocessor Mode (for 1- to 3-wait setting and external area access)
			• Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15".
			• $t_{d(BCLK-HLDA)}$ is added.
		41	Table 5.25 Memory Expansion Mode and Microprocessor Mode (for 2- to 3-wait setting, external area access and multiplexed bus selection)
			• $t_{d(BCLK-HLDA)}$ is added.
			• Max. of Standard in $t_{d(BCLK-ALE)}$ is revised from "25" to "15".
		42	Figure 5.4 Timing Diagram (1): "XIN input" is added.
		44, 45	Figures 5.6 and 5.7 Timing Diagram (3) (4): "DB" in Read timing is revised to "DBi".
		46, 47	Figures 5.8 and 5.9 Timing Diagram (5) (6): "DB" in Write timing is revised to "DBi".
		49	Figure 5.11 Timing Diagram (8)
			• "ADi/DB" in Read/Write timing is revised to "ADi/DBi".
		50	Appendix 1. Package Dimensions: 100P6Q-A is added.
2.10	Jun. 24, 2005	–	Revised edition issued
			* The contents of product are revised. (Normal-ver. is added.)
			* Revised parts and revised contents are as follows (except for expressional change).
		2	Table 1.1 Performance outline of M16C/6N Group (M16C/6N4)
			• Performance outline of Normal-ver. is added.
		4	Table 1.2 Product List is revised. (Normal-ver. is added.)
			Figure 1.2 Type No., Memory Size, and Package:
			• "(no): Normal-ver." is added to Characteristics.
		19	Figure 4.7 SFR Information (7): NOTE 1 is revised.
		32	Table 5.4 Electrical Characteristics (1)
			• Measuring Condition of V_{OL} is revised from "I_{OL} = –200μA" to "I_{OL} = 200μA".
		33	Table 5.5 Electrical Characteristics (2): Mask ROM (5th item)
			• "f(XCIN)" is changed to "(f(BCLK)).
		34	Table 5.6 A/D Conversion Characteristics: "Tolerance Level Impedance" is deleted.
2.40	Aug. 25, 2006	–	Revised edition issued
			* Electric Characteristics of Normal-ver. is added.
			* Revised parts and revised contents are as follows (except for expressional change).
		1	1.1 Applications: Comment of Normal-ver. is added.
		4	Table 1.2 Product Information
			• Status of development is revised and NOTES 1 and 2 are added.

REVISION HISTORY	M16C/6N Group (M16C/6N4) Data Sheet

Rev.	Date	Description	
		Page	Summary
2.40	Aug. 25, 2006	7, 8	Tables 1.3 and 1.4 List of Pin Names (1)(2) are added.
		9	Table 1.5 Pin Functions (1) • 3.0 to 5.5 V (Normal-ver.) is added to Description of Power supply input.
		22	Table 4.8 SFR Information (8) • The value of After Reset in IDB0 register is revised. • The value of After Reset in IDB1 register is revised.
		33	Table 5.3 Recommended Operating Conditions (2) • Power supply ripple is deleted. (three items) Figure 5.1 Voltage Fluctuation Timing is deleted.
		34	Table 5.4 Electrical Characteristics (1): Hysteresis XIN is deleted.
		52 to 87	5.2 Electrical Characteristics (Normal-ver.) is added.