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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dg256cfue

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The following items should be considered when using a derivative (**Table 0-1**):

- **Registers**

- Do not write or read CAN0 registers (after reset: address range \$0140 - \$017F), if using a derivative without CAN0.
- Do not write or read CAN1 registers (after reset: address range \$0180 - \$01BF), if using a derivative without CAN1.
- Do not write or read CAN4 registers (after reset: address range \$0280 - \$02BF), if using a derivative without CAN4.
- Do not write or read BDLC registers (after reset: address range \$00E8 - \$00EF), if using a derivative without BDLC.

- **Interrupts**

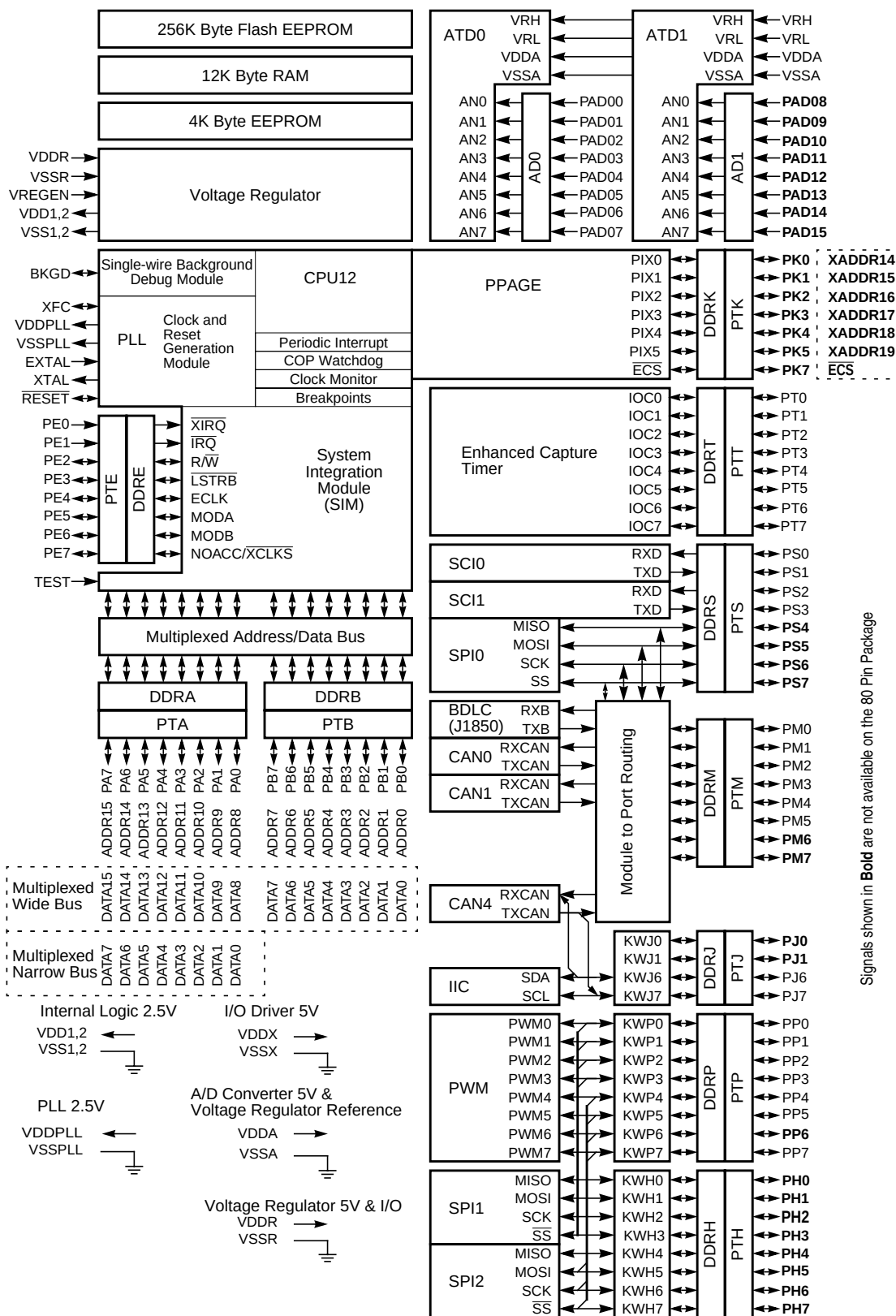
- Fill the four CAN0 interrupt vectors (\$FFB0 - \$FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0.
- Fill the four CAN1 interrupt vectors (\$FFA8 - \$FFAF) according to your coding policies for unused interrupts, if using a derivative without CAN1.
- Fill the four CAN4 interrupt vectors (\$FF90 - \$FF97) according to your coding policies for unused interrupts, if using a derivative without CAN4.
- Fill the BDLC interrupt vector (\$FFC2, \$FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC.

- **Ports**

- The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0.
- The CAN1 pin functionality (TXCAN1, RXCAN1) is not available on port PM3 and PM2, if using a derivative without CAN1.
- The CAN4 pin functionality (TXCAN4, RXCAN4) is not available on port PJ7, PJ6, PM5, PM7, PM6, PM5 and PM4, if using a derivative without CAN0.
- The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC.
- Do not write MODRR1 and MODRR0 bits of Module Routing Register (PIM_9DP256 Block Guide), if using a derivative without CAN0.
- Do not write MODRR3 and MODRR2 bits of Module Routing Register (PIM_9DP256 Block Guide), if using a derivative without CAN4.

Document References

Figure 1-1 MC9S12DT256 Block Diagram



Signals shown in **Bold** are not available on the 80 Pin Package

\$0040 - \$007F**ECT (Enhanced Capture Timer 16 Bit 8 Channels)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$006C	Reserved	Read:								
		Write:								
\$006D	TIMTST	Read:	0	0	0	0	0	0	TCBYP	0
	Test Only	Write:								
\$006E	Reserved	Read:								
		Write:								
\$006F	Reserved	Read:								
		Write:								
\$0070	PBCTL	Read:	0	PBEN	0	0	0	0	PBOVI	0
		Write:								
\$0071	PBFLG	Read:	0	0	0	0	0	0	PBOVF	0
		Write:								
\$0072	PA3H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0073	PA2H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0074	PA1H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0075	PA0H	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0076	MCCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$0077	MCCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$0078	TC0H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$0079	TC0H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$007A	TC1H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$007B	TC1H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$007C	TC2H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$007D	TC2H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
\$007E	TC3H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
\$007F	TC3H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

\$0080 - \$009F**ATD0 (Analog to Digital Converter 10 Bit 8 Channel)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0080	ATD0CTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
\$0081	ATD0CTL1	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0140 - \$017F**CAN0 (Motorola Scalable CAN - MSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
\$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
\$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
\$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
\$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
\$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
\$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
\$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
\$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
\$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0150 - \$0153	CAN0IDAR0 - CAN0IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0154 - \$0157	CAN0IDMR0 - CAN0IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0158 - \$015B	CAN0IDAR4 - CAN0IDAR7	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$015C - \$015F	CAN0IDMR4 - CAN0IDMR7	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0160 - \$016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see Table 1-2							
		Write:								
\$0170 - \$017F	CAN0TXFG	Read:	FOREGROUND TRANSMIT BUFFER see Table 1-2							
		Write:								

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
\$xxx0	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CANxRIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
\$xxx1	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CANxRIDR1	Write:								

\$0240 - \$027F**PIM (Port Integration Module PIM_9DP256)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$024D	PPSS	Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
\$024E	WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
\$024F	Reserved	Read: Write:	0	0	0	0	0	0	0	0
\$0250	PTM	Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
\$0251	PTIM	Read: Write:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
\$0252	DDRM	Read: Write:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
\$0253	RDRM	Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
\$0254	PERM	Read: Write:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
\$0255	PPSM	Read: Write:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
\$0256	WOMM	Read: Write:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
\$0257	MODRR	Read: Write:	0	MODRR6	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
\$0258	PTP	Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
\$0259	PTIP	Read: Write:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
\$025A	DDRP	Read: Write:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
\$025B	RDRP	Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
\$025C	PERP	Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
\$025D	PPSP	Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
\$025E	PIEP	Read: Write:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
\$025F	PIFP	Read: Write:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
\$0260	PTH	Read: Write:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
\$0261	PTIH	Read: Write:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
\$0262	DDRH	Read: Write:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
\$0263	RDRH	Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
\$0264	PERH	Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
\$0265	PPSH	Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0

2.3.9 PAD7 / AN07 / ETRIG0 — Port AD Input Pin of ATD0

PAD7 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

2.3.10 PAD[06:00] / AN[06:00] — Port AD Input Pins of ATD0

PAD06 - PAD00 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD0.

2.3.11 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.12 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.13 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus. The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive or a Pierce Oscillator. If input is a logic high a Colpitts oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.

2.3.18 PE2 / $\overline{R/W}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

2.3.19 PE1 / $\overline{IRQ}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.20 PE0 / $\overline{XIRQ}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.21 PH7 / KWH7 / $\overline{SS2}$ — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 2 (SPI2).

2.3.22 PH6 / KWH6 / SCK2 — Port H I/O Pin 6

PH6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

2.3.23 PH5 / KWH5 / MOSI2 — Port H I/O Pin 5

PH5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

2.3.24 PH4 / KWH4 / MISO2 — Port H I/O Pin 2

PH4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

2.3.25 PH3 / KWH3 / $\overline{SS1}$ — Port H I/O Pin 3

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 1 (SPI1).

2.3.40 PM1 / TXCAN0 / TXB — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the transmit pin TXB of the BDLC.

2.3.41 PM0 / RXCAN0 / RXB — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0). It can be configured as the receive pin RXB of the BDLC.

2.3.42 PP7 / KWP7 / PWM7 / SCK2 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

2.3.43 PP6 / KWP6 / PWM6 / $\overline{SS2}$ — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 2 (SPI2).

2.3.44 PP5 / KWP5 / PWM5 / MOSI2 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

2.3.45 PP4 / KWP4 / PWM4 / MISO2 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

2.3.46 PP3 / KWP3 / PWM3 / $\overline{SS1}$ — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 1 (SPI1).

Table 4-2 Clock Selection Based on PE7

PE7 = XCLKS	Description
0	Pierce Oscillator/external clock selected

Table 4-3 Voltage Regulator VREGEN

VREGEN	Description
1	Internal Voltage Regulator enabled
0	Internal Voltage Regulator disabled, VDD1,2 and VDDPLL must be supplied externally with 2.5V

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

6.6 HCS12 Breakpoint (BKP) Block Description

Consult the BKP Block guide for information on HCS12 breakpoint block

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

7.1.1 $\overline{\text{XCLKS}}$

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.13 PE7 / NOACC / XCLKS — Port E I/O Pin 7**).

Section 8 Enhanced Capture Timer (ECT) Block Description

Consult the ECT_16B8C Block User Guide for information about the Enhanced Capture Timer module. When the ECT_16B8C Block Guide refers to freeze mode this is equivalent to active BDM mode.

Section 9 Analog to Digital Converter (ATD) Block Description

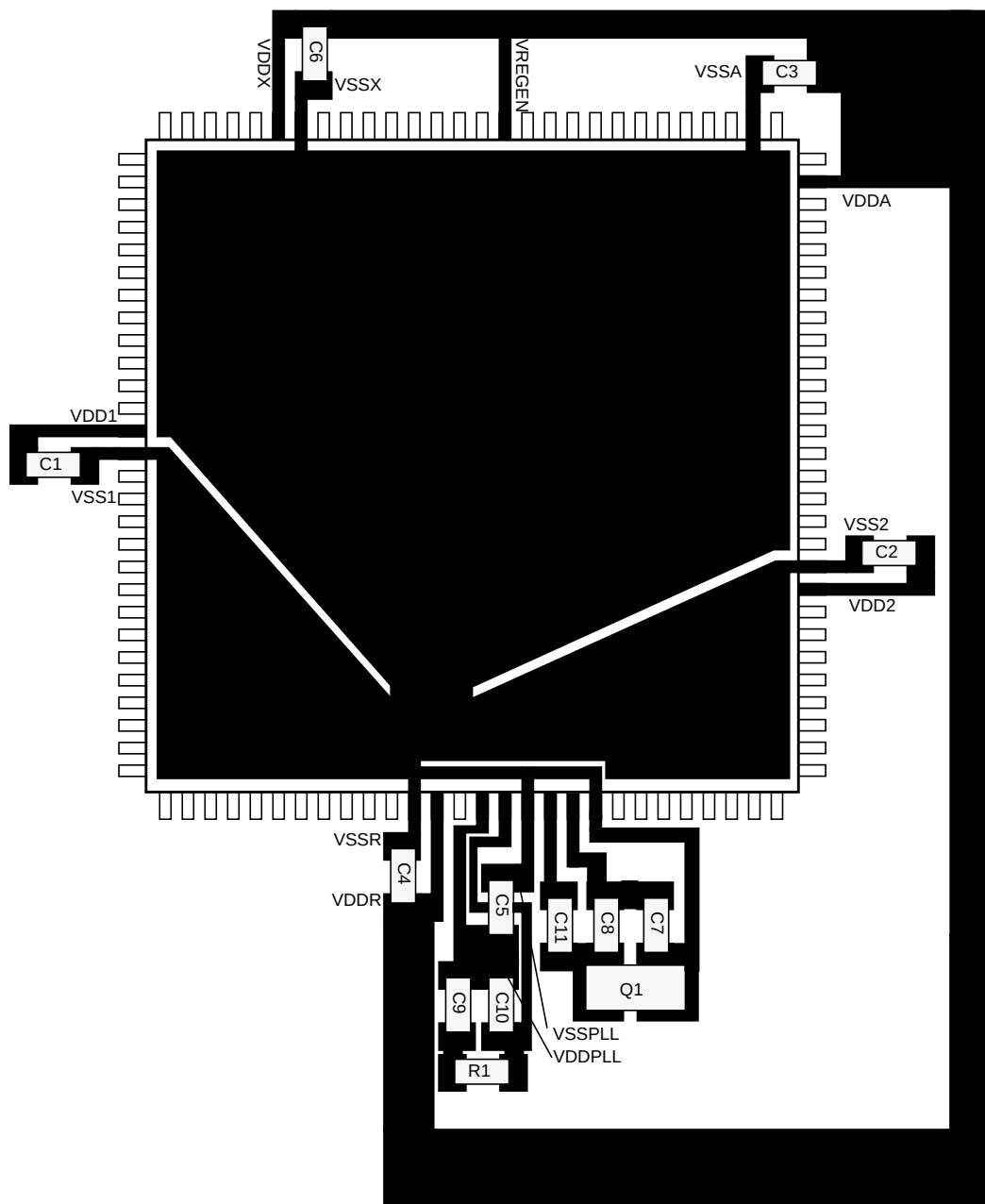
There are two Analog to Digital Converters (ATD1 and ATD0) implemented on the MC9S12DT256. Consult the ATD_10B8C Block User Guide for information about each Analog to Digital Converter module. When the ATD_10B8C Block Guide refers to freeze mode this is equivalent to active BDM mode.

Section 10 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 11 Serial Communications Interface (SCI) Block Description

Figure 20-1 Recommended PCB Layout for 112LQFP Colpitts Oscillator



2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply.
The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX} , V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA} .
4. Those pins are internally clamped to V_{SSPLL} and V_{DDPLL} .
5. This pin is clamped low to V_{SSR} , but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	C	Machine Model (MM)	V_{MM}	200	-	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	C	Latch-up Current at $T_A = 125^\circ\text{C}$ positive negative	I_{LAT}	+100 -100	-	mA
5	C	Latch-up Current at $T_A = 27^\circ\text{C}$ positive negative	I_{LAT}	+200 -200	-	mA

given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			65	mA
2	P P	Wait Supply current All modules enabled, PLL on only RTI enabled ¹	I_{DDW}			40 5	mA
3	C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) ^{1, 2} -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}		370 400 450 550 600 650 800 850 1200	500 1600 2100 5000	μA
4	C C C C C C C	Pseudo Stop Current (RTI and COP enabled) ^{1, 2} -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		570 600 650 750 850 1200 1500		μA
5	C P C C P C P C P	Stop Current ² -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}		12 25 100 130 160 200 350 400 600	100 1200 1700 5000	μA

NOTES:

1. PLL off

2. At those low power dissipation levels $T_J = T_A$ can be assumed

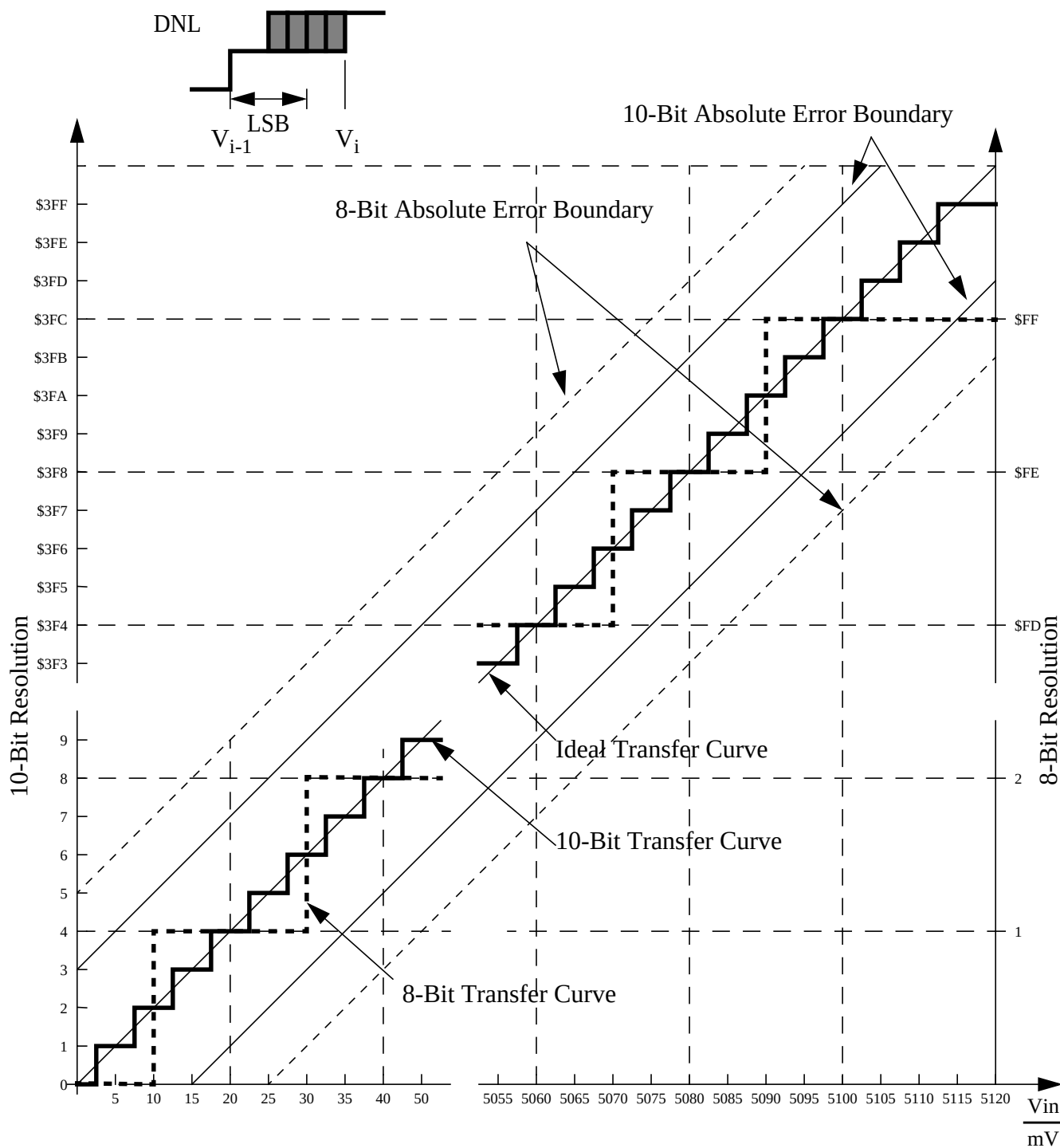


Figure A-1 ATD Accuracy Definitions

NOTE: Figure A-1 shows only definitions, for specification values refer to Table A-10.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{\text{ref}}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{\text{ref}}}{4 \cdot 10}; (\zeta = 0.9)$$

$$f_C < 25\text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{\text{VCO}}}{f_{\text{ref}}} = 2 \cdot (\text{synr} + 1) = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth $f_C=10\text{kHz}$:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} = 2 \cdot \pi \cdot 50 \cdot 10\text{kHz} / (316.7\text{Hz}/\Omega) = 9.9\text{k}\Omega \approx 10\text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) = 5.19\text{nF} \approx 4.7\text{nF}$$

The capacitance C_p should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10 \quad C_p = 470\text{pF}$$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-3**. With each transition of the clock f_{cmp} , the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-4**.

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-10** with the actual timing values shown on table **Table A-21**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.