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Details

Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	CANbus, I ² C, SCI, SPI
Peripherals	PWM, WDT
Number of I/O	59
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12dj256cfue

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- Compatible with I2C Bus standard
- Multi-master operation
- Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP package
 - I/O lines with 5V input and drive capability
 - 5V A/D converter inputs
 - Operation at 50MHz equivalent to 25MHz Bus Speed
 - Development support
 - Single-wire background debug™ mode (BDM)
 - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
 - Normal Single-Chip Mode
 - Normal Expanded Wide Mode
 - Normal Expanded Narrow Mode
 - Emulation Expanded Wide Mode
 - Emulation Expanded Narrow Mode
- Special Operating Modes
 - Special Single-Chip Mode with active Background Debug Mode
 - Special Test Mode (**Motorola use only**)
 - Special Peripheral Mode (**Motorola use only**)

Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
\$1000 - \$3FFF	RAM array	12288
\$4000 - \$7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
\$8000 - \$BFFF	Flash EEPROM Page Window	16384
\$C000 - \$FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at \$FF80 - \$FFFF	16384

\$00F0 - \$00F7**SPI1 (Serial Peripheral Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00F0	SPI1CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
\$00F1	SPI1CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
\$00F2	SPI1BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
\$00F3	SPI1SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
\$00F4	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00F5	SPI1DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
\$00F6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00F7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$00F8 - \$00FF**SPI2 (Serial Peripheral Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00F8	SPI2CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
\$00F9	SPI2CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
\$00FA	SPI2BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
\$00FB	SPI2SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
\$00FC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00FD	SPI2DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
\$00FE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

\$0100 - \$010F**Flash Control Register (fts256k)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
\$0101	FSEC	Read:	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
\$0102	FTSTMOD	Read:	0	0	0	WRALL	0	0	0	0
		Write:								
\$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	BKSEL1	BKSEL0
		Write:								

\$0140 - \$017F**CAN0 (Motorola Scalable CAN - MSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
\$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
\$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
\$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
\$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
\$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
\$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
\$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
\$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
\$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0150 - \$0153	CAN0IDAR0 - CAN0IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0154 - \$0157	CAN0IDMR0 - CAN0IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0158 - \$015B	CAN0IDAR4 - CAN0IDAR7	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$015C - \$015F	CAN0IDMR4 - CAN0IDMR7	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0160 - \$016F	CAN0RXFG	Read:	BACKGROUND RECEIVE BUFFER see Table 1-2							
		Write:								
\$0170 - \$017F	CAN0TXFG	Read:	BACKGROUND TRANSMIT BUFFER see Table 1-2							
		Write:								

Table 1-2 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
\$xxx0	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CANxRIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
\$xxx1	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CANxRIDR1	Write:								

\$0180 - \$01BF**CAN1 (Motorola Scalable CAN - MSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$0180	CAN1CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
\$0181	CAN1CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
\$0182	CAN1BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
\$0183	CAN1BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
\$0184	CAN1RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
\$0185	CAN1RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
\$0186	CAN1TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
\$0187	CAN1TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
\$0188	CAN1TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
\$0189	CAN1TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
\$018A	CAN1TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
\$018B	CAN1IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
\$018C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$018D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$018E	CAN1RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
\$018F	CAN1TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0190	CAN1IDAR0	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0191	CAN1IDAR1	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0192	CAN1IDAR2	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0193	CAN1IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0194	CAN1IDMR0	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0195	CAN1IDMR1	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0196	CAN1IDMR2	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0197	CAN1IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0198	CAN1IDAR4	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								

\$0280 - \$02BF**CAN4 (Motorola Scalable CAN - MSCAN)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$028C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$028D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
\$028E	CAN4RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
\$028F	CAN4TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
\$0290	CAN4IDAR0	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0291	CAN4IDAR1	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0292	CAN4IDAR2	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0293	CAN4IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0294	CAN4IDMR0	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0295	CAN4IDMR1	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0296	CAN4IDMR2	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0297	CAN4IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0298	CAN4IDAR4	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$0299	CAN4IDAR5	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$029A	CAN4IDAR6	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$029B	CAN4IDAR7	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
\$029C	CAN4IDMR4	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$029D	CAN4IDMR5	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$029E	CAN4IDMR6	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$029F	CAN4IDMR7	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$02A0 - \$02AF	CAN4RXFG	Read:	FOREGROUND RECEIVE BUFFER see Table 1-2							
		Write:								
\$02B0 - \$02BF	CAN4TXFG	Read:	FOREGROUND TRANSMIT BUFFER see Table 1-2							
		Write:								

2.3.26 PH2 / KWH2 / SCK1 — Port H I/O Pin 2

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.27 PH1 / KWH1 / MOSI1 — Port H I/O Pin 1

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.28 PH0 / KWH0 / MISO1 — Port H I/O Pin 0

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.29 PJ7 / KWJ7 / TXCAN4 / SCL — PORT J I/O Pin 7

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the transmit pin TXCAN for the Motorola Scalable Controller Area Network controller 4 (CAN4) or the serial clock pin SCL of the IIC module.

2.3.30 PJ6 / KWJ6 / RXCAN4 / SDA — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the receive pin RXCAN for the Motorola Scalable Controller Area Network controller 4 (CAN4) or the serial data pin SDA of the IIC module.

2.3.31 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

2.3.32 PK7 / $\overline{\text{ECS}}$ / ROMONE — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). During MCU normal expanded wide and narrow modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMONE). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit.

Section 3 System Clock Description

3.1 Overview

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules.

Consult the CRG Block User Guide for details on clock generation.

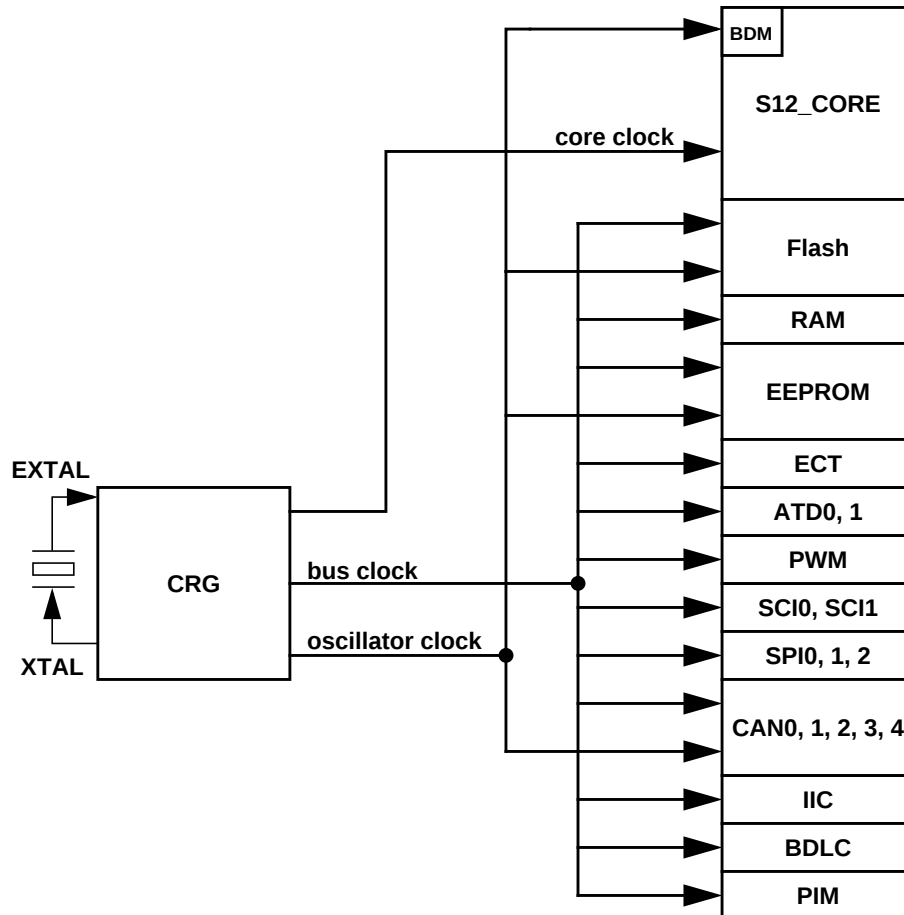
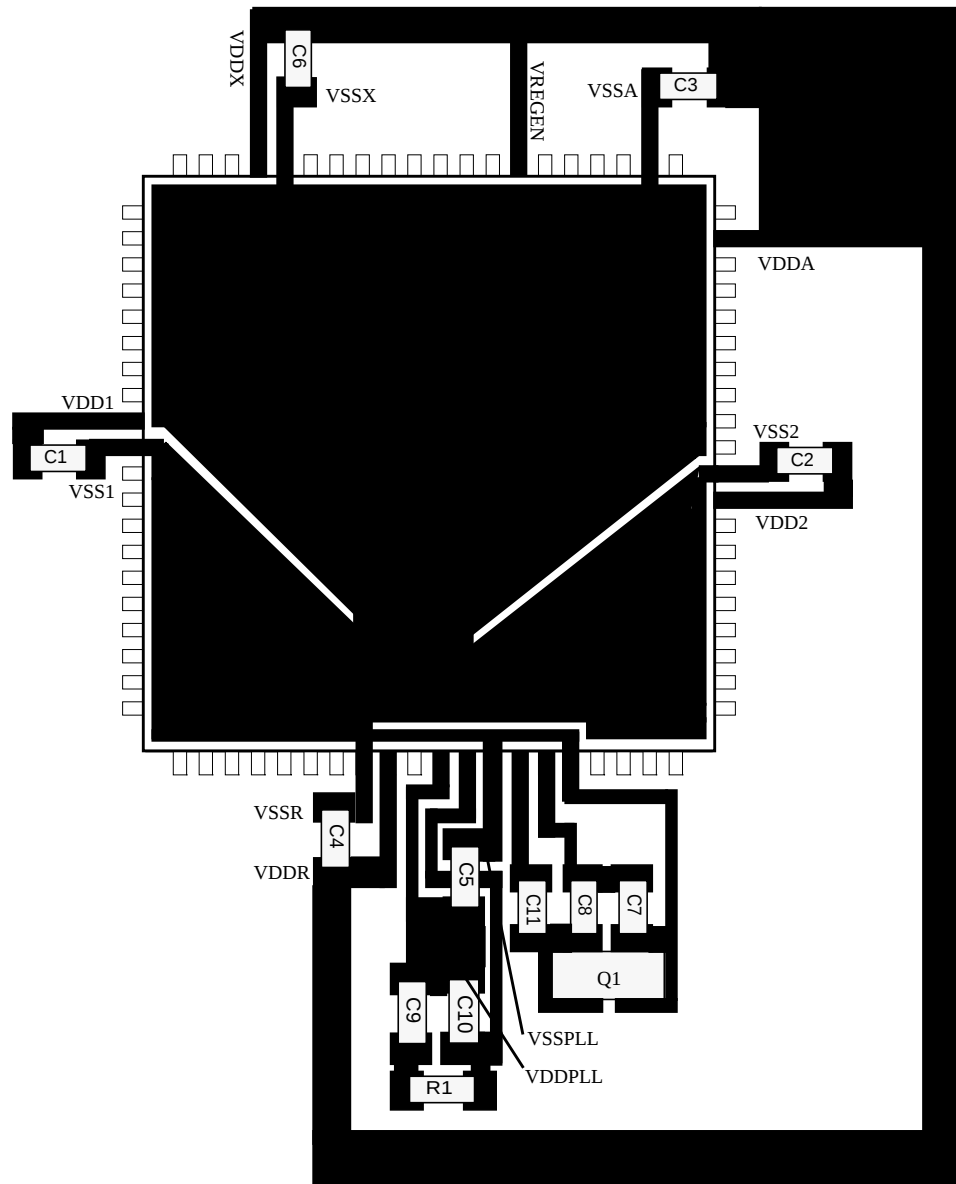


Figure 3-1 Clock Connections

Figure 20-2 Recommended PCB Layout for 80QFP Colpitts Oscillator



$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

For $R_{DS(on)}$ is valid:

$$R_{DS(on)} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DS(on)} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-7** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DS(on)} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

A.5 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.5.1 Startup

Table A-14 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block Guide.

Table A-14 Startup Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.5.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc} .

A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.5.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

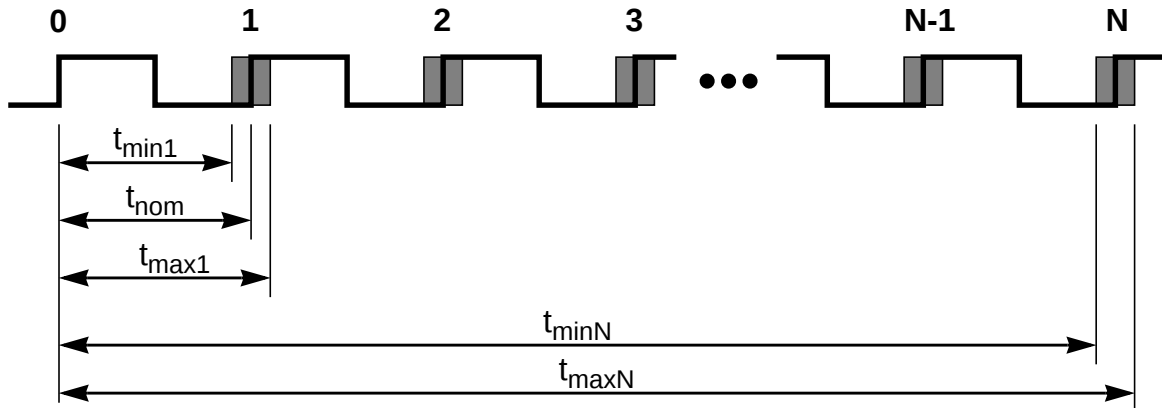


Figure A-4 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{\text{max}}(N)}{N \cdot t_{\text{nom}}}\right|, \left|1 - \frac{t_{\text{min}}(N)}{N \cdot t_{\text{nom}}}\right|\right)$$

For $N < 100$, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

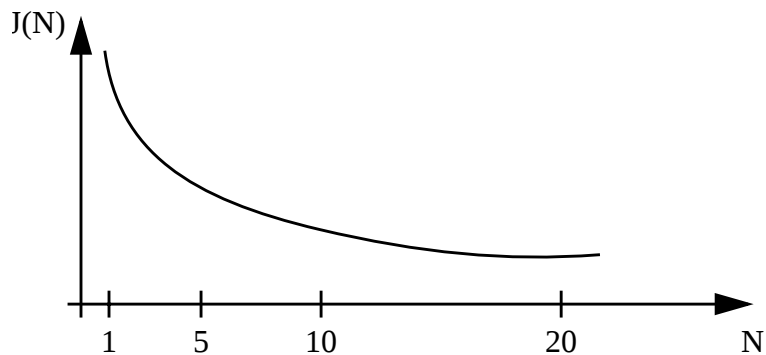
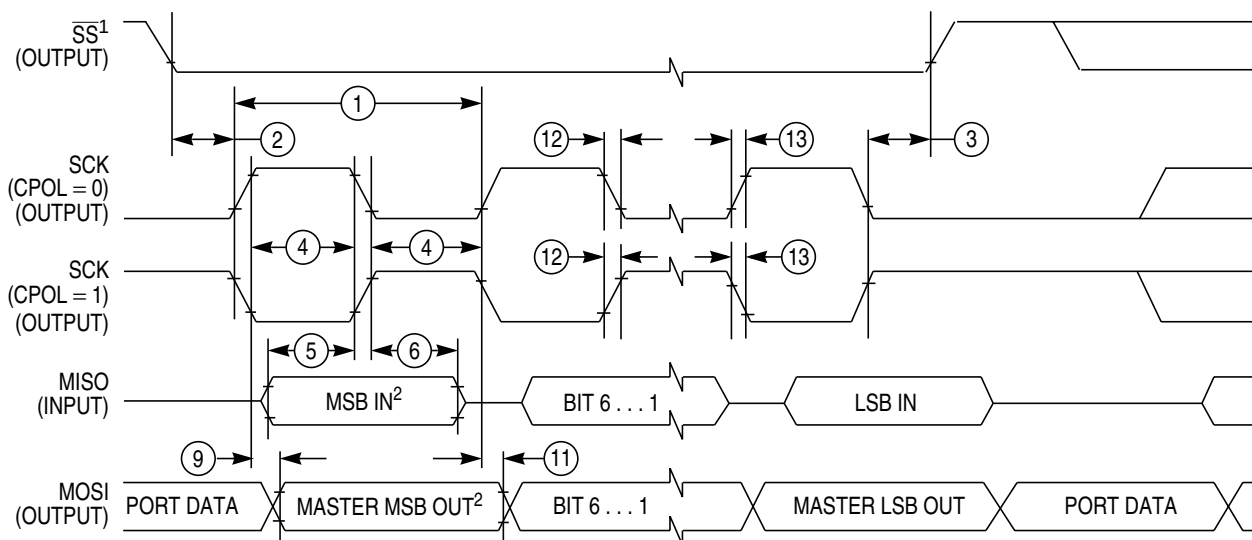


Figure A-5 Maximum bus clock jitter approximation



1. If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-7 SPI Master Timing (CPHA=1)

In **Table A-19** the timing characteristics for master mode are listed.

Table A-19 SPI Master Mode Timing Characteristics

Num	Characteristic	Symbol				Unit
			Min	Typ	Max	
1	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3	Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	30	ns
10	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

A.7.2 Slave Mode

In **Figure A-8** the timing diagram for slave mode with transmission format CPHA=0 is depicted.

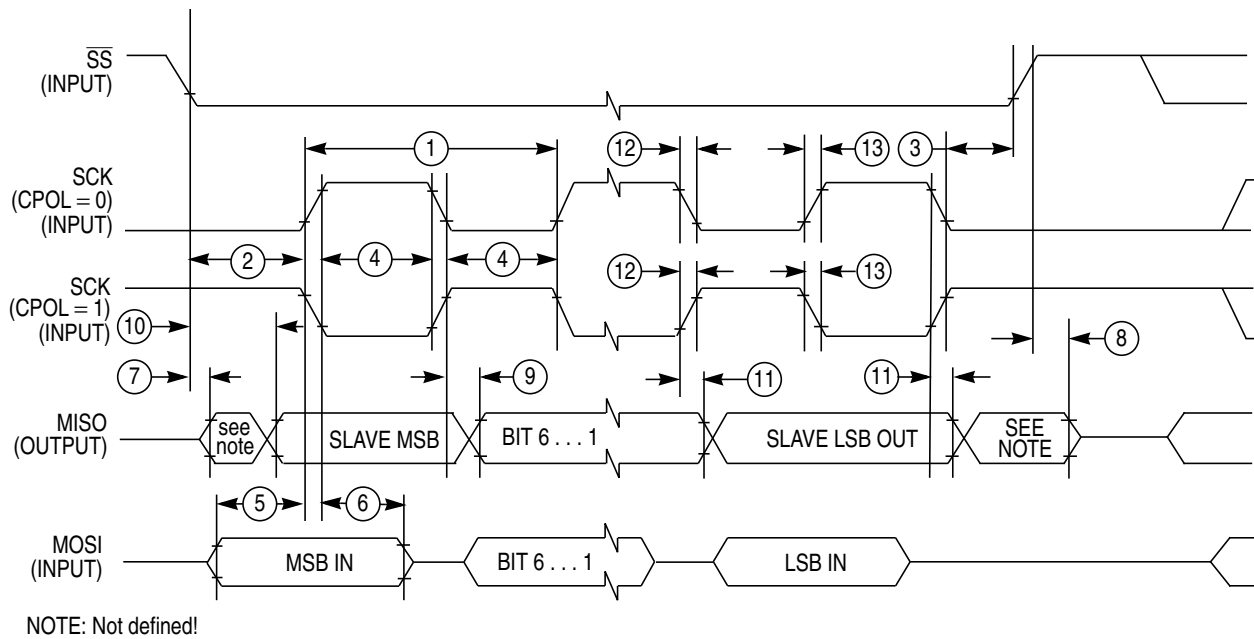


Figure A-8 SPI Slave Timing (CPHA=0)

In **Figure A-9** the timing diagram for slave mode with transmission format CPHA=1 is depicted.

Table A-21 Expanded Bus Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted, $C_{LOAD} = 50pF$							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
34	D	IPIPO[1:0] valid time to E rise ($PW_{EL} - t_{P0D}$)	t_{P0V}	11			ns
35	D	IPIPO[1:0] delay time ¹ ($PW_{EH} - t_{P1V}$)	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

NOTES:

1. Affected by clock stretch: add $N \times t_{cyc}$ where $N=0,1,2$ or 3 , depending on the number of clock stretches.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12DT256 packages.